## SERVICE MANUAL

## MODEL 3582A SPECTRUM ANALYZER

## Serial Numbers: 1747A00101 thru 1747A00125 And 1809A00126 and greater

## IMPORTANT NOTICE

This manual applies to instruments with the above serial number prefixes. As changes are made in the instrument to improve performance and reliability, the appropriate pages will be revised to include this information.

## WARNING

To help minimize the possibility of electrical fire or shock hazards, do not expose this instrument to rain or excessive moisture.

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## CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

## WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment [,except that in the case of certain components listed in Section I of this manual, the warranty shall be for the specified period] . During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by -hp-. Buyer shall prepay shipping charges to -hp- and -hp- shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to -hp- from another country.

Hewlett-Packard warrants that its software and firmware designated by -hp- for use with an instrument will execute its programming instructions when properly installed on that instrument. Hewlett-Packard does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

## LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HEWLETT-PACKARD SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

## EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HEWLETTPACKARD SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE<br>Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

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## CATHODE-RAY TUBE WARRANTY AND INSTRUCTIONS

The cathode-ray tube (CRT) supplied in your Hewlett-Packard Instrument and replacement CRT's purchased from -hp- are warranted by the Hewlett-Packard Company against electrical failure for a period of one year from the date of shipment from Colorado Springs. Broken tubes and tubes with phosphor or mesh burns are not included under this warranty. No other warranty is expressed or implied.

## INSTRUCTION TO CUSTOMERS

If the CRT is broken when received, a claim should be made with the responsible carrier. All warranty claims with Hewlett-Packard should be processed through your nearest HewlettPackard Sales/Service Office (listed at rear of instrument manual).

## INSTRUCTIONS TO SALES/SERVICE OFFICE

Return defective CRT in the replacement CRT packaging material. If packaging material is not available, contact CRT Customer Service in Colorado Springs. The Colorado Springs Division must evaluate all CRT claims for customer warranty, Material Failure Report (MFR) credit, and Heart System credit. A CRT Failure Report form (see reverse side of this page) must be completely filled out and sent with the defective CRT to the following address:

HEWLETT-PACKARD COMPANY<br>1900 Garden of the Gods Road Colorado Springs, Colorado 80907

## Parcel Post Address:

P.O. Box 2197

Colorado Springs, Colorado 80901

## Attention: CRT Customer Service

Defective CRT's not covered by warranty may be returned to Colorado Springs for disposition. These CRT's, in some instances, will be inspected and evaluated for reliability information by our engineering staff to facilitate product improvements. The Colorado Springs Division is equipped to safely dispose of CRT's without the risks involved in disposal by customers or field offices. If the CRT is returned to Colorado Springs for disposal and no warranty claim is involved, write "Returned for Disposal Only" in item No. 5 on the form.

Do not use this form to accomplish CRT repairs. In order to have a CRT repaired, it must be accompanied by a customer service order (repair order) and the shipping container must be marked "Repair" on the exterior.

## SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements. This is a Safety Class 1 instrument.

## GROUND THE INSTRUMENT

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

## DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

## KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

## DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

## USE CAUTION WHEN EXPOSING OR HANDLING THE CRT

Breakage of the Cathode-ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the instrument. Handling of the CRT shall be done only by qualified maintenance personnel using approved safety mask and gloves.

## DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument. Return the instrument to a HewlettPackard Sales and Service Office for service and repair to ensure that safety features are maintained.

## DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

## WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

## SAFETY SYMBOLS

## General Definitions of Safety Symbols Used On Equipment or In Manuals.



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

4 Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked).


Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with this symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.


Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

WARNING


-     - 

$\sim$
DANGER

CAUTION\}
Alternating current (power line).
Direct current (power line).
Alternating or direct current (power line).
The DANGER sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like, which could result in injury or death to personnel even during normal operation.

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE: The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like, which is essential to highlight.

## SECTION I GENERAL INFORMATION

## 1-1. INTRODUCTION.

1-2. The Operating Manual contains information required to install, operate, and verify the instrument's operational capabilities.

1-3. The Service Manual contains the necessary information to test, adjust, and service the 3582A Spectrum Analyzer.

1-4. The part number of this manual is listed on the title page. Also listed on the title page is a Microfiche part number. This number can be used to order $4 \times 6$ inch microfilm transparencies of the manual. Each microfiche contains photo-duplicates of up to 96 manual pages. The microfiche package also includes the latest Manual Changes supplement as well as pertinent Service Notes.

### 1.5. SPECIFICATIONS.

1-6. Instrument specifications are listed in Table 1-5. These specifications are the performance standards against which the instrument is tested.

### 1.7. SAFETY CONSIDERATIONS.

$1-8$. This product is a Safety Class 1 instrument (provided with a 3 -wire cord). The instrument and manual should be reviewed for safety markings and instructions before operation.

## 1.9. ©instruction manual symbol.

1-10. Wherever the 3582 A instrument is marked with this symbol, the user should refer to the instruction manual in order to protect against damage to the instrument. This symbol is found primarily in the Service Manual.

## 1-11. INSTRUMENTS COVERED BY MANUAL.

1-12. Attached to the instrument is a serial number plate. The serial number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the serial prefix and the last five digits are the suffix. The prefix is the same for all identical instruments; it changes only when a change is made to the instrument. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with serial number prefix(es) listed under SERIAL NUMBERS on the title page.

1-13. An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a yellow Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

1-14. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual part number, which also appears on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-15. For information concerning a serial number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Sales and Service Office.

## 1-16. DESCRIPTION.

1-17. The -hp- Model 3582A is a dual-channel spectrum analyzer covering the frequency range of 0.02 Hz to 25.6 kHz . By combining advanced digital processing techniques and a powerful micro-computer, it can provide measurement capability previously found only in complicated computer systems.

1-18. The performance features of the instrument provide optimal solutions to the problems of low frequency spectrum analysis. Frequency spans from 1 Hz to 25 kHz full scale allow great flexibility in selecting the portion of the spectrum to be analyzed. The spans from 5 Hz up to 25 kHz can be positioned anywhere within the frequency range of the instrument to provide exceptionally good frequency resolution.

1-19. Without resorting to external signal conditioning, the instrument can measure input from +30 dBV ( 31.6 volts) down to -120 dBV ( 1 microvolt). Even with this high sensitivity, the input circuits are protected against overloads of up to 100 volts. For measurements where the signal of interest exists in the presence of large unwanted signals, the wide 70 dB dynamic range of the instrument is important.

1-20. These spectrum measurements are made with "real-time" speed for frequency spans less than 500 Hz . Here real-time means that processing time is less than data acquisition time so that no input data is "lost" while waiting for processing. Data acquisition time must be increased for narrower spans to provide the required resolution. For broader spans, data acquisition time is small and processing speed becomes the limiting factor.

1-21. The Model 3582A can also measure the phase of the various spectral components or transfer function. This makes it possible to fully characterize a signal and can provide new insight into the operation of complex electrical or mechanical devices.

1-22. The most significant additional measurement capabilities of the instrument result from having two input channels that operate simultaneously. Not only can independent input signals be examined for common characteristics, but also device input/output relationships can be evaluated. The instrument directly provides both amplitude and phase information of the transfer function of a device. A built-in pseudo-random noise or a built-in random "band limited white noise"' source can be used to drive the device under test to perform low frequency network analysis.

## NOTE

The random 'band limited white noise" source is not available on instruments with serial numbers prefixed 1747A.

1-23. Many signals cannot be analyzed with conventional spectrum analyzers because they are not stable. Digital signal processing techniques allow the Model 3582A to capture and analyze transient signals that last for only a few milliseconds.

1-24. In the Model 3582A, the large-screen CRT makes the measurement results avilable in a highly usable form. In addition to two simultaneous information traces, the display provides four lines of alphanumeric data giving measurement configuration and results. The alphanumeric marker makes it possible to read results directly in absolute or relative units. In addition to measurement results, the CRT is also used to display operational diagnostic messages.

1-25. In order to provide maximum confidence in the operation of the instrument, self test routines have been built in. These tests, in conjunction with the internal calibration signal, make it possible to quickly verify the calibration of the instrument before beginning a critical measurement sequence.

1-26. Virtually all of the measurement functions of the Model 3582A are remotely programmable via the Hewlett-Packard Interface Bus (HP-IB). Since actual measurement data can be remotely input or output, it is possible with a computing controller to extend the basic measurement capability.

## 1-27. OPTIONS.

1-28. Table 1-1 lists the options which are available for the 3582A. These options may be ordered with the instrument or installed later.

Table 1-1. Options.

| 3582A Option | -hp- Part Mumber | Description |
| :---: | :---: | :--- |
| 001 | - | High Transfer Function Accuracy |
| 07 | $5061-0090$ | Front Handle Kit |
| 908 | $5061-0078$ | Rack Flange Kit |
| 909 | $6061-0084$ | Rack Flange and Handle Kit |
| 910 | $03582-90000$ | Extra Operating Manual |
| 910 | $03582-90001$ | Extra Service Manual |
| 009 | $03582-80009$ | Japanese Pullout Card |

## 1-29. ACCESSORIES SUPPLIED.

1-30. Table 1-2 lists the accessories supplied with the -hp- Model 3582A Spectrum Analyzer.
Table 1-2. Accessories Supplied.

| Item | Quantity | -hp. Part Number |
| :---: | :---: | :---: |
| Accessory Kit (includes the following): | 1 ea. | 03582-84401 |
| PC Board Extender | 1 ea. | 03582-66531 |
| PC Board Extender | 1 ea. | 03582-66532 |
| PC Board Extender | 1 ea. | 03582-66533 |
| Fuse . 25 amp 250 V Slow Blo | 1 ea. | $2110-0201$ |
| Fuse 1.5 amp 250 V Normal Blo | 2 ea. | $2110-0043$ |
| For use in the Familiarization Exercise: |  |  |
| Capacitor, 3000 pF 5\% 300 V | 1 ea. | 0160-2229 |
| Resistor, $10 \mathrm{k} \Omega 1 \% 1 / 4 \mathrm{~W}$ | 1 ea. | 0757-0442 |

### 1.31. ACCESSORIES AVAILABLE.

1-32. Table 1-3 indicates the accessories which are available for the -hp- 3582A. These accessories may be obtained through your -hp- Sales and Service Office.

Table 1-3. Accessories Available.

| Accessory | -hp- Model |
| :---: | :---: |
| 10:1 Voltage Divider Probe | 10001A |
| HP-IB Cables | 10631A 1 meter (3.3 feet) |
|  | 10631B 2 meters ( 6.6 feet) |
|  | 10631C 4 meters (13.2 feet) |
| Scope Camera | Model 197A Option 006 |
| Slide Rack Mount | Standard Slide Kit (-hp- Part No. 1497-0017) |
|  | Tilt Slide Kit (-hp- Part No. 1494-0020) |
| Test Leads | 11000A 112 cm ( 44 in ); dual banana both ends |
|  | 11001A $112 \mathrm{~cm}(44 \mathrm{in}$ ); dual banana to BNC |

## 1-33. RECIMMMENDED TEST EQUIPMENT.

1-34. Equipment required to maintain the Model 3582A is listed in Table 1-4. Other equipment may be substituted if it meets or exceeds the critical specifications listed in the table.

1-35. Note that the Performance Test is automatic and controlled via the Hewlett-Packard Interface Bus (HP-IB). Thus, the calculator and HP-IB compatability for the instruments is not strictly required. However, the full manual test will take about 10 times longer than the automatic test.

1-36. If manual testing must be done, it is recommended that only the Performance Test appropriate to a specific problem and/or repair be done, supplemented by the Operational Verification given at the end of Section III.

Table 1-4. Recommended Test Equipment.

| Instrument | Required Characteristics | hecommended Modelis) | Use* |
| :---: | :---: | :---: | :---: |
| Audio Oscillator | Harmonics, Hum and Noise <br> Down at least 86 dB <br> Freq. Range: $10 \mathrm{~Hz}-25 \mathrm{kHz}$ <br> Output Level: 10 dBV (3.16 Vrms) | -hp- 239A/339A <br> (See Note 1) | P |
| Bus Analyzer | Bus System Analyzer Meeting I.E.E.E. 488-1975 Standards | -hp- 59401 A | T |
| Calculator (Controller) | (See Note 2) | -hp-9825A (Option 002) | P |
| HP - IB Interface | (See Note 2) | -hp. 98034A | $p$ |
| Calculator ROM's | (See Note 2) | $\begin{aligned} & \text {-hp- } 98210 \mathrm{~A} \\ & \text {-hp- } 98211 \mathrm{~A} \\ & \text {-hp- } 98214 \mathrm{~A} \end{aligned}$ | P |
| Counter | 6 Digits <br> Frequency Range: $200 \mathrm{HZ}-200 \mathrm{kHz}$ <br> Sensitivity: 50 mV rms <br> Input Impedance: $1 \mathrm{M} \Omega,<50 \mathrm{pF}$ | -hp-5328A | T, A |

Table 1.4. Recommended Test Equipment (Cont'd).

| Digital Voltmeter | HP-IB Capability (see Note 3) <br> AC Function: <br> Frequency Range: 200 HZ - 100 kHz <br> Accuracy: $\pm(0.1 \%$ of RDNG $+0.025 \%$ of range) <br> DC Function: <br> Accuracy: $\pm(0.005 \%$ of RDNG $+0.001 \%$ of range $)$, | -hp-3455A | P, T |
| :---: | :---: | :---: | :---: |
| High Voltage Probe | 1000:1 Division <br> $1 \%$ Accuracy at 4 kV | -hp- 3440A-K05 | A, T |
| Logic Probe | TTL Compatible | -hp-10525A | T |
| Oscilloscope | 50 MHz ; range down to $5 \mathrm{mV} / \mathrm{Div}$ | $\begin{gathered} \text { hp- 1740A } \\ \text {-hp- } 10007 \mathrm{~A} \text { Probe } \end{gathered}$ | T, A |
|  |  | -hp-10004-67605 Spanner Tip |  |
| Signature Analyzer |  | -hp-5004A | T |
| Synthesizer: | HP-IB Capability (see Note 3) | -hp- 3330B <br> (Option 005) | P,T,A |
|  | Frequency Range: 0.02 Hz to 100 Hz <br> Amplitude Range: -80 dBm to $+13 \mathrm{dBm}(50 \mathrm{ohms})$ Amplitude Accuracy: $\pm 0.2 \mathrm{~dB}$ at 10 kHz and -70 dBm | -hp- 3325A <br> (Option 002) |  |
| $50 \Omega$ Termination | $50 \pm 0.1$ ohm; Feedthru | -hp- 11048C | P, T, A, |
| Function Generator | Square and Triangle Outputs | $\begin{aligned} & -h p-3310 A \\ & -h p-3311 A \\ & -h p-3312 A \\ & -h p-3325 A \end{aligned}$ | P |
| Load Resistor | 2.5n, 5\%, 10W | -hp-0811-2844 | A |
| Test Cartridge | Automatic Performance Test Software | -hp-03582-10002 | P |

NOTE 1: The 339A is a distortion measurement set with built-in low distortion oscillator. The oscillator alone is available as the 239A.

NOTE 2: Performance test software is written for the -hp-9825A Calculator and 9866B Printer. Use of a different printer will require program modification. The test can be run using the 9825A's Printer, but the printout will be pass/fail rather than the full explanation given with the 9866B.

NOTE 3: HP-IB capability required for automatic testing.

* $\mathbf{P}=$ Performance Test; $\mathbf{A}=$ Adjustments; $\mathbf{T}=$ Troubleshooting


## Table 1-5. Specifications

## FREQUENCY

## FRERUENCY MODES:

0.25 kHz Span: The selected measurement is performed over the fixed frequency range of 0 Hz to 25 kHz independent of the FREQUENCY SPAN control.

0-Start: The selected measurement is performed over the frequency range defined by the FREQUENCY SPAN control and with a fixed start frequency of OHz .

Set Center: The selected measurement is performed over a frequency range with a width determined by the FREQUENCY SPAN control and with a center frequency variable with 1 Hz resolution.

Set Start: The selected measurement is performed over a frequency range with a width determined by the FREQUENCY SPAN control and with a start frequency variable with 1 Hz resolution.

FREQUENCY RANGE: 0.02 Hz to 25.5 kHz . The low frequency limit is the result of the $D C$ response.

FREQUENCY SPANS:
0 Start Mode: 1 Hz full scale to 25 kHz full scale in a 1-2.5-5-10 sequence.

Table 1-5. Specifications (Cont'd).

Set Start Or Set Center Mode: 5 Hz span to 25 kHz span in a 1-2.5-5-10 sequence.

FREQUENCY ACCURACY: The frequency accuracy is $\pm 0.003 \%$ of the display center frequency.

FREQUENCY RESOLUTION: The marker resolution is equal to the calculated point spacing for the selected frequency span and number of channels.

FILTER PASSBAND SHAPE:

|  | Flat Tap | Hanning | Uniform |
| :---: | :---: | :---: | :---: |
| (dB Bandwidth: <br> (single-channel) | $(1.4 \pm 0.1) \%$ <br> of span | $10.58 \pm 0.05) \%$ <br> of span | $(0.35 \pm 0.02) \%$ <br> of span |
| Shape Factor: | $2.6 \pm .1$ | $9.1 \pm .2$ | $716 \pm 20$ |

$[60 \mathrm{~dB}$ bandwidth $]$
[3dB bandwidth]
The FLAT TOP PASSBAND SHAPE provides optimum amplitude accuracy. The UNIFORM PASSBAND SHAPE is optimized for use with transients and for use with the PERIODIC NOISE SOURCE, and the HANNING PASSBAND SHAPE provides an amplitude/frequency resolution compromise and is used for general noise measurements.

## Single-Channel Analysis Parameters:



The corresponding dual-channel parameters are found by doubling the calculated point spacing and equivalent noise bandwidths and taking one half the time record length.

## AMPI.ITUDE

AMPLITUDE MEASUREMENT MODES: 256 point amplitude spectra are measured in the single-channel mode. Two 128 point amplitude spectra are measured in the dualchannel mode.

## AMPLITUDE DISPLAY MODES:

Log: $10 \mathrm{~dB} /$ major division
$2 \mathrm{~dB} /$ major division
Linear: Constant voltage/major division

## AMPLITUDE MEASUREMENT RANGE:

Log: The calibrated attenuator range is +30 dBV to -50 dBV single tone RMS maximum input level in 10 dB $\pm 0.2 \mathrm{~dB}$ steps. The continuous vernier provides $>10$ dB of additional uncalibrated sensitivity between the 10 dB steps.

Linear: The calibrated attenuator range is +30 volts RMS to 3 millivolts single tone RMS maximum input in a 1-3-10 sequence. The vernier provides continuous coverage between the major steps. The AMPLITUDE

REFERENCE LEVEL provides 8 additional ranges down to 8 microvolts full scale.

DYAMIC RANGE:

Distortion Products: $>70 \mathrm{~dB}$ below the maximum input level.

Spurious Respanses: $>70 \mathrm{~dB}$ below the maximum input level.

## Noise:



DC Response: Adjustable to $>40 \mathrm{~dB}$ below the maximum input level with the front panel DC balance adjustment.

Table 1-5. Specifications (Cont'd).

## AMPI.ITUDE (Cont'd)

## AMPLITUDE ACCURACY:

|  | Log |
| :---: | :---: |
| Accuracy At The <br> Passband Centar: <br> [Full Scale) | $\pm 0.5 \mathrm{~dB}$ |
| Flat Top Filter: Hanning Filter: Uniform Filter: | $\begin{aligned} & +0,-0.1 \mathrm{~dB} \\ & +0,-1.5 \mathrm{~dB} \\ & +0,-4.0 \mathrm{~dB} \end{aligned}$ |

Overall accuracy is the sum of the accuracy at the passband center and the filter accuracy.

## AMPLITUDE RESOLUTION:

Log: 0.1 dB with the marker
Linear: 3 digits with the marker

## AMPLITUDE LINEARITY:

$\pm 0.2 \mathrm{~dB} \pm 0.02 \%$ of full scale
AMPLITUDE CALIBRATOR: The internal calibration signal is a line spectrum with nominal 1 kHz frequency spacing and a fundamental level of $22 \pm 0.2 \mathrm{dBV}$ on the log scales and $20 \pm 0.5$ volts on the linear scale.

## AMPLITUDE OVERLOAD LIMITS:

Log: Overload occurs at $100 \%$ of the maximum input level which is equal to full scale when the AMPLITUDE REFERENCE LEVEL is set to NORMAL. When overload occurs spurious products may be displayed.

Linear: Overload occurs at $100 \%$ of the maximum input level which, depending on the input attenuator setting, is at $6 / 8$ or $5 / 8$ of full scale when the AMPLITUDE REFERENCE LEVEL is set to NORMAL. When overload occurs spurious products may be displayed.
PHASE

PHASE MEASUREMENT MODES: 256 point phase spectra are measured in the single-channel mode. Two 128 point phase spectra are measured in the dual channel mode.

PHASE DISPLAY RANGE: From 200 degrees to -200 degrees.

PHASE ACCURACY: $\pm 10$ degrees

PHASE RESOLUTION:

Display: 50 degrees/major division
Marker: 1 degree

## TRANSFER FUNCTION

TRANSFER FUNCTION MEASUREMENT MODES: Dual-channel 128-point transfer functions are measured.

## TRANSFER FUNCTION DISPLAY MODES:

Log Amplitude: $10 \mathrm{~dB} /$ major division
$2 \mathrm{~dB} /$ major division
Linear Amplitude: Constant floating point fraction/major division

Phase: Constant 50 degrees/major division
transfer function measurement range:

Log Amplitude: Calibrated ranges of +160 dB full scale to -80 dB full scale in 10 dB steps. The uncalibrated verniers provide continuous coverage between the 10 dB steps.
Linear Amplitudg: Calibrated ranges of $4.0 \times 10^{8}$ full scale to $4.0 \times 10^{-8}$ full scale in factor of 10 steps. The un-
calibrated verniers provide continuous coverage between the factor of 10 steps.
Phase Display Range: +200 degrees to -200 degrees.
TRANSFER FUNCTION ACCURACY ISTANDARD):
Amplitude: $\pm 0.8 \mathrm{~dB}$
Phase: $\pm 5$ degrees
TRANSFER FUNCTION ACCURACY (OPTIDN 001):

| .02 Hz |  | 5 kHz | 25.5 kHz |  |
| :--- | :---: | :---: | :---: | :---: |
| Amplitude: | .4 dB | $\pm .8 \mathrm{~dB}$ |  |  |
| Phase: | $\pm 2^{\circ}$ | $\pm 5^{\circ}$ |  |  |

TRANSFER FUNCTION RESOLUTION:
Log Amplitude: 0.1 dB with the marker
Linear Amplitude: 3 digit scientific notation with the marker

Phase: 1 degree with the marker

## COHERENCE FUNCTION

COHERENCE FUNCIION MEASUREMENT MODE: Dual-channel 128 point coherence functions are measured with RMS averaging only.

COHERENCE MEASUREMENT RANGE: The bottom display line is 0.0 and the top display line is 1.0 .

COHERENCE FUNCTION RESOLUTIION:
Display: $0.125 /$ major division
Marker: 0.01

Table 1-5. Specifications (Cont'd).

## TRIGGER

## TRIGGER MODES:

Free Run: A new measurement is initiated by the completion of the previous measurement.

External: A rear panel switch allows new measurements to be initiated by an external TTL pulse.

Input Signal: A new measurement is initiated when the input signal meets the specified trigger condition.

## TRIGGER CONDITIONS:

Signal Conditions: Triggering can be selected to occur on a positive or negative going transition through the trigger level. The trigger level is adjusted between the time record overload limits by a continuous vernier.

Single/Multiple Triggers: Single-shot triggering is specified by taking the instrument out of the REPETITIVE mode. The ARM control sensitizes the instrument to take another measurement in the non-repetitive mode.

## INPUT CHANNELS

INPUT IMPEDANCE: $10^{6} \Omega \pm 5 \%$ shunted by $<60$ pf from input high to low for less than $75 \%$ relative humidity.

DC ISOLATION: Input low may be connected to chassis ground or floated up to 30 volts to reduce the effects of ground loops on the measurement.

INPUT COUPLING: The input circuit may be AC or DC coupled. The low frequency 3 dB roll off of the AC coupling is $<1 \mathrm{~Hz}$.

## COMMON MODE REJECTION:

$50 \mathrm{~Hz}:>60 \mathrm{~dB}$
$60 \mathrm{~Hz}:>58 \mathrm{~dB}$
INPUT CHANNEL CROSSTALK: $<-140 \mathrm{~dB}$ between channels with $1 \mathrm{k} \Omega$ source impedance driving one channel and the other channel terminated in $1 \mathrm{k} \Omega$.

## OUTPUT SIGNALS

## X-Y RECORDER:

Vertical: 0 to $5.25 \mathrm{~V} \pm 5 \%$
Horizontal: 0 to $5.25 \mathrm{~V} \pm 5 \%$

Impedance: $1 \mathrm{k} \Omega$
Pen Lift: Contact closure during sweep.

## NDISE SOURCE:

Periodic: Pseudorandom noise signal with spectral line spacings that match the calculated point spacing for the selected frequency span. The noise spectrum is band limited and band translated to match the selected measurement.

Random: Random noise signal; the noise spectrum is band limited and band translated to match the selected measurement.

Level: Vernier control from $<10 \mathrm{mV}$ to $>500 \mathrm{mV}$ RMS into a load of $\geq 50 \Omega$ when measured with a broadband True RMS voltmeter.

Periodic Noise Frequency Response: $\pm 1 \mathrm{~dB}$ with UNIFORM PASSBAND SHAPE and -10 dBV level.

Impedance: $<2 \Omega$
IMPULSE SOURCE: A TTL low to high pulse with a period equal to the time record length.

## DISPLAY

CRT:

Screen Size: $11.9 \mathrm{~cm}(4.7 \mathrm{in}$.) wide by $9.6 \mathrm{~cm}(3.8 \mathrm{in})$. high.

Graticule: 10 major division horiztonal by 8 major divisions vertical with internal illumination for CRT photography.

Text: Maximum of four 32 character lines of alphanumeric text.

ALPHANUMERIC ANNOTATION: Single or dual-channel configuration, input or stored trace, frequency calibration, amplitude calibration, equivalent noise bandwidth,
relative or absolute marker frequency, relative or $a b$ solute marker phase, relative or absolute marker coherence, RMS noise density at the marker, time record collection time.

DISPLAY A'CCURACY: Display accuracy is $3 \%$ of total height or width for $25 \pm 15^{\circ} \mathrm{C}$. Note that if numeric readings are taken visually from the displayed trace, this factor must be added to the basic accuracy specification.

TRACE STORAGE: A maximum of two independent traces may be digitally stored and recalled. Annotation information is not stored with the traces.

Table 1-5. Specifications (Cont'd).

## AVERAGE

## AVERAGING MODES:

RMS: For each calculated frequency point the displayed amplitude is

$$
\sqrt{\frac{1}{N} \sum_{i}^{N} A_{i}^{2}(f)} \quad \text { and the phase is } \frac{1}{N} \sum_{i}^{N} \theta_{i}(f)
$$

Peak: For each calculated frequency point the displayed amplitude is MAX Ai(f) and the phase is the corresponding value for the retained amplitude point.

Time: For each time record point the amplitude is

$$
\frac{1}{N} \sum_{i} A i(t)
$$

The averaged time record is transformed to give the corresponding amplitude and phase.

NUMBER OF AVERAGES: 4 to 256 in a binary sequence plus exponential. Exponential in the RMS mode gives a running average with new spectral data weighted $1 / 4$ and the previous result by $3 / 4$. Exponential in the peak mode gives a continuous peak hold operation.

## REMOTE OPERATION

PROGRAMMING: All analyzer front panel controls except the CRT controls, NOISE SOURCE LEVEL and TYPE, TRIGGER LEVEL, AMPLITUDE VERNIERS, and GROUND ISOLATION are remotely programmable via the HP-IB.

DATA INPUT: Time records, amplitude and phase spectra, coherence functions, transfer functions and
alphanumeric text can be input to the analyzer via the HP-IB.

DATA OUTPUT: Time records, amplitude and phase spectra, coherence functions, transfer functions, alphanumeric text, marker values and control settings can be output via the HP-IB.

## GENERAL

## environmental:

Operating Temperature: $0^{\circ} \mathrm{C}$ to $+55^{\circ} \mathrm{C}$.
Mon-operating Temperature: $-40^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$.
Humidity: To $95 \%$ relative humidity at $40^{\circ} \mathrm{C}$.
Operating Altitude: 4600 Meters (15,000 feet).
Non-operating Altitude: 6300 Meters (25,000 feet).
Shock: $30 \mathrm{G}, 11 \mathrm{msec}$ half sine wave on each of six sides.

Vibration: 10 Hz to 55 Hz at 0.010 inch peak-to-peak excursion.

OPERATING POWER: Switch selection of $110 \mathrm{~V}+5,-10 \%$ or $230 \mathrm{~V}+5,-10 \% 48-66 \mathrm{~Hz}$; less than 150 VA .

## PHYSICAL PARAMETERS:

Size: 425.5 mm (16.75 inches) wide 552.5 mm (21.75 inches) deep 188 mm ( 7.4 inches) high

Net Weight: $24.5 \mathrm{~kg}(54 \mathrm{lbs}).$.
Shipping Weight: $29 \mathrm{~kg}(63 \mathrm{lbs}$.$) .$

## SECTION II

## INSTALLATION

## 2-1. INTRODUCTION.

2-2. This section contains instructions for installing and interfacing the Model 3582A Spectrum Analyzer. Included are initial inspection procedures, power and grounding requirements, environmental requirements, installation instructions, interfacing procedures and instructions for repacking and shipment.

## 2-3. INITIAL INSPECTION.

2-4. This instrument was carefully inspected both mechanically and electrically before shipment. It should be free of mars or scratches and in perfect electrical order upon receipt. To confirm this, the instrument should be inspected for physical damage incurred in transit. If the instrument was damaged in transit, file a claim with the carrier. Check for supplied accessories (listed in Section I) and test the electrical performance using the Operational Verification given in Section IV Part I. If there is damage or deficiency, see the warranty in the front of this manual.

## 2-5. POWER REOUIREMENTS.

2-6. The Model 3582A can be operated from any power source supplying $100 \mathrm{~V}, 120 \mathrm{~V}, 220 \mathrm{~V}$ or $240 \mathrm{~V}(-10 \%$ to $+5 \%), 48 \mathrm{~Hz}$ to 66 Hz single phase. Power consumption is less than 150 VA.

### 2.7. Line Voltage And Fuse Selection.

2-8. Figure 2-1 gives information for line voltage and fuse selection. The voltage and proper fuse have been factory selected for 120 V ac operation.


Figure 2-1. Line Voltage And Fuse Selection.

## 2-9. Power Cable And Grounding Requirements.

2-10. To protect operating personnel, the National Electrical Manufacturer's Association (NEMA) recommends that the instrument panel and cabinet be grounded. The Model 3582A is equipped with a three-conductor power cord which, when plugged into an appropriate receptacle, grounds the instrument cabinet. The type of power cable plug shipped with each instrument depends on the country of destination. Refer to Figure 2-2 for the part number of the power cable and plug configurations available.


Figure 2-2. Power Cables.

## 2-11. OPERATING ENVIRONMENT.

## 2-12. Temperature.

2-13. The instrument may be operated in temperatures from $0^{\circ} \mathrm{C}$ to $+55^{\circ} \mathrm{C}$.

## 2-14. Humidity.

2-15. The instrument may be operated in environments with humidity up to $95 \%$. However, the instrument should be protected from temperature extremes which cause condensation within the instrument.

## 2-16. Altitude.

2-17. The instrument may be operated at altitudes up to 4600 meters ( 15,000 feet).

## 2-18. Cooling Fan.

2-19. The 3582A is equipped with a cooling fan mounted on the rear panel. The instrument should be mounted so that air can freely circulate through it. The filter for the cooling fan should be removed and cleaned every 30 days by flushing with soapy water.

## 2-20. Thermal Cutout.

2-21. The 3582 A is equipped with a thermal cutout switch which automatically removes line voltage whenever the internal temperature becomes excessive. The temperature at which this will occur is dependent upon line voltage and airflow but with proper airflow will not occur in less than a $55^{\circ} \mathrm{C}$ ambient at high line. The switch resets automatically when the instrument cools. If a thermal cutout occurs, check for fan stoppage, clogged fan parts and other conditions that could obstruct airflow or otherwise cause excessive heating.

## NOTE

The thermal cutout will operate at any external temperature down to $+15^{\circ} \mathrm{C}$ if the airflow is blocked.

## 2-22. INSTALLATION.

## 2-23. Mounting.

2-24. The 3582 A is shipped with plastic feet and tilt stand in place, ready for use as a bench instrument. the plastic feet are shaped so that the 3582A may be mounted on top of other -hp- equipment. Plastic feet mounted on the rear panel enable the 3582A to be placed in a vertical position if desired. When operating the instrument, choose a location that provides at least three inches of clearance at the rear and at least one inch for each side. Failure to provide adequate air clearance will result in excessive internal temperature, reducing instrument reliability. The clearances provided by the plastic feet in bench stacking and the filler strip in rack mounting allow air passage across the top and bottom cabinet surfaces.

2-25. Option 908 (Rack Mount Kit) enables the 3582 A to be mounted in an equipment cabinet. The rack mount for the 3582A is an EIA standard width of 19 inches. Installation instructions are included with the Rack Mount Kit. Option 908 may be ordered from the nearest -hp- Sales and Service Office under -hp- part number 5061-0078.

## 2-26. HP.IB SYSTEM INTERFACE CONNECTIONS.

2-27. The Model 3582A instrument is compatible with the Hewlett-Packard Interface Bus (HP-IB).

## NOTE

The HP-IB is Hewlett-Packard implementation of IEEE std. 488-1975, 'Standard Digital Interface for Programmable Instrumentation'.

2-28. The instrument is connected to the HP-IB by connecting an HP-IB interface cable to the connector located on the rear panel. Figure 2-3 illustrates a typical HP-IB System interconnection.


Figure 2-3. Typical HP-IB System Interconnection.

2-29. With the HP-IB system, you can interconnect up to 15 HP-IB compatible instruments. The -hp- 10631 HP-IB cables have identical "piggy-back" connectors on both ends so that several cables can be connected to a single source without special adapters or switch boxes. You can interconnect system components and devices in virtually any configuration you desire. There must, of course, be a path from the calculator (or other controller) to every device operating on the bus. As a practical matter, avoid stacking more than three or four cables on any one connector. If the stack gets too long, any force on the stack produces great leverage which can damage the connector mounting. Be sure that each connector is firmly screwed in place to keep it from working loose during use. The 3582A uses all the available HP-IB lines, therefore, any damaged connector pins may adversely affect HP-IB operation (see Figure 2-4).


Figure 2-4. HP-IB Connector.

### 2.30. Cable Length Restrictions.

2-31. To achieve design performance with the HP-IB, proper voltage levels and timing relationships must be maintained. If the system cable is too long, the lines cannot be driven properly and the system will fail to perform (see Table 2-1 for HP-IB cable lengths). Therefore, when interconnecting an HP-IB system, it is important to observe the following rules:
a. The total cable length for the system must be less than or equal to 20 meters ( 65 feet).
b. The total cable length for the system must be less than or equal to 2 meters ( 6 feet) times the total number of devices connected to the bus.

## Table 2.1. HP-IB Cables With Metric Fasteners.

| HP.IB Cable | Length |
| :---: | :---: |
| 10631 A | 1 m |
| 10631 B | 2 m |
| 10631 C | 4 m |
| 10631 D | .5 m |

## 2-32. HP-IB Address Selection.

2-33. The 'talk" and "listen'' addresses for the instrument are selected by the Instrument Bus Address switch. This switch is the seven section "DIP"' switch located on the A2 HP-IB board under the front right card nest cover in the instrument. the five switches labeled 1 through 5 are used to select the unique talk and listen address. The HP-IB Address is set at the factory to 11 (listen address + and talk address K ). You can leave the instrument at this address or change it to any of the alternatives in Table 2-2.

## WARNING

Access to the HP-IB Address switch requires removal of the instrument top cover, exposing potentially lethal voltages. To avoid electrical shock, do not attempt to check or change the switch setting unless you are properly service trained.

### 2.34. STORAGE AND SHIPMENT.

### 2.35. Environment.

2-36. The instrument may be stored or shipped in environments within the following limits:

> Temperature. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $-40^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$
> Humidity. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . Up to $95 \%$
> Altitude. . . . . . . . . . . . . . . . . . . . . Up to 7,630 meters ( 25,000 feet)

The instrument should also be protected from temperature extremes which cause condensation within the instrument.

### 2.37. Packaging.

2-38. Original Packaging. Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Also, mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

Table 2-2. Address Selection.

| ASCII Code Character |  | Address Switches |  |  |  |  | 5-bit Decimal Code |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Listen | Talk | A5 | A4 | A3 | A2 | A1 |  |  |
| SP | @ | 0 | 0 | 0 | 0 | 0 | 00 |  |
| ! | A | 0 | 0 | 0 | 0 | 1 | 01 |  |
| . | B | 0 | 0 | 0 | 1 | 0 | 02 |  |
| \# | C | 0 | 0 | 0 |  | 1 | 03 |  |
| \$ | D | 0 | 0 | 1 | 0 | 0 | 04 |  |
| \% | E | 0 | 0 | 1 | 0 | 1 | 05 | NOT USED |
| 8 | F | 0 | 0 | 1 | 1 | 0 | 06 | $1$ |
| , | G | 0 | 0 | 1 |  | 1 | 07 |  |
| 1 | H | 0 | 1 | 0 | 0 | 0 | 08 | $1$ |
| 1 | 1 | 0 | 1 | 0 |  | 1 | 09 | INSTRUMENT SERVICE |
| * | $J$ | 0 | 1 | 0 | 1 | 0 | 10 | ADDRESS |
| + | K | 0 | 1 | 0 1 |  | 1 | 11 12 |  |
| - | $\stackrel{L}{M}$ | 0 0 | 1 |  |  | 0 1 | 12 |  |
| - | N | 0 | 1 | 1 | 1 | 0 | 14 | $\square \square \square \square$ |
| $i$ | 0 | 0 | 1 | 1 | 1 | 1 | 15 | M W M $\quad \square$ |
| 0 | P | 1 | 0 | 0 | 0 | 0 | 16 | - - - $\square_{3}$ |
| 1 | Q | 1 | 0 | 0 | 0 | 1 | 17 | $\begin{array}{lllllll}1 & 2 & 3 & 4 & 5 & 6 & 7\end{array}$ |
| 2 | R | 1 | 0 | 0 | 1 | 0 | 18 |  |
| 3 | S | 1 | 0 | 0 | 1 | 1 | 19 | - |
| 4 | T | 1 | 0 | 1 | 0 | 0 | 20 |  |
| 5 | U | 1 | 0 | 1 | 0 | 1 | 21 |  |
| 6 | $\checkmark$ | 1 | 0 | 1 | 1 | 0 | 22 |  |
| 7 | w | 1 | 0 | 1 | 1 | 1 | 23 |  |
| 8 | $X$ | 1 | 1 | 0 | 0 | 0 | 24 | OPOSITION (DOWN) |
| 9 | Y | 1 | 1 | 0 | 0 | 1 | 25 |  |
| : | Z | 1 | 1 | 0 | 1 | 0 | 26 |  |
| ; | [ | 1 | 1 | 0 | 1 | 1 | 27 |  |
| $<$ | 1 | 1 | 1 | 1 |  | 0 | 28 |  |
| $=$ | 1 | 1 | 1 | 1 |  | 1 | 29 |  |
| > | $\sim$ | 1 | 1 | 1 | 1 | 0 | 30 |  |

2-39. Other Packaging. The following general instructions should be used for repacking with commercially available materials:
a. Wrap the instrument in heavy paper or plastic. (If shipping to a Hewlett-Packard office or service center, attach a tag indicating the type of service required, the return address, the model number, and the full serial number.)
b. Use a strong shipping container. A double-wall carton made of 350 -pound test material is adequate.
c. Use a layer of shock-absorbing material 70 to 100 mm ( 3 to 4 inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside of the container. Protect the control panel with cardboard.
d. Seal shipping container securely.
e. Mark shipping container FRAGILE to ensure careful handling.
f. In any correspondence, refer to the instrument by model number and full serial number.

## WARNING

The Model 3582A is not intended for outdoor use. Do not expose it to rain or other excessive moisture.

# SECTION III <br> OPERATING REFERENCE 

## 3-1. INTRODUCTION.

3-2. This section contains a brief collection of data, which concerns both manual and remote operation. Also covered is a fundamental theory of operation and some application information.

## 3-3. USING SECTION III.

3-4. For quick reference to operating subject matter, refer to the Table of Contents below.
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## I. Introduction



What are these things and how are they related?
The answer to this question is hinted at by the graphic. All three are spectrum analyzers-but not all spectrum analyzers are real time analyzers. Each is a more specific description as you will see.

## Swept Analyzer

The most common technique for implementing a spectrum analyzer is the swept IF technique. The HP Model 3580A is an example of a product that uses this technique.


Conceptually, this technique can be viewed as moving a single filter over the frequency range of interest as follows.


This approach has some disadvantages-particularly at low frequencies. The most noticeable is that it is quite slow for narrow resolution bandwidths. This is a fundamental limitation of the technique and not the result of a particular implementation.

In order to get around this limitation, several types of "real time" analyzers have been developed. From a conceptual point of view, the parallel bank of filters is the simplest to understand.


Here, rather than a single filter that has to traverse the frequency span of interest, the filters are fixed and just have to be examined. Clearly, this is substantially faster than the swept technique. Because of the large number of filters, it is also more expensive.

The Fast Fourier Transform or FFT gets around this problem by effectively implementing the parallel filters digitally.


As a result of this computation process, the FFT can also provide phase information and some other advantages-but basically it is a means of performing spectrum analysis.

## II. Instrument Control Details

The front panel of the HP Model 3582A is logically divided into groupings of controls that have related functions. This chapter is intended to provide a good working knowledge of how these controls are used in making typical measurements. Chapter VI
further illustrates this with step-by-step checklists for the further illustrates this with step-by-step checklists for the more common measurement sequences.


HP.IB• STATUS SECTION: HP-IB is standard and provides full remote programming and
flexible data input and output.
X.Y RECORDER SECTION Front panel contr SECTION Front panel controls facilitate
the interface with analog $X-Y$ recorders. SECTION: Two inde pendent display traces an be digitally stored

PASSBAND SHAPE shapes are Passband filter shapes are optimized for various
situations and can be changed situations and can be changed
without having to redo a measwithout having to redo a mea
urement unless averaging has
been selected both channels or the transfer
function can be displayed function can be displayed. The
sampled time waveform and a sampled time waveform and
measurement called the coherence function can also be displayed.

FREQUENCY SECTION: 0 Start spans down to 1 Hz full scale and set center or set star
spans down to 5 Hz full scale spans down to 5 Hz full scal
can be selected. In the set center selected. Int the set
center or set start mode the RPG knob tunes the start or center display frequency



NOISE SOURCE SECTION: NOISE SOUR
source serves as the "real-time" equivalent of a conventional
tracking generator. equivalent of a con
tracking generator.


TRIGGER SECTION: Multiple or single shot triggering of a or single shot triggering of a
measurement can be initiated by an input signal on Channel

INPUT SECTION: Two independent input signals can be measured separately or simultaneously. The input circuits can be AC or DC coupled and


## A. Input Section

The INPUT section serves two major functions. First, it contains the controls that define which input channel or channels are to be active. Second, it contains the input sensitivity controls for both input channels.

The INPUT MODE slide switch defines which of the input channels is sampled. For maximum resolution, it should be set to either A or B . When set to BOTH the number of samples from each channel is cut from 1024 to 512 . Normally BOTH is used only for transfer function or coherence measurements.

The SENSITIVITY knob selects the maximum input signal level that can be applied to the instrument without overloading. When the signal level is not known, the appropriate input sensitivity is obtained by down-ranging until the LED comes on and then backing off one position. Overloads in the Model 3582A are somewhat unusual and are discussed in Section VI.

The difference between the reference level and the overload point in the linear mode is important and is also discussed in Section VI. When set to the CAL position, an internally generated calibration signal is connected to the measurement path. The signal has a spectral line every 1 kHz and an amplitude of 22 dBV (20V) as shown:


As long as the sensitivity VERNIER is in the CAL position, the measurement results will be calibrated and can be read in voltage or dBV ( 1 volt $\mathrm{rms}=0 \mathrm{dBV}$ ). The sensitivity VERNIER provides an additional 11 dB of attenuation for continuous coverage between the major 10 dB steps. When not in the CAL positions, the alphanumeric text indicates that display and marker results are uncalibrated. When not in the CAL position, only relative marker operations are valid. Note that this control is not programmable.

The ISOL/CHAS switch determines whether the input circuit is "floating" or single-ended. Normally this switch is set to ISOL. In this mode, a maximum of 30 volts can be applied between the: chassis ground and the input terminal.

The COUPLING switch selects AC ( ) or DC (--) coupling of the input circuit. When AC coupled a series capacitor removes DC signals and drifts from the input signal. For inputs with valid information at very low frequencies this is unacceptable; the coupling capacitor removes the signal information also. For these low frequency signals, DC coupling should be selected. DC coupling is used for signals with components of interest below about 10 Hz .

The actual inputs are GR type connectors and have $10^{6} \Omega$ in parallel with nominally 60 pf . This makes it possible to use 10:1 divider probes such as the HP Model 10001A. The noise source and transfer function amplitude display is a great way to accomplish probe compensation.


## B. Frequency Section

The FREQUENCY section controls what portion of the frequency range is analyzed. As shown, there are four major operational modes. Normally, the $0-25 \mathrm{kHz}$ span mode is used as an initial quick look. In this mode, the analysis is independent of the other frequency controls. In the 0 start mode, only the span control is active. It defines the stop frequency with the start frequency fixed at 0 Hz . There are 14 of these baseband spans from 1 Hz full scale, to 25 kHz full scale.

The set start and set center spans are used to achieve significant improvements in resolution by selecting only portions of the. spectrum for analysis. All 256 resolution elements can be located in a frequency span of 5 Hz to 25 kHz . The location of the analysis band can be set in two ways. The most common way is to use the SET FREQ marker feature. The intensified dot marker frequency becomes the new start or center frequency depending on the selected mode. The second way is to use the ADJUST knob. This control directly tunes either the start or center frequency depending on the selected mode. The tuned
frequency is displayed alphanumerically in the lower left corner of the display and is updated as it is tuned. The tuning knob is an endless turns knob with three tuning rates depending on how rapidly it is turned. Note that tuning is locked out when the instrument is in an averaging sequence to prevent the collection of invalid data.


## C. Display Section

The DISPLAY section defines what measured data is to be displayed and what display format is to be used. Three amplitude functions, three phase functions, and coherence are available as latching display buttons. A maximum of two traces from this group or the stored trace group can be selected simultaneously.

The Amplitude Controls select one or more amplitude displays. These buttons must agree with the INPUT MODE switch or a diagnostic (see section VI) is generated.

The Phase Controls select one or more phase displays. As with the amplitude displays these buttons must agree with the INPUT MODE switch or you get the same diagnostic. The scale on these displays is fixed at 50 degrees/division with foldover at $\pm 200$ degrees. Interpretation and use of the single channel phase display is covered in Section IV.

The XFR FCTN buttons select the display of the magnitude and/or phase of the transfer function. The magnitude is given in dB or as a floating point ratio if the linear display is selected.

The Scale Controls define the display as 80 dB or 16 dB high in log modes or as voltage in the linear mode. The difference between the reference level and the overload level in the linear mode is important and is discussed in Section VI.

The AMPLITUDE REFERENCE LEVEL switch in conjunction with the SENSITIVITY controls set the full scale sensitivity. In the $\log$ display modes, each step offsets the display by 10 dB without changing the maximum input level. In the linear mode, the full scale sensitivity is modified in a 40-16-8-4 sequence.

In all cases this is just an arithmetic scaling operation and does not affect the input level that will cause overloading. Also, since its a 16 bit arithmetic operation, it does not contribute to the accuracy specification like an IF attenuator would. The most common uses for this control are:

1. To properly scale a transfer function amplitude display.
2. To examine signals below $10 \%$ of full scale in the linear mode.

The COHER control selects the display of the coherence function. The most common use of this display is as a check on the validity of a transfer function measurement. The coherence function is a measure of the proportion of the power in the outputsignal caused by the input signal. A coherence value of 1.0 would indicate that the cause/effect relationship is ideal-and the transfer function ratio at that frequency is valid. It is only valid in the dual-channel mode with RMS averaging selected. Any other configuration results in a diagnostic (see section VI). The scale is a fixed 0.0 to 1.0 percentage scale. Application Note 245-2 titled "Measuring the Coherence Function with the HP 3582A. Spectrum Analyzer" treats this particular measurement in detail.

The TIME display buttons supersede the other display controls. Only one time display can be selected at a time and all other displays are suspended. The time display is active only as long as the pushbutton is held in.

The Model 3582A is not a digital time domain oscilloscope. In the baseband mode the display is composed of every other time. sample (The display circuitry can take only 512 points.) of the input. For input signals well below the span width, the reproduction can be pretty good-but for frequencies near the. span width, the reproduction is very poor. When in the band analysis mode, the display consists of the "real" points after filtering. These "real" points for a single tone will appear as the difference frequency between the input tone and the band analysis local oscillator.


## D. Trigger Section

The TRIGGER section defines the conditions under which a new block of data is collected and analyzed. The most common mode is with the REPETITIVE button in and the LEVEL set to FREE RUN. Under these conditions, the new block of data is collected when the previous measurement is completed.

When the LEVEL control is not in the detented position, it: specifies a trigger level in the time domain. When viewing the TIME display, the control will vary the trigger level over the entire non-overloaded input range. The vertical position is nominally about a zero level.

The SLOPE button defines whether the trigger is to occur on a positive or negative slope transition through the selected level.

The ARM control is used in conjunction with the REPETITIVE button to define single shot trigger mode. The ARM button sensitizes the trigger path to initiate data collection the next time all other trigger conditions are satisfied. Unless re-ARMed no subsequent trigger conditions will be recognized. When the trigger circuit is sensitized, the ARM light is on.

The DATA LOADING light indicates when data collection is taking place and stays on during the collection process. When this light is not flashing, the instrument is not collecting new data-and may appear to be "hung up." Checking the framed buttons will indicate the reason new data is not being collected.


## E. Passband Shape

The PASSBAND SHAPE controls determine the frequency domain filter shape or equivalently the time domain "window" function.

Each of the passband shapes represents a tradeoff between amplitude uncertainty and frequency resolution. The amplitude uncertainty problem is illustrated in the following figure.


As shown, the filter-to-filter spacing $\Delta f$ is fixed by the sampling rate. As the actual spectral line moves from $N \Delta f$ to $(N+1) \Delta f$ it traces out the top of the passband as shown. The uncertainty is maximum when the actual component falls midway between the filters. As the filter passband becomes flatter on top, the uncertainty is reduced-but so is the frequency resolution.

The FLAT TOP passband is optimized for minimum amplitude uncertainty and contributes less than 0.1 dB . The frequency resolution is correspondingly poorer than the other two filters. Normally this passband is used for measuring discrete spectral lines.

The HANNING passband is a traditional "window" found on most real time analyzers. It offers a compromise between the FLAT TOP and the UNIFORM shape. Its worst case uncertainty is 1.5 dB but it has a 3 dB bandwidth that is about $40 \%$ of that or the FLAT TOP filter. It is most commonly used for random noise measurements.

The UNIFORM passband is the result of using no time domain "window" weighting. It has a worst case amplitude uncertainty of 3.9 dB and a 3 dB bandwidth that is $60 \%$ of that of the HANNING window. It is used for transient measurements and whenever the built-in periodic noise source is used.


## F. Average Section

The AVERAGE controls are used to average the noise displayed on the CRT. Operationally it replaces the video filtering or display smoothing usually found on spectrum analyzers. The major advantages of digital averaging are repeatability, and predictability. The TIME average does offer a unique capability of actually enhancing the signal-tonoise ratio.

The RMS average mode combines a new spectrum with a partial result on a point-by-point basis using an RMS calculation. At any point in the cycle the amplitude at some frequency $A(f)$ is given as
$A(f)=\sqrt{1 / n\left[A_{1}{ }^{2}(f)+A 2^{2}(f)+\cdots+{A n^{2}}^{2}(f)\right]}$
The phase is $\phi(f)=1 / n\left[\phi_{1}(f)+\phi_{2}(f)+\quad+\phi_{n}(f)\right]$.
This averaging results in smoothing of the noise variations, but does not reduce the level of the noise. RMS averaging must be used when making coherence measurements.

The TIME average mode involves time domain averaging. When a synchronizing trigger is available successive time records are averaged point-by-point. Signal variations that are synchronous with the trigger will average to some value while noise that is not synchronous will average to zero. This eliminates the noise prior to the transformation to the frequency domain. Time averaging is unique in that it does result in an enhancement of the signal-to-noise ratio. It is also by far the fastest averaging mode and should probably be used any time a synchronizing trigger is available.

If you try to TIME average without a trigger you get a diagnostic (see Section VII).

The PEAK mode is not truly an averaging mode, but rather is the result of keeping the maximum value at each frequency point. The phase point retained is the phase of the retained point at each frequency. PEAK averaging is useful for measurements such as monitoring signal drift, etc.

The NUMBER of averages is selectable between 4 and 256 in a binary sequence. The SHIFT key selects whether the lower case black numbers or the upper case blue numbers are active.

The EXP mode is a continuous averaging process where the new input is weighted $1 / 4$ and the old previous average weighted $3 / 4$. This causes the most recent data to be most important while the older data dies out in importance at a decaying exponential rate. The exponential accumulation mode works only with RMS averages. It is most useful when the process under consideration exhibits relatively slow time variations and yet some averaging is still desired. The time constant of the exponential weighting is such that it averages
out short term variations, yet follows longer term variations. When EXP is selected in the PEAK mode, the instrument will accumulate PEAK data indefinitely.

In all of the averaging modes except exponential the instrument stops taking new data when the selected number of averages are completed. WHEN THIS OCCURS, THE 3582A MAY APPEAR TO BE "HUNG UP" WHEN ACTUALLY IT IS WAITING FOR FURTHER INSTRUCTIONS. This is the reason the AVERAGE OFF button is highlighted. Any time the 3582A appears to be stopped, this button should be checked. When the instrument has taken the selected number of averages the RESTART button is used to start the next averaging sequence. When the averaging mode is changed, a restart is automatically executed. When the number of averages is changed from one number to a larger number a restart is not required; the instrument continues from where it stopped to the new number of averages.

Note that RESTART actually clears the time record and restarts the measurement process even with the averaging turned off. This is probably the easiest way to restart any measurement if you don't like the time record being collected.

Application Note 245-1 titled "Signal Averaging with the HP 3582A Spectrum Analyzer" covers the topic of averaging in detail.


## G. Marker Section

The MARKER feature is one of the major conveniences of the instrument. When ON an intensified dot marker appears on one of the traces. The POSITION knob is used to move the dot marker either right or left on the trace. The amplitude and frequency information corresponding to the marker location is read out in alphanumeric form on the display.

As long as the REL button is out both readouts are in absolute units. To get relative measurements, the reference point is first located with the dot marker. Pushing the SET REF button saves the frequency and amplitude values of the marker as a reference. In subsequent measurements when the REL button is in the marker readout will be with respect to the selected reference. When the REL button is out the absolute readout is given.

When there are two active traces the TRACE button causes the dot marker to toggle between the two traces.

The $\div \sqrt{\mathrm{BW}}$ button is used for making measurements of random noise. Normally the level measured at any point with the analyzer is a function of the filter bandwidth and the actual noise density. Since different filter bandwidths will give different answers the comparison of results is difficult. In order to eliminate this problem, it is customary to normalize out the bandwidth factor by dividing the reading by the square root of the EQUIVALENT NOISE BANDWIDTH. This is the width of an ideal rectangular filter with the same response as the actual filter as shown.


The $\div \sqrt{\mathrm{BW}}$ button performs this normalization automatically and presents the results directly in $\mathrm{dBV} / \sqrt{\mathrm{Hz}}$ or voltage $/ \sqrt{\mathrm{Hz}}$.

The SET FREQ button is used to provide information to the band analysis modes of operation. When pressed, the current frequency of the intensified dot marker is stored to become the band analysis start or center frequency, depending on the frequency mode selected.

The marker frequency resolution on wide bandwidths may cause the display to be not exactly centered when changing modes. Repositioning the marker and doing SET FREQ again will refine the display because the marker resolution is better on narrower spans.


## H. Noise Source Section

The NOISE SOURCE is functionally the equivalent of a tracking generator on conventional spectrum analyzers. It is a driving source that stimulates a device under test across a measurement band. Since the 3582A is an FFT analyzer it can be viewed as conceptually measuring 256 parallel filters simultaneously. This is not compatible with a swept signal source.

The 3582A provides two broad band sources. The random noise signal requires extensive averaging to get valid results. The 3582A also has a periodic noise source synchronized to the data collection process. This source places a spectral line at each of the measurement points. More importantly, extensive averaging is not necessary; the variance of the periodic signal when it is analyzed is theoretically zero. The easiest way to get a feel for periodic noise is to simply measure the CAL signal. Rather than directly matching 256 spectral lines with 256 measurement points the calibrator matches 25 spectral lines or about one every tenth measurement points.

The BNC output is a very low (e.g., typically $1 \Omega$ ) impedance source. When measured with a high impedance voltmeter the LEVEL control will vary the output from nominally 0 V to 0.7 V mss in the 25 kHz span. The full scale position is detented. Note that this control is not programmable.

## III. Spectrum Analyzer Performance

There are a number of performance characteristics that are fundamental to a low frequency spectrum analyzer. This section discusses the most important of these characteristics and provides pertinent facts about each of them.

## A. Frequency Range



- Minimum baseband span of 1 Hz full scale.
- Resolution to within 20 milliHertz of DC.
- 14 baseband spans (1-2.5-5-10 sequence) for maximum flexibility.
- Filter bandwidth automatically tracks the selected span.

When thinking about the low end of the frequency range, there are several points to keep in mind.

1. As described in Section $V$ the length of time required to collect a time record is inversely related to the selected span. On the 1 Hz span, a single-channel time record is 250 seconds long. While this is long, it is a fundamental physical limitation.
2. In order to prevent the $A C$ coupling of the input circuit from distorting very low frequency signals, the input circuit must be DC coupled. The low frequency roll-off of the AC coupled input is easy to show by monitoring the pseudorandom noise source on the 5 Hz span with AC coupling. You will see the following:

3. On the 1 Hz baseband frequency span, the calculated point spacing is only 4 milliHertz, but the analyzer exhibits a type of "zero response" as shown.

This is not due to L.O. feedthrough as with a conventional analyzer. Rather it is due to DC drifts and offsets in the front end. These obscure the actual DC component of the input signal that the FFT would calculate. The 20 milliHertz low end frequency is somewhat subjective and is the minimum frequency component 70 dB below full scale that can be accurately resolved.
4. Filter bandwidth is a dependent variable. It is the result of selecting a calculated point spacing (by selecting a span width) and a filter shape. Thus the operator does not have to worry about it; he just sets the appropriate span.

## B. Frequency Resolution



When thinking about the narrow frequency resolution, there are several points to keep in mind.

1. Again, the length of time required to collect a time record is inversely related to the frequency span. Thus even if a 5 Hz span is located at 20 kHz , it will take 50 seconds to collect a singlechannel time record.
2. The calculated point spacing on the 5 Hz span is 20 mHz , but the bandwidth number on the CRT is the equivalent noise bandwidth. The uniform passband shape has an equivalent noise bandwidth equal to the point spacing. Because of the specialized nature of this filter shape, however, it is not generally used. It is more common, when concerned about frequency resolution to use the Hanning filter shape with an equivalent noise bandwidth of about 30 mHz on the 5 Hz span.
3. As with the baseband case, the filter bandwidth tracks the selected frequency span and filter passband shape and is not an independent selection.

C. Measurement Range


- 150 dB of measurement range in calibrated 10 dB steps.

1. The 3582A exhibits a $1 / \mathrm{f}$ type noise floor characteristic as shown on the data sheet. As the following plot shows the specifications are rather conservative at room temperature.

2. It is important to note that the noise floor specification applies to the RMS noise level. This does not imply that noise peaks will not exceed the specification limit on a random basis.
3. The overioad protection circuits are designed to handle $\pm 100$ volts DC or 120 volts RMS. Note that the AC limit is time related-with a specification of 1 minute.
D. Dynamic Range


- Full 70 dB dynamic range on all ranges except -50 dBV.

1. Recall that a 12 -bit A/D converter inherently only spans 72 dB . Extending this to better than 75 dB is the result of something called "Processing Gain" in the FFT. It requires an exceptionally linear $A / D$ converter.
2. The 3582A is actually cleaner than its specification. You can divide the distortion contributors into analog and digital and each can be highlighted individually. The digital contributors are highlighted by synthesizing a time record mathematically with a calculator. With the HP-IB this can be substituted for an input waveform. The resulting FFT distortion is as follows:


As shown, it is well down from full scale. The second example shows the analysis of an actual signal from a 339A oscillator which has harmonics over 100 dB down.


This illustrates the distortions of the entire processing chainboth analog and digital.

## E. "Real Time" Measurement Speed



- Spans of 1 kHz and over are typically analyzed in less than 400 ms .
- Spans of 1 Hz to 500 Hz (single channel) are limited by time record collection as the following shows:

| Span | 500 Hz | 250 | 100 | 50 | 25 | 10 | 5 | 2.5 | 1 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Time | .5 sec | 1 | 2.5 | 5 | 10 | 25 | 50 | 100 | 250 |

The term "real-time" is often used, but very seldom understood. Technically it is the bandwidth where the time record collection process exceeds the actual transform and display time (see Section V ). The following points are worth noting about the 3582A measurement speed.

1. It is certainly faster than a swept analyzer. While the comparisons are not exact, the following table gives a feel for the comparison.

|  | Typical Swept Analyzer |  | 3582A |  |
| :---: | :---: | :---: | :---: | :---: |
|  | Bandwidth | Time | Bandwidth | Time |
| 100 Hz SPAN | 1 Hz | 200 SEC | 0.4 Hz | $\approx 3 \mathrm{SEC}$ |
| 500 Hz SPAN | 3 Hz | 100 SEC | 2 Hz | $\approx 9$ SEC |
| 1000 Hz SPAN | 3 Hz | 200 SEC | 4 Hz | $\approx 8 \mathrm{SEC}$ |

2. The "Real Time" spans are the ones that take the longest to measure. On the 1 Hz span the measurement is in "Real-Time" but it takes 250 seconds. On the 25 kHz span the measurement is not in "Real-Time" -but it only takes about 400 milliseconds. It seems backwards, doesn't it? Section V contains a more complete discussion.
3. The actual measurement time depends on a number of things including the data being analyzed. The following table gives some typical times.


These can be expected to vary as much as 20 ms depending on the data being analyzed. Note that for maximum analysis speed in HP-IB type environments, the display should not be activated until necessary.
4. It may be worth noting that even on spans that are "Real-Time" the instrument may miss a couple of time domain samples between records. Normally, this time lag between the end of one measurement and the start of the next is only 1 to 2 milliseconds.

## F. Accuracy

$\pm 0.5 \mathrm{~dB}$


- Basic amplitude accuracy of $\pm 0.5 \mathrm{~dB}$ at the passband center.
- Basic frequency accuracy of $\pm 0.003 \%$ of the band center frequency.

1. The basic 0.5 dB accuracy applies only at the calculated points. If the component of interest is not on a calculated point, the filter passband will also contribute to the absolute accuracy. This is sometimes known as the "picket fence" effect and can be viewed as follows:


All FFT analyzers that use the Hanning window will exhibit this problem.
The Flat Top filter of the 3582A reduces the passband inaccuracy to $+0,-0.1 \mathrm{~dB}$.
3. The Frequency accuracy of $0.003 \%$ of the center frequency is better than the frequency resolution of 0.02 Hz for frequencies below 666 Hz . For higher frequencies the resolution of the 5 Hz band analysis span is much better than the specified accuracy as shown.


The worst case is at 25 kHz where the accuracy is about $\pm 0.75 \mathrm{~Hz}$.

## G. Averaging



Precise, repeatable digitally computed results.

- 4 different averaging modes with the number of averages selectable from 4 to 256 .
- Application Note 245-1 titled "Signal Averaging with the HP 3582A Spectrum Analyzer" gives details.

The digital averaging of the 3582A is similar to display smoothing or video filtering on conventional spectrum analyzer. The relationship of the two is moderately complex and is discussed in Application Note 245-1.

The following points are key:

1. RMS averaging reduces the variance of the estimate of the noise spectrum. It does not reduce the noise level or enhance the signal-to-noise ratio. It corresponds most closely to conventional display smoothing.
2. Exponential averaging in the RMS mode gives a running average with new inputs weighted $1 / 4$ and previous results by $3 / 4$. This results in an exponentially decaying weight on samples as follows:

3. The PEAK mode is not really an averaging mode. At each calculated frequency point the maximum spectral value is trapped and held. This can be useful for tracing out envelopes of signals that change in frequency with time.

4. Exponential averaging in the PEAK mode gives a continuous peak monitoring function that is stopped by releasing the repetitive trigger button.
5. Time averaging is useful for cases where discrete and random signals are mixed and where it is possible to trigger synchronously with the discrete signal. In this case, averaging provides signal-to-noise enhancement of as much as 24 dB , but does not smooth the variance of the estimate. Time averaging is the only way to obtain signal-to-noise enhancement.

## H. Noise Source



- Both random and periodic noise.
- Low impedance source with variable level.
- Noise bandwidth and location automatically tracks analysis band.
- Frequency response of $\pm 1 \mathrm{~dB}$ on periodic noise with the uniform passband.

Hewlett-Packard's years of experience with spectrum analyzer measurements have pointed out the value of a tracking generator. With an FFT type analyzer, however, a swept sine wave is not an optimum drive dignal. It will show up as a carrier with FM sidebands spaced at the reciprocal of the sweep rate.

What is required is a flat signal that is present at all of the calculated frequency points simultaneously. This is the description of a frequency comb and is exactly what the periodic noise source looks like. The details of how and why are given in Section V. Some of the key points to be aware of include:

1. The periodic noise signal automatically has a spacing exactly equal to the calculated point spacing. Thus, on the 1 kHz span where the calculated point spacing is 4 Hz , the periodic noise spectral line spacing is also 4 Hz as shown.

2. The periodic noise signal is automatically band limited and frequency translated when the analyzer is being used for band analysis. This concentrates the drive energy where it is required without disturbing other critical frequencies.
3. The periodic noise source should always be used with the uniform passband shape; the two are carefully matched. If you look carefully at the periodic noise source, you will notice that it is not exactly flat. When measuring transfer functions, however, even the residual is taken out.
4. The noise source has a crest factor (peak-to-rms ratio) of between 3:1 and 4:1. Measuring the level with an average responding voltmeter can lead to errors. More importantly, this crest factor can cause unexpected overloading of circuits designed to accept a sine wave input. A noise signal will exhibit peak excursion of more than twice what a sine wave with an equivalent RMS value will exhibit.
5. The random noise source is similar to the periodic noise source in that it is band limited and band translated, etc. The major distinction is that RMS averaging and the Hanning passband shape must be used.

## IV. New Measurement Capability

The use of advanced digital signal processing techniques allows the HP Model 3582A to perform measurements that are not possible with conventional swept analyzers. This section discusses these and provides useful facts about them.

## A. Phase Spectrum



Phase is a measure of the time displacement of two waveforms. By convention it is normalized to the basic frequency. Since it is always a relative measurement a $t=0$ reference is implied. With a network analyzer the input signal serves as this reference.

This is equivalent to using the positive slope transition through zero of a cosine as $t=0$. It is just as easy to define an entire collection of reference signals for a given time reference as follows:


It is this collection of references that is relevant when measuring phase with the Model 3582A. Note carefully that this selection of $\mathrm{t}=0$ at the center of the time record is just a fixed offset from the trigger point.

Varying the trigger point corresponds to varying the $t=0$ reference and thus the phase value.

Conceptually the 3582A can be viewed as measuring phase by filtering off the frequency in question and companing it with the appropriate hypothetical reference cosine. As an example, let's first consider a square wave fundamental and its third harmonic.


Note that in this representation, three different $\mathrm{t}=0$ references could be selected. As the example shows, all three result in the same results. If the trigger level doesn't vary, the display should remain stable. If the trigger level is varied, the display will vary, but the relative values remain stable.

The next step in conceptual difficulty is to consider two unrelated frequencies.

As before, three different $t=0$ references can be defined for $\mathrm{f}_{1}$-all resulting in the same phase value. For each of these references on $f_{1}$, however, a new set of hypothetical $f_{2}$ reference cosines is generated. If $A$ is selected, the phase of $f_{2}$ relative to the A reference cosine is $\phi \mathrm{A}$. If B is the selected reference the phase of $\mathrm{f}_{2}$ relative to the B reference cosine is $\phi \mathrm{B}$ and similarly for C . This means that if a trigger is selected to hold the phase of $f_{1}$ constant relative to its reference cosine, the phase of $f_{2}$ relative to its own reference cosine will vary as shown:


An alternative is to view the two frequencies as vectors rotating at $f_{1}$ and $f_{2}$. For any single vector the reference cosine corresponds to the line shown:


The phase corresponds to the relative offset as shown. Conceptually at least, all the reference cosine does is to stop the rotation of the vector or equivalently makes the frame of reference rotate at $f_{1}$ also. If you now add $f_{2}$ to the diagram, it must rotate relative to $f_{1}$. This implies that the angle between $f_{1}$ and $f_{2}$ or equivalently, the relative phase of the two changes predictably with respect to time.

This can be shown by measuring the combined output of two synthesizers offset slightly in frequency as follows:


Here the trigger signal is provided by $A$ which fixes the reference as $f_{1}$. By selecting the difference frequency of .1 Hz , the second $f_{2}$ vector will "catch up to" the $f_{1}$ vector every 10 seconds. The relative phase will go through 360 degrees in 10 seconds. With a 500 Hz frequency span ( .5 second time record). This rate of rotation is quite apparent.

Operationally, there are at least three distinct cases of interest.

1. Signal plus harmonics: Once a trigger level is established, a stable display with valid relative phase values results.
2. Signal plus sidebands: Once the trigger level is established, the carrier phase should remain stable but the sideband phases should vary in a predictable fashion. If the modulation is amplitude modulation (AM), the sideband phases average to 0 or 180 degrees. If it is frequency modulation (FM), they average +90 or -90 degrees from the carrier.
3. Mixed signals: About all that can be concluded is that the phases will vary with time.

A few points about the Model 3582A phase measurement capability are in order.

1. The phase of random noise poses a problem; it is also a random variable and results in a meaningless display. In order to prevent this, the 3582A does not display phase values for signals that are more than about 65 dB below the maximum input level. In these areas, it simply displays zero phase.
2. The basic display is $\pm 200$ degrees with cycling taking place nominally at $\pm 180$ degrees. In order to generate a more usable display, there is 20 degrees of hysterisis between 180 and 200 degrees. This minimizes situations where the display bounces between $\pm 180$ degrees.
3. For passbands that are fairly wide such as the flat top shape, there is more than one point on the phase line and these points exhibit a positive slope. The appropriate phase value is the one corresponding to the maximum amplitude point.
4. With the uniform passband shape, the phase reference is not a hypothetical cosine at the center of the time record, but rather at the start. This is particularly useful for transients.

## B. Transient Capture



- Time records from 10 ms to 250 seconds.
- 1024 point or 512 point time records.
- Single or multiple triggers.
- External TTL trigger or trigger on input signal.
- Selectable trigger level and slope.

The FFT analysis procedure operates on a relatively short block of data called a time record. This makes it possible for the 3582A to capture and analyze transients. There are a few points about this type of operation that are worth remembering.

1. In the 3582A the time record length is not directly selected. Instead the frequency span and the time record length are related as:

$$
\begin{aligned}
& T=\frac{250 \text { sec }}{\text { span }} \text { for single channel } \\
& T=\frac{125 \sec _{\text {span }} \text { for dual channel }}{}
\end{aligned}
$$

or
2. The uniform passband shape is virtually always used when analyzing transients because it does not pre-weight the time domain data. Since most transients have the bulk of their energy near the start of the time record either of the two "tapered" time domain weighting functions (Hanning or Flat Top) will distort the signal analyzed as follows.

3. The 3582A does not include pre-trigger capability. In some cases (particularly impulses) it is possible to externally simulate pre-trigger.
4. In most cases, setting the trigger level carefully will minimize the number of points on the transient being missed. You can graphically illustrate this by varying the trigger level and comparing successive analysis.
5. The band analysis functions operate on transient data, but you must recall that the time record length is a function of the frequency span. For the 5 Hz span to be of any value, the analyzer must sample data for 50 seconds.

## C. Transfer Function Measurements

$$
\begin{aligned}
& \text { Transfer Function Measurements } \\
& \text { - Measure amplitude with } \pm 0.8 \mathrm{~dB} \text { accuracy and phase } \\
& \text { with } \pm 5 \text { degrees accuracy. } \\
& \text { - Resolution down to } 40 \text { milliHertz over the entire } 25.5 \\
& \mathrm{kHz} \text { frequency range. } \\
& \text { - Log measurement range of }+160 \mathrm{~dB} \text { full scale to } \\
& -80 \mathrm{~dB} \text { full scale in } 10 \mathrm{~dB} \text { steps. } \\
& \text { - Linear measurement range of } 4 \times 10^{8} \text { full scale to } 4 \\
& \times 10^{-8} \text { full scale in } \mathrm{X} 10 \text { steps. }
\end{aligned}
$$

The transfer function measurement in the Model 3582A is not a simple $B / A$ ratio. It is actually the more "proper" measurement as follows:

$$
H(f)=\frac{G y x(f)}{G x x(f)}=\frac{\text { cross power spectrum }}{\text { auto power }} \text { spectrum }
$$

For theoretically ideal conditions, the two approaches would give the same answer. In reality if there are any additive signals such as noise, only this power spectrum approach gives valid answers. A few additional points are worth reviewing:

1. The band analysis functions work in the transfer function mode. You can look at a portion of the transfer function that is as narrow as 5 Hz with 40 mlliHertz resolution.
2. The passband shape to be used is determined in the same way it would be for a simple spectrum measurement.

| Drive Signal | Passband Shape |
| :--- | :--- |
| Random Noise | Hanning |
| Periodic Noise | Uniform |
| Impulse | Uniform |

Since the transfer function is measured simultaneously at all frequency points, the drive signal must be present at all frequencies measured. The above three signals fit this criteria.
3. For transfer functions with wide dynamic ranges, it may be possible to achieve better resolution of the low level portions using a swept sine wave and the PEAK averaging mode
5. The valid measurement range of the instrument is specified only to 25.6 kHz and indeed the frequency marker readout quits right there-but the display does not. By setting a center frequency of 25 kHz and using a 25 kHz span, you may see some general shapes out to about 37.5 kHz . Note very carefully that there are some significant compromises in this mode of operation. First, there are at least two out-of-band signals that appear in this range as shown.


To a fairly crude first order approximation, these will divide out in transfer functions. Second, the anti-alias filter roll-off shown places severe restrictions on the dynamic range in this area. Again, to a first order approximation, they divide out-but the signal to noise implications are severe. In short, this is not a recommended mode of operation.

## D. Coherence Function



In the most basic sense the coherence function is a normalized measure of the degree of causality between two signais. The subject is considerably more complex than this would indicate. Application Note 245-2 titled "Measuring the Coherence Function with the HP 3582A Spectrum Analyzer" is recommended for a more complete understanding of the subject. Just a few points are in order here.

1. The most common use of the coherence function is with transfer functions as follows:


Here the additive signal could be random noise or could be due to non-linearities or an unanticipated input signal. The coherence function is a measure of how significant the additive signal is relative to the measured drive signal. The result can even be related to a signal-to-noise ratio at each frequency.

From a practical point of view, the coherence function should be used with transfer functions as a kind of waming flag. If the coherence is not high, the data should be questioned.
2. If the additive signal is common to both measured signals the coherence function will not flag the problem. This might occur with 60 Hz line components, for example. Again, reading Application Note 245-2 will more completely discuss the problem.
3. If the periodic noise source is used to drive a non-linear device, the coherence function may not flag the problem. This is because the distortion products of the periodic noise signal remain constant from measurement to measurement. This usually shows up as a "ragged" looking transfer function with high coherence as follows:


One of the more common causes of this is overdriving the device under test. Switching from periodic random to random noise will highlight the problem. This is the same measurement as above but with true random noise.

4. People who are familiar with correlation often ask how it relates to coherence. The answer is that the coherence function is equal to the squared correlation coefficient between the two signals at each frequency. Application Note 245-2 provides the mathematics.

## V Some Specific Topics

There are a few aspects of the Model 3582A that warrant special attention. These include:

- Time records and the time display
- Passband shapes and window functions
- Real time bandwidth
- Noise source

The following sections provide an overview of these topics.

## A. Time Records and The Time Display

The input to the analysis procedure used in the Model 3582A is a block of time domain sample points called a time record. In order to fully understand the operation of the instrument and in particular the time display, it is necessary to be acquainted with the different types of time records. These time records vary depending on whether the analysis is single or dual channel and whether it is baseband or not.

Before actually examining the time records, it is important to consider what they represent. The actual Fourier Transform does not have an explicit time reference; it simply operates on a sequential collection of points. This also implies that it does not have an explicit frequency reference; it simply outputs a sequential collection of points. The only absolute calibration is provided by the sampling rate which is in turn controlled by the frequency span setting.

## Baseband Modes

The following simple relationships are key for baseband or O-Start analysis:

## where

$$
\begin{aligned}
\Delta t & =\frac{1}{4 F S} \\
T & =N \Delta t \\
\Delta f & =\frac{1}{T}
\end{aligned}
$$

$\Delta t=$ the time domain sample spacing
FS = the selected frequency span
$\mathrm{N}=$ the number of time domain samples (1024 for single channel) ( 512 for dual channel)
$\mathrm{T}=$ the total time record length
$\Delta f=$ the frequency domain sample spacing

In the baseband modes, the time record is composed of 1024 (single channel) or 512 (dual channel) time samples. These N samples are transformed to $\mathrm{N} / 4$ complex frequency points as follows:


SINGLE.CHANNEL BASEBAND
Note that both positive and negative frequency points are calculated but the negative points provide no new information. Also note that the upper half of the frequency points are discarded as potentially aliased.

Since the actual display hardware of the 3582A is only capable of displaying $512 \mathrm{X}-\mathrm{Y}$ points, the entire 1024 point single channel baseband time record can't be displayed. The compromise solution is to display only the alternate points as the annotation shown.


For consistency, this is also the way dual channel baseband time records are displayed.

In using the baseband TIME display function, it is vital to remember that the display is of samples of a waveform. These samples do have enough theoretical information to allow reconstruction of the input-but the human eye may not properly perform the reconstruction. The following two examples illustrate this.


1 KHz on the 25 KHz range


24 KHz on the 25 KHz range

Both contain sufficient information for complete analysis of a pure sinusoid-but one visually appears quite different after sampling. Quite obviously the 3582A is not a time doman oscillosscope. In fact for signals that are more than about $10 \%$ of the frequency span, the visual distortion becomes noticeable.

## Band Analysis Modes

The time record is quite different in the band analysis modes since each time domain sample is converted to a complex value with both|"real" and "imaginary" parts. This means that there is a factor of two |differences between the number of time domain sample points and the number of time record points. The following simple relationships are key for band analysis:

The major difference is that the time record is complex. The actual processing proceeds as follows:


As before, the N complex time point pairs transform to N complex frequency point pairs, but now all N provide necessary information. Of the N , the upper half are still potentially aliased and are discarded resulting in $\mathrm{N} / 2$ valid points. As in the baseband case, there are 256 valid pairs in the single channel mode and 128 in the dual-channel mode.


The time display in the band analysis mode is a compromise, since the time record is complex. The display annotation is even more specific calling it low pass filtered, sampled and heterodyned. As shown, the samples displayed are the "real" samples or those multiplied by cosine terms in the band analysis procedure. About the only major use of this display is to see whether or not signals are present. Its physical interpretation is difficult at best. Probably the easiest way to view it is as the difference between the incoming signal frequency and the band analysis local oscillator.

## B. Passband Shapes and Window Functions

In a conventional spectrum analyzer, the passband filter shape is a hardware filter with the shape determined by the need to sweep. In an FFT analyzer, the filter shape is the result of the processing done on the collection of the time domain samples as described in Appendix A. As the following illustration shows, the Fourier transform of the time domain weighting is the filter shape.


In fact, the time domain weighting functions are synthesized in order to achieve certain filter characteristics.

The 3582A provides three distinct passband filter shapes for different measurement situations. Each is optimized for a different type of measurement as the following chart illustrates.

| PASSBAND FILTER SHAPE | APPLICATION |
| :--- | :--- |
| FLAT TOP | DISCRETE SPECTRAL LINE <br>  <br>  <br> MEASUREMENTS |
| UNIFORM | RANDOM NOISE <br> MEASUREMENTS |
|  | TRANSIENTS ANLD THE <br>  <br>  <br>  <br>  <br>  <br>  <br> PERIODIC NOISE <br> SOURCE |

Normally this chart is all you need to remember-but in some cases, the concept of the "picket fence" effect or "leakage" will come up.

## Picket Fence

As noted in the introduction, the FFT process used in the 3582A effectively uses 256 parallel filters to obtain a display. The spacing between these filters as well as the width of the individual filters is controlled by the frequency span setting. This causes a problem that is sometimes referred to as the "picket fence effect." If a signal falls midway between two adjacent filters, it will not show up at full amplitude, but rather will reflect the roll-off of the filter.

The extent of the problem depends explicitly on the weighting function or passband shape selected. The three passband shapes of the 3582A compare as follows:


Note that this is not a function of the specific product-but rather is characteristic of any FFT analyzer that uses these filters.

## Leakage

In addition to the "picket fence" effect, the FFT synthesized filters exhibit a behavior referred to as "leakage."

In a conventional spectrum analyzer, the passband filter shape is usually $\mid$ Gaussian. As a spectral line is analyzed, it does not come out as an ideal impulse-but rather it traces out the shape of the filter.

Leakage is very similar in that the spectral line effectively traces out the filter shape. The difference is that the FFT analyzer selects only discrete points off the shape which are then joined with line segments.

The easiest case to examine is the uniform case. The filter shape that corresponds to this time domain function is the $\sin X$

X shape.

The display that results will depend on where the selected discrete points fall. The following example illustrates two distinct possibilities.


The Hanning passband shape has considerably lower sidelobes-with almost no leakage. The tradeoff is that the basic filter shape is considerably widened for each improvement in leakage reduction.

The real key is, of course, which is used for a specific measurement. That is summarized in the earlier table.

## C. Real-Time Analysis and Real Time Bandwidth

The term "real time" can be relatively confusing because it is not consistently defined and thus often is misinterpreted. Three common definitions are:

- One hundred percent processing of incoming time domain information.
- "Very fast" as opposed to the slower processing of a swept filter type analyzer.
- Flicker-free oscilloscope trace presentation.

Technically, only the first definition is correct-but even it does not provide the answer to how fast a measurement can be made.

An FFT based analyzer like the 3582A processes data in two distinct steps. First, a time record must be completely collected and then the entire time record is transformed to a spectrum record. The time required to process a time record is the transform and display time and is a function of the hardware realization. The time required to collect a time record is determined by the FREQUENCY SPAN and, given a fixed time record size, is independent of the hardware. It is the relationship of these two times which determines the "real time bandwidth." When the transform display process is finished before the next time record is collected, the processing is in real time. In this case the physical sampling laws constrain the measurement time. When the time record collection finishes first, there will be gaps in the data being analyzed; the processing is not real-time. The following illustrates both situations.


NON REAL-TME PROCESSING: $T<P$

This still does not indicate what impact a higher real time bandwidth has from a measurement point of view. This is best illustrated by comparing the measurement time that would result from having a higher real time bandwidth as follows:

|  | MEASUREMENT TIME |  |
| :---: | :---: | :---: |
| SPAN | 500 Hz REAL TIME <br> BANDWIDTH | 2500 Hz REAL TIME BANDWIDTH |
| 1Hz | 250 SEC | 250 SEC |
| 2.5 Hz | 100 SEC | 100 SEC |
| 5 Hz | 50 SEC | 50 SEC |
| 500 Hz | $\cong 1 \mathrm{SEC}$ | $\cong .6 \mathrm{SEC}$ |
| 1000 Hz | ミ.75 SEC | ※.35 SEC |
| 2.5 kHz | き. 6 SEC | $\cong .2 \mathrm{SEC}$ |
| 5kHz | $\cong .5$ SEC | $\cong .15$ SEC |

Where the measurement time is highest (e.g., 250 seconds) you are operating in real-time. Where it is lowest you are not.

## D. Noise Source Characteristics

If you view the FFT as implementing 256 parallel filters, it is clear that a swept sine wave is not an optimum stimulus source. A compatible source must stimulate all 256 measured frequencies simultaneously.

Any of the following signals will accomplish this:

> Impulse
> Gaussian White Noise
> Pseudorandom Noise

Each is useful in certain measurement situations and each has some limitations. The impulse signal is easy to generate in mechanical measurements but the extremely high crest factor can cause overloading. Random noise has substantial advantages where the device may be somewhat non-linear, but requires extensive averaging to obtain valid results. Pseudorandom noise provides valid results without averaging but gets into trouble when the device is non-linear. All three signals are provided on the 3582A. Appendix A provides an overview of the actual hardware realization.

In the band analysis modes, the noise signal is first generated as the proper bandwidth at DC. It is then mixed with the band analysis local oscillator which translates the noise to the proper frequency. This minimizes the energy that is applied to portions of the spectrum not being measured.

As long as the device under test is linear, the periodic noise source provides excellent results without averaging. When the device exhibits non-linearity, harmonics of stimulus spectral lines are generated. Since the noise source is periodic with a period equal to the time record length, the harmonics will be consistent from measurement to measurement. This means that they will cause unwanted responses that do not average out. The coherence function will not identify these responses.

In addition, since the periodic noise has a finite spacing between frequency lines, it is possible that very narrowband responses will not be properly stimulated.

In order to minimize these problems, a more nearly random noise signal is also provided. This is generated by simply lengthening the sequence. For all practical purposes, this period of the sequence is so long, two identical time records are separated by substantial periods of time. This means that distortion products, when generated appear as random components; they vary from time record to time record. They will average out of the result and the coherence function will illustrate the extent of the measurement problem. The major disadvantage of the random noise stimulus is that extensive averaging must be used to get valid results.

It is worth noting that the periodic noise signal always has one period in the time record, but the start of the period does not occur at the same point. By using the rear panel impulse signal as an extemal trigger, the noise signal will be periodic and will always start at the same place in the time record.

From a practical point of view the periodic noise stimulus should be used as long as it gives valid results. Unfortunately, determining when results are valid is difficult. About the only check is to look for a "ragged" response or to compare the result with a random stimulated result.

## VI. Operating Details

The Model 3582A is more than just a spectrum analyzer; it is a sophisticated measurement tool with five significant measurement modes. These are:

- single channel amplitude spectrum
- single channel phase spectrum
- transient capture and analysis
- dual-channel transfer function
- dual-channel coherence function.

This section provides a concise overview of the operational details of making these measurements. In addition, it also covers some other topics such as overloads and operational diagnostics.

## A. Instrument Preset Conditions

Under manual front panel control, the state of the 3582A is defined by the positions of the latching pushbuttons and switches. Unlike an instrument with true keyboard control, there is no single button that presets the instrument to a fixed set of conditions. The reset button only redefines the instrument state to match the front panel control settings.

The HP-IB interface does include an instrument preset command ("PRS") to bring the instrument to a known state. In this state it is basically set to measure a single channel amplitude spectrum over the full 25 kHz span. This is an ideal starting point for setting up most measurements. As the following illustrations show, all of the measurement checklists use the preset state as a starting point. The illustrations only indicate the deviations from the preset state.


## INSTRUMENT PRESET STATE

| OPERATING CONTROL | PRESET SETTING |
| :--- | :--- |
| Input Coupling | AC (Both channels) |
| Input Mode | A |
| Input Sensitivity | +30 dBV (both channels) |
| Trigger Slope | - |
| Trigger Level | Free Run |
| Trigger Repetitive | On |
| Frequency Span Mode | $0-25 \mathrm{kHz}$ Span |
| Frequency Span | 25 kHz |
| Marker | Off (all controls) |
| Display Amplitude | A (only) |
| Display Scale | $10 \mathrm{~dB} / \mathrm{div}$. |
| Amplitude Reference Level | Norm |
| Display Phase | Off (all controls) |
| Display Coherence | Off |
| Passband Shape | Flat Top |
| Average | Off |
| Average Number | 4 (No shift) |
| Trace 1 and 2 | Off (All controls) |

## B. Important Control Settings

In some operating modes, the Model 3582A will not initiate a new measurement until commanded to do so by the operator. It may appear under these conditions that the instrument is "hung-up" when actually it is simply awaiting further instructions. If the instrument is not sampling-as indicated by the DATA LOADING indicator not flashing-the following control settings should be reviewed.


1. When in the Non-REPETITIVE mode (button out) the instrument will initiate a new measurement only when ARMed.
2. When not in FREE RUN the instrument will initiate a new measurement only when the LEVEL and SLOPE trigger conditions are satisfied. The LEVEL will depend on the input SENSITIVITY.
3. When the instrument completes an average sequence, it stops until RESTARTed or until AVERAGING is turned off.
4. When the instrument is under remote HP-IB control, it will not respond to front panel changes until returned to local control.
5. The RESET control executes a power-up sequence which redefines the instrument state to correspond to the front panel switch settings.
6. When the CRT INTENSITY control is turned off, there will be no display present.
7. When the rear panel trigger switch is in the EXT position, only the FREE RUN front panel position is valid. When out of FREE RUN, triggering is initiated by rear panel signals.

## C. Single Channel Amplitude Spectrum Measurement

The instrument preset condition is essentially the proper set up for single channel amplitude measurements. Normally the only changes required are to the INPUT SENSITIVITY controls and possibly the FREQUENCY SPAN and MODE controls. The MARKER functions will provide direct or relative readout of results.


## SINGLE CHANNEL AMPLITUDE SPECTRUM

## STEP

OPERATIONAL ACTION

1. Set the instrument to the preset state.
2. Adjust the input SENSITIVITY control until the overload indicator goes out.
3. If further analysis is to start at DC, select the 0-START FREQUENCY SPAN mode and the appropriate SPAN.
4. If further analysis is to be band analysis, turn the intensified dot MARKER on and position it to the signal of interest.
5. Press SET FREQ. to define the marker frequency as the start or center of the analysis band. Select the appropriate FREQUENCY SPAN MODE and FREQUENCY SPAN.

## D. Single Channel Phase Spectrum Measurement

Normally the simplest way to make a single channel phase spectrum measurement is to start with the appropriate single channel amplitude spectrum. In order to get a usable display a trigger condition must be established.


## SINGLE CHANNEL PHASE SPECTRUM

## STEP

OPERATIONAL ACTION

1. Set the instrument to the preset state.
2. Set up the appropriate single channel amplitude spectrum measurement.
3. Select the desired TRIGGER SLOPE. View the CHANNEL A TIME display and adjust the TRIGGER LEVEL. The unit is triggering with the DATA LOADING light on.
4. Select the CHANNEL A PHASE display. If the frequency components are not harmonically related the display will vary from measurement to measurement. Selecting NON-REPETITIVE triggering and using the ARM control will trap a single display.

## E. Transient Capture and Analysis

The only difference between amplitude measurements is usually the selected trigger conditions and the passband shape. The following illustrates the difference.


## TRANSIENT CAPTURE AND ANALYSIS

STEP
OPERATIONAL ACTION

1. Set the instrument to the preset state.
2. Select the UNIFORM PASSBAND SHAPE.
3. Select the appropriate CHANNEL A SENSITIVITY
4. Set the proper TRIGGER SLOPE, TRIGGER LEVEL and whether or not triggering is to be REPETITIVE. If non-repetitive triggering is selected, the ARM control must be used.
5. Select the appropriate time record length by adjusting the FREQUENCY SPAN control and viewing the. TIME display.

## F. Dual-Channel Transfer Function Measurements

The exact sequence of operations required for making transfer function measurements depends on the type of stimulus source. An impulsive stimulus or the periodic noise stimulus requires the UNIFORM PASSBAND SHAPE. The random noise stimulus requires the HANNING PASSBAND SHAPE and averaging.


## DUAL CHANNEL TRANSFER FUNCTION

1. Set the instrument to the preset state.
2. Select the INPUT MODE of BOTH and adjust both INPUT SENSITIVITIES.
3. Select the UNIFORM PASSBAND SHAPE if using the built-in PERIODIC NOISE or an impulse for a stimulus. Select the HANNING PASSBAND shape if using a random noise source.
4. Select the XFR FCTN display of AMPLITUDE and/or PHASE. Use the AMPLITUDE REFERENCE LEVEL control to bring the amplitude display on scale.
5. If further analysis is to start at DC select the O-START FREQUENCY SPAN MODE and the appropriate SPAN.
6. If further analysis is to be band analysis, turn the intensified dot MARKER ON and position it to the signal of interest.
7. Press SET FREQ to define the marker as the start or center of the analysis band. Select the appropriate FREQUENCY SPAN MODE and FREQUENCY SPAN. Note that the INPUT SENSITIVITIES may have to be readjusted.

## G. Dual Channel Coherence Function Measurements

The dual channel coherence function is used in two distinct situations; as a "confidence" overlay on transfer functions and as a way to investigate cause/effect relationships. From a measurement point of view, the two are set up the same way.


DUAL CHANNEL COHERENCE FUNCTION
STEP
OPERATIONAL ACTION

1. Set the instrument to the preset state.
2. Select the INPUT MODE of BOTH and adjust both INPUT SENSITIVITIES.
3. Select the UNIFORM PASSBAND SHAPE if the inputs are the built-in PERIODIC NOISE or are impulses. Select the HANNING shape if the inputs are predominantly random. Select the FLAT TOP shape if the inputs are predominantly spectral lines.
4. Select the appropriate FREQUENCY SPAN MODE, SPAN WIDTH, and if required, the proper display start or center frequency.
5. Select RMS AVERAGE and the desired number or averages.
6. Select the COHER DISPLAY and any other display trace desired.

## H. Operational Diagnostics

The powerful microcomputer control of the 3582A makes it possible to diagnose most operational mistakes. When an invalid measurement situation is detected, the instrument continues with the last valid state that it was in until the invalid situation is corrected. As long as a diagnostic is on the screen, only the RESET and POWER controls will be recognized. These controls cause the instrument to cease doing anything until the invalid condition is corrected. The following examples illustrate the invalid situations that can occur.


The instrument can display only two traces including stored traces. The display won't change until you are down to only two traces selected.


Trying to display any CHANNEL A data while set to the B INPUT MODE or vice versa is invalid.


Since dual channel traces are 128 points and single channel traces are 256 points, you can't mix them. This means you can't store a single channel display and compare it with a dual channel display.


The TIME display is a full 512 points (altemate points of the 1024 point time record). This is twice as big as the storage area so it can't be stored.


Band analysis spans cover only 5 Hz to 25 kHz . When the 2.5 Hz or 1 Hz span is selected in the SET CENTER or SET START modes, everything is ignored until you correct the span setting.


Both input channels must be selected before a transfer function measurement can be made.


Coherence only makes sense in the dual channel mode and with averaging. See Application Note 245-2 for the detailed reasons why.


If the PASSBAND SHAPE is changed while doing PEAK or RMS averaging, the results will be invalid. Such changes are ignored until you press RESTART. If a change to or from a FREE RUN trigger is made while averaging, the same problem exists.


There is no exponential TIME average. Note that PEAK average can also be selected, but it is not truly exponential.


TIME average depends upon a synchronizing trigger for valid results. Without it, the measurement would not be useful.


All of the AVERAGE MODES except TIME are properly calibrated as they progress. For example, if an RMS average is stopped at 146 by releasing the REPETITIVE control, the display is valid. This is not true for TIME average. Valid results are obtained only at the specified AVERAGE NUMBER.

## I. Overloads

There are two distinct overload indications on the 3582A and they serve different functions.


The LED overload indicators show momentary overloading of the input $A / D$ converter or the digital filters. Either of these conditions indicates a "hard" overload as the following example illustrates. When the input is clipped like this, the spectrum display is of the clipped signal-which in this case is similar to a square wave.


Non-overloaded time domain


Non-overloaded frequency domain


Overloaded time domain


Overloaded frequency domain
Valid measurements require the overload LED indicators to be out. There is no graceful overload of the front end; it is a hard clipping.


The CRT overload is somewhat more subtle. It is more of a warning or caution than anything else. It indicates that one or more of the time samples being analyzed may be invalid. For example, with a random noise input it indicates that one or more of the random excursions was clipped by the A/D converter. It also indicates that the data being analyzed may be contaminated by ringing of the digital filters as the following example shows.


Here the ringing is caused by an occurrence in time record N . Its effects may or may not contaminate record $\mathrm{N}+1$. Since an accurate determination of the effects can't be made, the CRT overload indicator is set during the analysis of both records N and $\mathrm{N}+1$.

Similarly, if an overload occurs during any time record that is part of an average sequence, it may contaminate the results. Under these conditions the CRT overload indicator is latched for the duration of the potentially contaminated average sequence.

It is worth noting that any change of the INPUT SENSITIVITY control or the FREQUENCY SPAN MODE control cause momentary transients which show up as overloads. These will cause the overload LED to blink and the CRT overload to latch. Pressing RESTART will clear the latched CRT overload.

The actual level at which overloading occurs depends only on the setting of the INPUT SENSITIVITY Control. The AMPLITUDE REFERENCE LEVEL control is only a display scaling operation. With this control set to its normal position, the overload limit is at exactly full scale on the two log amplitude display modes.

The overload limit on the LINEAR amplitude mode is somewhat unusual. With the AMPLITUDE REFERENCE LEVEL control set to normal, the overload limit or maximum input level varies in a 1-3-10 sequence. The display full scale value, however, varies in a 4-8-16-40 sequence. This means that the overload limit is actually at either the 5th or 6th graticule line as follows:


Linear mode overload at 6th graticule


Linear mode overload at 5th graticule

## VII. Basic Measurements

There are numerous areas where low frequency spectrum analysis is important. A few of the more significant are:

- Traditional electronics
- Telecommunications
- Mechanical and electromechanical systems
- Audio/acoustical
- Sonar/underwater sound
- Geophysical/seismic
- Biomedical

Within each of these segments, there are unique measurement problems that the 3582A will solve. This section presents a few specific comments about measurements found in these areas.

## A. Traditional Electronics and Telecommunications

This is certainly the most familiar area of application for the Model 3582A. As such, most of the following measurements are review. The emphasis is on the unique capabilities that allow the 3582A to make the measurements better than before. The number of measurements reviewed indicates the exceptional flexibility of the instrument.

## 1. Harmonic Analysis

For measuring Total Harmonic Distortion (THD), the HP family of distortion analyzers is great. For analyzing harmonics individually, a spectrum analyzer is required. The 25 kHz frequency range limits the 3582 A to low audio frequency signals, but in this range it has some unique capabilities.

The 3582A is unique in that it allows the phase of the harmonics to be measured. Some care must be exercised in setting up the phase reference but valid relative results are simple to obtain.

In some cases the 70 dB dynamic range of the 3582A may not be sufficient to see the harmonics as with the oscillator in the 339A. An interesting solution to this problem is as follows:


Here the internal notch of the 339A is used to eliminate the high amplitude fundamental and the result or residual output is measured on channel B. Putting the source on channel A provides a trigger signal for the TIME AVERAGE Mode. This allows the signal-to-noise ratio for the harmonics to be improved.

## 2. Spurious Tones, Sidebands, Etc.

The measurement of spurious tones, etc., is a straightforward spectrum analysis task, but the 3582A offers a couple of unique capabilities. The exceptionally narrow resolution bandwidth makes it possible to resolve tones or sidebands very close together or near the carrier. The marker is capable of very accurate frequency ( $\pm 0.003 \%$ ) and amplitude readout of these tones. Again, with the phase capability, it is also possible to gain more information about a signal such as whether sidebands are AM or FM.

## 3. Close-In Phase Noise

The low end frequency coverage and real time measurement speed of the 3582A make it well suited to measuring close-in phase noise. Application Note AN 207 (Understanding and Measuring Phase Noise in the Frequency Domain) describes the following measurement technique:


A typical plot for a synthesizer looks like this:


Note that the $\div \sqrt{B W}$ marker function reads out the noise level normalized to a 1 Hz bandwidth directly. This eliminates the need to correct the reading for analyzer characteristics.

## 4. Modulation Measurement

There aren't a great number of applications where an audio frequency carrier is intentionally modulated-with the exception of modems. Modulation does occur unintentionally and as noted earlier, the phase spectrum can be used to determine the actual type of modulation.

## 5. Intermodulation Distortion

There are two methods commonly used for measuring intermodulation distortion. One is the SMPTE method:


The other is the CCIF method.


The 3582A handles both measurements with ease.


SMPTE method


CCIF method

## 6. Crosstalk

The dual-channel capability of the 3582A is handy for making crosstalk measurements as follows:


Putting the driven input on CHANNEL A and the crosstalk input on CHANNEL B allows the relative marker to directly read how far down the crosstalk is. Again, triggering on CHANNEL A and using the TIME AVERAGE can improve the ratio of the crosstalk signal to noise. If the built-in noise source is used as the drive source, crosstalk as a function of frequency is displayed with the marker still useful for direct readout. The 140 dB crosstalk specification of the 3582A should not pose problems in this measurement.

## 7. Filter Characterization

The transfer function capability of the 3582A provides both the gain and phase characteristics of two port networks such as filters. While this is very similar to the common network analyzer measurement, there are some differences:
a. The built-in noise source has a crest factor of between 3:1 and $4: 1$ as compared with a sine wave crest factor of about $1.4: 1$. As the following illustrates, additional care must be taken to prevent the device-under-test from clipping the drive signal:

b. If the transfer function covers a wide dynamic range, averaging may be required in order to properly resolve the low level portions of the function. In these areas the signal-tonoise ratio is fairly low-but RMS averaging tends to smooth the truly random noise.
c. The coherence function can give you a qualitative measure of the signal-to-noise ratio at points of the measurement. It also gives confidence measures on the results.
d. It is even possible to obtain transfer function measurements with impulsive inputs-but the crest factor problems can be severe. The impulse can be generated externally and measured on channel A or in some cases, the rear panel impulse can be used.

## 8. Electrical Impedance

Impedance measurements are nothing more than specialized transfer function measurements. They are specialized only in that one of the input signals is a voltage directly proportional to the current. While RLC meters measure impedances at fixed frequencies, this transfer function approach can give more complete results for complex impedances such as loudspeakers as shown:


Also, this approach can give good results at very low impedances.

The most straightforward approach is to use a series sensing resistor as shown:


Probably the main thing to remember is that the noise source is capable of only about 10 mA of output current so the total load must be $50 \Omega$ or greater.

A second approach is to use a current sensing probe such as the Model 456A.

## 9. Amplifier Rejection Characteristics

The 3582A can be used to characterize both the common mode rejection and power supply rejection characteristics of an amplifier as shown:


## B. Mechanical Systems

The study of mechanical sound and vibration is another area of application for the HP 3582A. With the appropriate transducers force and motion can be studied in the frequency domain. The following are some of the typical measurements of interest.

## 1. Rotating Machinery Signatures

Vibration is the motion of a mechanical structure caused by some type of force. One of the more common applications for measuring vibration is in characterizing the "health" of rotating machinery. Every rotating machine exhibits a unique vibration pattem or "signature" that is best viewed in the frequency domain.

Before dealing with the actual measurements, let's look at the sources of the vibration components. If there is an unbalanced mass off center from the rotating shaft, a rotating force vector of magnitude $\mathrm{F}=\mathrm{MRW}^{2}$ is generated. When a transducer is mounted at a fixed point, it sees the projection of a vector rotating at $W=2 \pi \mathrm{Fr}$. In the frequency domain, this is just a spectral line at Fr .

Now let's turn to the ball bearings in which the shaft rotates. As the following shows,

d = BALLDIAMETER
D = PITCH DIAMETER
$\mathrm{N}=$ NUMBER OF BALLS
$F=$ ROTATION FREQUENCY

- $F_{r}=$ ROTATION FREQUENCY
- $F_{B}=$ BALL ROTATION FREQUENCY

$$
=1 / 2 \cdot F_{r} \cdot\left(\frac{D}{d}\right) \quad\left[1-\left(\frac{d}{D}\right]^{2}\right)
$$

- $F_{C}=$ CAGE ROTATION FREQUENCY
$=1 / 2 F_{r} \cdot\left(1-\frac{d}{D}\right)$
- $F_{\emptyset}=$ OUTER BALL PASSING FREQUENCY
$=1 / 2 \cdot F_{r} \cdot N \cdot\left(1-\frac{d}{D}\right)$
- $\mathrm{F}_{\mathbf{I}}=\operatorname{INNER~BALLPASSING~FREQUENCY~}$
$=1 / 2 \cdot F_{\mathbf{r}} \cdot N \cdot\left(1+\frac{\mathbf{d}}{\mathbf{D}}\right)$
the bearing geometries cause spectral lines-all related to Fr . Modulation and intermodulation products are generated, again related to Fr . Only the true random noise components are not directly related to Fr. Similar results for gear trains can be derived.

The result is a messy spectrum with a relatively high level. The key problem is to identify problems as indicated by component changes. For example if the component Fr changes, the problem is likely to be balance. Other components can even be related to actual geometries.

## 2. Rotating Machinery Balance

There are at least three major types of unbalance that are routinely discussed. The most common is called STATIC UNBALANCE and is when a single mass is off center as shown:


As mentioned earlier, the transducer effectively sees the projection of a rotating force vector which is just a sinusoid. With a little effort, the 3582A can identify and help correct this problem. First a single tach pulse must be generated to provide a position reference. By triggering with this signal, the phase of the unbalance signal gives the angular location of the unbalance.

Now by experimentally adding a known counterbalance mass at a known location, a new result is generated. Some straightforward vector algebra on the two sets of results will define how large the counterbalance mass should be.

A second type of unbalance is COUPLE UNBALANCE where two unbalanced masses cancel each other statically, but when rotated, set up a twist force.


This problem is solved in much the same way as before. Additional counterbalance weights are experimentally attached to the rotating parts. The number of experimental modifications and the vector algebra are more complex, but the process is fairly similar.

The final type of unbalance is DYNAMIC UNBALANCE which is just a combination of STATIC and COUPLE unbalance.

## 3. Mechanical Impedance Measurements

Mechanical systems and electrical systems are fundamentally very similar if you just remember the following correspondences.

| Electrical | Mechanical |
| :--- | :--- |
| Current | Force |
| Voltage | Velocity |
| Resistance | Damping |
| Capacitance | Mass |
| Inductance | Spring |

When you consider mechanical systems as collections of masses, springs, and dampers, it is not surprising that a concept similar to electrical impedance becomes important.

The major difference is that in the electrical world, voltage and current are taken as the basic units. In the mechanical world, force is standard but motion is measured as displacement $(X)$, velocity $\left(\frac{d x}{d t}\right)$ or acceleration $\left(\frac{d^{2} x}{d t^{2}}\right)$.
This leads to six ratios where in the electrical world, there are only two:

| RESPONSE <br> PARAMETER | DISPLACEMENT |
| :--- | :--- | :--- | :--- | VELOCITY $\quad$ ACCELERATION

The key, of course, is how you actually measure useful information. That can be viewed as follows:


RESPONSE $1=$ DRIVING POINT MEASUREMENT FORCE
RESPONSE $2=$ TRANSFER MEASUREMENT FORCE

From this type of measurement, the result is typically a plot like this:


The resonances tend to relatively high Q -e.g. factors of 50 or larger are not uncommon. If the mechanical designer designs his safety margins on the average motion level, he may have to use extremely high margins-or his structure may shake itself apart. Most likely, he would try to modify the structure to dampen the resonances or to move them out of the area of trouble. In many cases, this is done experimentally implying a need for measurement of results.

These mechanical impedance type measurements require dual-channel transfer function capability. A second point is that mechanical resonances tend to be sharp and close together so band selectable analysis is a major requirement.

## 4. Feedback System Characterization

The designers of feedback systems almost invariably need to know the frequency and phase response of their closed loop system. By adding noise to the system, the Model 3582A can determine the parameters of the operating loop. The technical details of this type of application are discussed in Application Note 140-2.

Basically, the method can be viewed as follows:


Here the noise is added to the forward part of this loop with a summing node.

The Model 3582A is used to measure the transfer function $\mathrm{Y} / \mathrm{N}$. This is the "test ratio" T described in Application Note 140-2.

## Appendix A.

## Theory of Operation

The Model 3582A is a dual channel spectrum analyzer based on the calculation of the Discrete Fourier Transform by the use of the highly efficient Fast Fourier Transform algorithm. This section concentrates on the hardware organization. The basic block diagram is shown.


Both of the input channels are identical as shown. Their operation is principally determined by whether or not the frequency span mode is in SET START or SET CENTER or not. The simplest case to consider is the O-START case where the analysis always starts at DC. In this case, only one of the two digital filters is actively producing time sample outputs.

The 25 kHz analog low pass filter serves to eliminate any energy that could be aliased into the range of interest by the sampling process.

After this initial analog filtering, the input signal is fed into the 12 -bit A/D converter. This produces a sequence of samples at a 102.4 kHz rate. * Further anti-alias filtering for all but the 25 kHz span is done digitally.

The four LSI digital filters represent an exceptional technology contribution. They are 200 mils on a side and perform several significant processing operations.

[^0]

This implementation is critical to the price/performance ratio of the Model 3582A. From a block diagram point of view, the digital filters appear as follows:


Note that it is a cascade of eight distinct filter stages, each of which can reduce the incoming bandwidth by a factor of 0,2 , or 5. Thus, for example, to get the filtering for the 1 Hz range, the original 25 kHz bandwidth must be reduced by 25,000 . This is
done by cascading five sections of $\div 5$ and three sections of $\div 2$ for a result of $\left(2^{3}\right) \cdot\left(5^{5}\right)=25,000$. The characteristics of the $\div 2$ and $\div 5$ sections are as follows:


After the signal has been digitally low pass filtered, the samples that appear at the output are no longer independent. This means that parts of the data are theoretically redundant and can be ignored. This function is referred to as sample rate reduction. It essentially involves selecting samples at a rate of four times the span width. For example, on the 1 Hz span, only four samples per second are retained even though 102,400 per second come into the filter. What comes out of the filter is a properly anti-aliased filtered signal sampled at four times its maximum frequency of interest. This data is stored in the time buffer until a full 1024 point (single channel) or 512 point (dual channel) time record is complete.

In the SET START or SET CENTER frequency span modes, the digital filters perform a third function for band translation. In these modes, both digital filters in the input channel are processing data. One of the filters multiplies the incoming digital data by the digital value of the "local oscillator" cosine generator. The other multiplies the incoming data by the digital value of the "local oscillator" sine generator. The output of the first filter is treated as "real" data and the second as "imaginary" data. The result is that the time record that is constructed now consists of 512 complex points (single channel) or 256 complex points (dual channel). The FFT algorithm can process either real or complex data.

Once a time record is complete in the time buffer, the selected time domain weighting is applied to it. This is just a point by point multiplication of the record and a stored weighting function. The rest of the processing is basically software executed by the same powerful 16 bit microcomputer found in the HP Model 9825A desk top computer.


The program executes an FFT that is organized as follows:


The noise source is based on the generation of a pseudorandom binary sequence which is then filtered. The block diagram is as follows:


In the periodic noise configuration, the shift register outputs a sequence of pseudorandom binary pulses that result in a ( $\frac{\sin x}{x}$ ) line spectrum as follows:


By passing this signal through a good low pass digital filter,

a good approximation to a frequency comb is generated. By carefully selecting the filter cutoff, the slope of the envelope is kept very small. Note that the digital filter automatically tracks the modified clock frequency so it serves all spans.

In order to band translate the noise, the digital numbers that come out of the local oscillator are converted to the equivalent analog cosine signal. This is then mixed with the noise to translate the spectrum to the desired frequency.

In the random noise case, the length of the sequence is extended substantially. This results in a shift register period usually measured in hours and a line spacing that puts several thousand lines between calculated display points.

## Appendix B

## REMOTE OPERATION

In remote operation, the 3582A has even greater flexibility than in manual operation. The following functions describe how the 3582A may be controlled through the HP-IB.*

## Remote Front-Panel Programming

In addition to the normal front panel switch controls, the operation of the 3582A can be controlled by remote commands sent on the HP-IB.

## Instrument Data Output

Display data, alphanumerics, switch settings and other useful data can be output from the instrument for the purpose of making plots, additional processing, etc.

## Instrument Data Input

Time record data obtained by external means can be input to the instrument for analysis. Also, any of the instrument data output may be reentered into the instrument at a later time.

Instrument Signal Processing Control and Status Additional Special HP-lB commands allow limited control of the signal processing. An 8 -bit status word is available to indicate various states of the signal processing.

## I. REMOTE FRONT PANEL PROGRAMMING.

The Command List specifies all of the functions which may be activated by the 3582A via the HP-IB. Note that many of the functions are the remote equivalent of setting a front panel switch manually and may be executed in similar sequences. For example, the arm command (AR) would not be given until all other applicable functions are set for a measurement operation. The Command List is given at the end of this Appendix.

The HP-IB status light "REMOTE," located at the lower left of the front panel, indicates whether the instrument is currently operating under local (front panel switches) or remote control. Remote operation is accomplished only via commands sent on the HP-IB.

When the instrument is in local, the operation is determined solely by the front panel settings. At the time that the instrument is programmed to remote, the operation remains exactly the same as it was in local. Additional commands sent on the HP-IB can change the mode of operation. Returning to local, either by pushing the LOCAL button or by an HP-IB command, causes the instrument to return to front panel switch control.

## A. Syntax.

The Command List (actually sent as DATA) is divided into groups of related operations. Each command in a group is divided into a function and a setting (some groups do not have settings). If the function is a front panel switch, the

[^1]letters will correspond to the underlined letters of the name of that switch on the front panel. The setting indicates a switch position. A zero setting will indicate that the switch is out (OFF) and numbers greater than zero indicate that the switch is in (ON) or set at some other position (rotary switches and slide switches). On rotary and slide switches, a one (1) will indicate a counterclockwise or left most position (COUPLING switches excepted, a one indicates ac).

Adjust Frequency. For Adjust Frequency (AD 0-24999), the setting is a number which corresponds to the CENTER or START frequency in the band analysis modes.

Marker Position. The marker position setting corresponds to a position on the display. For single trace modes of operation, the marker may be programmed to one of 256 horizontal positions. For dual trace operation, the marker may be programmed to one of 128 horizontal positions on the selected trace.

## B. Delimiters.

Delimiters are not needed, but if desired, commas, spaces, upper or lower case alphanumerics can be used.

## NOTE

The last character needs to be followed by a CRLF, space, or a comma. For example, the 9825A automatically sends this information if the wrt statement is used. If the cmd statement is used, these additional characters must be supplied. Spaces following characters will not affect the messages sent, except for the write alphanumerics (WTA) command which requires the output string of characters to have a fixed number of characters (32) and may consist of spaces and/or alphanumeric characters.
-hp- 9825A

Example: wrt711,"prs, ad442,ac1"
wrt711,"PRSAD442AC1"

## II. SPECIAL FRONT PANEL COMMANDS.

Special commands are useful when it is desirable to set the front panel controls for a particular mode of operation. Special sequences are useful when data is being transferred between the 3582A and a controller.

## A. Preset.

The preset (PRS) command places the 3582A front panel controls in a mode which is equivalent to that in the Turn-On Procedure. If the 3582A instrument appears to be "hung up" due to an inadvertant programming error, sending the PRS command will often return the instrument to an operating status. Furthermore, it is a good programming practice to "initialize" the front panel controls of the 3582A using the PRS command before entering an extensive programming sequence. See the Command List for the PRS switch settings.

## B. Setting the Marker.

The marker position command (MP) combined with a marker position number ( $0-255$ or $0-127$ ) sets the marker horizontal position on the display. The marker position may be determined by the following equations:

$$
\text { MARKER POSITION }=\frac{250\left(\text { or } 125^{\circ}\right)}{\text { SPAN }} \times(\mathrm{fm}-\mathrm{fs})
$$

$\begin{array}{ll}\text { Where: } & \mathrm{fm}_{\mathrm{m}}=\text { Desired marker frequency } \\ & \mathrm{fs}_{\mathrm{s}}=\text { START FREQUENCY or }\end{array}$ CENTER FREQUENCY - ( SPAN

- NOTE

The marker has 128 positions for each trace in dual mode.

Note that on larger spans and dual trace operation, the marker position (derived from the equation) will not be an integer for some frequencies. In this case, round the marker position to the nearest integer number.

## III. INSTRUMENT DATA OUTPUT.

The listing commands are used to read control or display data from the 3582A. The general form for initiating a list command requires that the list command be given by the controller which sets the 3582A in a "talk" mode. The 3582A will then output data, as specified by the list command, to the controller which must then be programmed to the "listen" mode.

## A. Listing Control Settings.

The position of some front panel control settings, in decimal or exponential format, may be read by the controller through the following list commands:

## Command

## Description

LAD List frequency adjust value NNNNN.NN CRLF
LMK List marker amplitude and frequency $\pm$ NNNNNE $\pm$ NN, NNNNN. NNN CRLF
LSP List span (Hz) NNNNN CRLF
LAS List channel A sensitivity
LBS List channel B sensitivity $\pm$ N.NNE $\pm$ NN CRLF
LXS List Transfer Function sensitivity
Notice that all of the list commands above, except LMK, require one variable in which to store the data in the controller. The LMK instruction requires two variables in which to store data, and both must be available when the LMK command is given. The sensitivities obtained by the LAS, LBS, and LXS commands are the same as those indicated on the display and are the total of the SENSITIVITY switch setting and the AMPLITUDE REFERENCE LEVEL switch setting. The units are either volts or dBV as determined by the LOG/LINEAR switches.

## Program Examples.

List frequency adjust value (LAD).


List marker amplitude and frequency (LMK).


List span (LSP).

D: "program to demo LSF common d":
1: fxd 1/urt. 711, "LSP"
2: red 711, A: prt A:dSp "SPAN
$=*, A$
3: lel 711iend
$+323$

List channel A sensitivity (LAS).

B. Listing Display Data. The display graphics or the display alphanumerics may be listed using the following instructions:

Command
Description
LDS List display (128, 256, or 512 points in corresponding units) each point $\pm$ N.NNE $\pm$ NN separated by commas; CRLF
LAN List alphanumerics (128 ASCII characters, CRLF; representing the four 32 character lines)

The LDS instruction causes the 3582A to output data from the display in three different quantities. The number of points which are ouputted depends upon the particular mode of operation the instrument is in when the LDS command is received as the following table illustrates.

LDS Points Returned.

| Mo. of Points |  |
| :---: | :---: |
| 128 | Single trace in dual channel mode |
| 256 | 1. Single trace in single channel mode |
|  | 2. Dual trace in dual channel mode (128 points for channel A |
|  | followed by 12B points for channel B$)$ |
| 512 | Single trace time in single channel mode |

The points are outputted in corresponding units. That is, the SCALE and SENSITIVITY will determine the type of units and the relative magnitude. However, the magnitude of the time points are determined by the SENSITIVITY setting alone. Each group of ASCII coded characters is separated by commas with the CRLF sent after the last point.

Note that if the display is listed when the instrument is in the UNCAL (uncalibrated) mode, the units which are output will be different than when the instrument is in the CAL mode as follows:

Output Units.

| Funtion | CAL | UNCAL |
| :---: | :---: | :---: |
| Amplitude | dBV (log) Volts (lin) | 0 to 1 |
| Time | - 1 to + 1 | 0 to 1 |
| Phase | -200 to + 200 | 0 to 1 |
| Transfer Function |  | dB |

## Program Example.

List display points (LDS).


The LAN (list alphanumerics) instruction causes the 3582A to output 128 ASCII coded characters which represent the four alphanumeric display lines. Note that some symbols such as $\sqrt{ }$ (square root) do not have an ASCII equivalent and may require conversion to another code form. The following gives the displayed character and the ASCII equivalent which is sent or received over the HP-IB.

Display-ASCII Equivalents.


## Program Example.

List alphanumerics (LAN).


## IV. INSTRUMENT DATA INPUT.

## A. Writing Alphanumeric Messages.

Alphanumeric messages may be written into any of the four alphanumeric lines on the display through the use of the following instruction:

## WTA 1-4, 32 ASCII Characters

select line 1, 2, 3, or 4 Use blanks to fill up remaining spaces to total 32 .

The first part of the instruction (WTA) should be followed immediately by a line number and a comma. The next 32 characters are reserved for the text of the message. For example, to write "A COSINE SPECTRUM" on line 1 of the display, the command and message would appear as follows ( $\Delta$ means space):

## "WTA1, $\Delta \Delta \Delta \Delta \Delta \Delta \Delta A \Delta$ COSINE $^{2}$ SPECTRUM $\Delta \Delta \Delta \Delta \Delta \Delta \Delta \Delta$ "

## NOTE

The text of the message must have at least 32 characters or the 3582A will not display the message and will appear to be "hung up" while waiting for the completion of the message.

## Program Example.

Write alphanumerics (WTA).


## V. WORKING WITH MEMORY.

The RAM (Random Access Memory) contents are completely accessible via the HP-IB. Data in memory is stored in a binary format consisting of 16 bit words. But information is transferred over the HP-IB in 8 bit bytes, therefore, two bytes are required to transmit or receive memory word.

## A. The Binary Format.

In order to work with memory data directly, it is important that the binary format of words be understood. The words themselves indicate a magnitude for numerics or a particular
code for alphanumerics. There are no units indicated in a numeric word and the word is simply a 2 's complement binary number with an equivalent decimal range of from -32768 to +32767 as shown.

Words in Memory.


In the display section of memory, numerics and alphanumerics are mixed together and require a decoding procedure if they are to be interpreted by a controller program as binary data. This will generally not be necessary since the List Display commands perform the decoding operations and transmit the words in ASCII format.

When binary data is transmitted over the bus between the controller and the 3582A, the most significant byte of a 16 bit word is sent first followed by the least significant byte.

## B. Memory Instructions.

There are two instructions for working with binary memory data. These commands are primarily for the advanced user who wishes to input his own time record or display or to do special processing:

## Command Description

LFM,M,N List from memory
WTM,M,N Write to memory
Where: $\quad M=$ Start address (octal)
$\mathrm{N}=$ Number of words to be transferred (decimal)
Data is in 2 N 8 bit bytes, most significant byte first

These memory instructions are transmitted via the HP-IB in ASCII format. The controller must be programmed to take the appropriate action directly after the instruction is sent with no intervening messages. Each instruction requires that the memory location (in octal) be specified. For example, if a time record is to be entered into the 3582A for processing, the instruction would appear as follows:

$$
\text { WTM,70000, } 1024
$$

## NOTE

The 3582A starts accepting or sending binary data after the LF character is sent. The CRLF is automatically sent by the 9825A if the wrt command is used. When the LFM or WTM instruction is used, a $C R$ or $L F$ is not sent by the 3582 A after the binary string, nor is it looked for after a binary string is received from the controller.

After the instruction is given, the controller may send the data as a character string or as individual bytes.

## C. Memory Locations.

The principal memory locations of interest are given as follows:

|  | Start <br> Address <br> Description | (M, octal) $)$ | Number <br> of Words <br> (N, decimal) | Binary Format |
| :--- | :---: | :---: | :---: | :---: |

## VI. INSTRUMENT SIGNAL PROCESSING CONTROL AND STATUS.

## A. Service Request.

Service Request (SRQ) is set only as a result of syntax errors caused by improper HP-IB commands. It is cleared by a DEVICE CLEAR or cleared as the result of a SERIAL POLL. When cleared, the five bit status byte returned will always consist of zeros.

## B. Status Word.

The status word may be used to determine what operational state the 3582A is in. The eight bit status word contains the following information:
\(\left.$$
\begin{array}{ccl}\text { Bit } & \text { Value } & \text { Meaning } \\
0 & 1 & \begin{array}{l}\text { Diagnostic on screen. Indicates current switch } \\
\text { setting is invalid. Set and cleared by 3582A. }\end{array} \\
1 & 2 & \begin{array}{l}\text { Arm light is on. Set and cleared by 3582A to } \\
\text { agree with arm light on front panel. }\end{array} \\
2^{*} & 4 & \begin{array}{l}\text { A overload. Set by 3582A when } \\
\text { 1. Time record is moved to FFT area or } \\
\text { time record is complete }\end{array}
$$ <br>

2. and hardware overload has occurred\end{array}\right\}\)| 3. and A or BOTH INPUT MODE |
| :--- |

## NOTE

The Status Word is not the same as the HP-IB STATUS BYTE. The STATUS BYTE returned as the result of a serial poll will be zeros since the only reason for an SRQ from the 3582A is incorrect HP-IB commands.

The two commands for obtaining a status word are: Command

Description
LST1 Reads status word
LST0 Reads status word and then resets*

As with many other HP-IB commands, the controller first gives the command and then reads the returning byte into a variable for decoding. The LST0 command resets the starred bits after they are read so that new information may be entered on the next machine cycle.

## Program Example.

List status word (LST).

> Q: "Frogram to
> 1: moct: $f \times \mathrm{xd} \mathrm{g}$ :
> hrt 711 "LST1.
> 2: dserab(711)t
> 1c1 711:End
> +9201

```
Hy%}\frac{dem}{d
```


## C. Processor Control Commands.

There are two processor control commands which can be used to improve data transfer rates when large blocks of data are transmitted.

Command Description

## HLT Unconditional halt at next HP-IB branch point

 RUN Unconditional runWithout the use of these commands, the processor handles the HP-IB in an interrupt mode of operation. When the HLT command is given, the processor is stopped which allows practically direct memory access without unnecessary time delay. After the data is transferred, the processor may be returned to normal operation by giving the RUN command. However, no momentary buttons are processed when the processor is in the HLT mode.

## VII. EXAMPLE FLOWCHARTS AND PROGRAMS.

## A. Loading a Time Record Into Memory.

The following flowchart presents the fundamental steps needed to load a time record into memory in the baseband $0-25 \mathrm{kHz}$ mode. The time record should consist of 1024 data points with each point being a 16 bit 2's complement number (other magnitude ranges will require scaling). The example flowchart includes scaling for a function which has a range between +1 and -1 and also conversion of the scaled number to an integer.

## Storing a Time Record in Memory.



## Program Example: Writing to Memory.

Write to memory (WTM).

```
0: arosram to 
        demo WTM comman
        d":
    1: radiurt 711,
    TTA1
    2: mdecidim f[10
        24]
    3: for I=1 to
    1024
    4: 20000*cos (2\pi%
        (I-1)/256)}->\textrm{A}[1
    5: next I
6: fmt 1,"WTM.
    70000,1024"
7: wrt >11.1
8: beep
9: for I=1 to
    1 0 2 4
10: wtb 731:Shf(
    A[I],8)
11: wtb 731,bond
    (255,A[I])
12: next I
13: beep
14: end
*9460
```


## B. Reading Binary Data From Memory.

The following flowchart presents the fundamental steps needed to read data from memory. A very useful function, derived from this operation, is the storage of data for long periods of time. Remember that if the 3582A is turned off, all data in RAM is lost. As an example, switch settings, time records, or the entire display may be stored in the controller and then later written back into the 3582A memory (using a technique similar to entering a time record but without the need for scaling since the data itself is merely being stored and not operated on). The example flowchart includes scaling* but this step may be skipped if the data is only to be stored.

## Reading Binary Data From Memory.



* Only Necessary If Data Is Operated On.


## C. The Learn Mode.

One method of programming the instrument is to use the PRS (preset) command and then program the control settings as necessary. Another method involves the Learn Mode. To use this method, the instrument controls are set up manually in the LOCAL mode of operation. The switch settings may then be stored in the controller by accessing the five switch registers using the LFM (list from memory) command. At a later time when it is desirable to duplicate the same switch settings, the controller may write the switch settings back into the five switch registers using the WTM (write to memory) command.

## Program Example: The Learn Mode (reading and

 writing to memory).Learn mode.


HP-IB Command List.


HP-IB Command List (Cont'd).

| Group | Command |  | Description |
| :---: | :---: | :---: | :---: |
|  | Function | Setting |  |
| Display | MB | 0-1 | Marker / $\sqrt{\text { BW }}$ |
|  | MT | 0-1 | Marker Trace |
|  | MF |  | Marker Set Freq ${ }^{\text {Marker }}$ ( 127 for dual channell |
|  | MP | 0-255 | Marker Position (0-127 for dual channel) |
|  | AA | 0-1 | Amplitude A |
|  | AB | 0-1 | Amplitude B |
|  | AX | 0-1 | Amplitude Transfer Function |
|  | SC | 1 | Scale Linear |
|  | SC | 2 | Scale $10 \mathrm{~dB} /$ Div. |
|  | SC | 3 | Scale $2 \mathrm{~dB} /$ Div. |
|  | PA | 0-1 | Phase A |
|  | PB | 0-1 | Phase B |
|  | PX | 0-1 | Phase Transfer Function |
|  | TA | 0-1 | Time A |
|  | TB | 0-1 | Time B |
|  | CH | 0-1 | Coherence |
|  | AM | 1-9 | Amplitude Ref. Level (Add - 10 dB per step, $2=-10 \mathrm{~dB}, 9=-80 \mathrm{~dB}$ ) |
| Passband Shape | PS | 1 | Flattop |
|  | PS | 2 | Hanning |
|  | PS | 3 | Uniform |
| Average | AV | 1 | Off |
|  | AV | 2 | RMS |
|  | AV | 3 | Time |
|  | AV | 4 | Peak |
|  | RE |  | Restart |
|  | NU | 1 | Number 4/64 |
|  | NU | 2 | Number 8/128 |
|  | NU | 3 | Number 16/256 |
|  | NU | 4 | Number 32/Exp |
|  | SH | 0-1 | Shift |
| Trace | TS |  | Trace 1 Store |
| Storage | TR | 0-1 | Trace 1 Recall |
| \& | RS |  | Trace 2 Store |
| Recall | RR | 0-1 | Trace 2 Recall |
| X-Y | PL |  | X-Y Plot |
| Recorder | UL |  | 1-Lower Left \& Reset) <br> $\rightarrow 1$ (Upper Right) |

Special Commands

| Group | Command | Description |
| :---: | :---: | :---: |
| Listing Commands | LAD LMK LSP LAS LBS LXS LDS LAN | List frequency adjust value NNNNN.N CRLF <br> List marker amplitude and frequency $\pm$ N.NNNE $\pm$ NN, NNNNN CRLF <br> List span (Hz) NNNNN CRLF <br>  <br> List display $(128,256$, or 512 points in corresponding units) each point $\pm$ N.NNE $\pm$ NN separated by commas; CRLF List alphanumerics (128 ASCII characters, CRLF; representing the four 32 character lines) |
| Binary Memory I/O | LFM,M,N WTM,M,N | List from memory <br> Write to memory <br> $\mathrm{M}=$ Start Address (Octal) <br> $N=$ Number of words to be transferred (decimal) <br> Input is in 2N 8-bit bytes <br> Most significant byte first |
| Writing Display Alphanumerics | $\begin{gathered} \text { WTA } 1-4, \\ 32 \text { ASCII } \\ \text { Characters } \end{gathered}$ | Inputs a 32 character string to alpha line 1 to 4 (top to bottom) of display. Use blanks where needed to complete 32 character count. |
| Processor Control | HLT <br> RUN | Unconditional halt at next HP-IB branch point <br> Unconditional run |
| Status <br> Word | $\begin{aligned} & \text { LST0 } \\ & \text { LST1 } \end{aligned}$ | List status word <br> * (LSTØ Resets Bits After Reading) |

## Special Commands (Cont'd).

| Group | Command | Description |  |
| :---: | :---: | :---: | :---: |
|  |  | $5^{*} \quad 32$ $\begin{array}{lc} 6^{*} & 64 \\ 7^{*} & 128 \end{array}$ | ingle sweep spectrum complete. Set wen time complete data has been $\mathrm{FFT}^{\prime D}$ and displayed. Use LST1 to check this lag! It depends on internal flags which are leared by LST0. <br> verage complete. <br> $X-Y$ plot complete. |
| Preset | PRS | Preset command <br> Causes instrument to go into the following control state: <br> ( $25 \mathrm{kHz}, 1$ channel) |  |
|  |  | Switch | Setting (when applicable) |
|  |  | Coupling <br> Input Mode <br> Sensitivity <br> Level <br> Repetitive <br> Arm <br> Trigger Slope <br> Marker <br> Marker Relative <br> Marker $\div \sqrt{B W}$ <br> Mode <br> Span <br> Amplitude <br> Scale <br> Phase <br> Time <br> Coherence <br> Amplitude Ref Lev <br> Passband <br> Average <br> Average Number <br> Average Shift <br> Trace 1 Store <br> Trace 1 Recall <br> Trace 2 Store <br> Trace 2 Recall | AC (Channels A \& B) Channel A <br> 30 V (Channels A \& B) <br> Free Run <br> On <br> Off <br> Off <br> Off <br> Off <br> 0-25 kHz Baseband <br> 25 kHz <br> A (B\&XFR-OFF) <br> $10 \mathrm{~dB} / \mathrm{Div}$ <br> None <br> None <br> Off <br> Normal <br> Flat Top <br> Off <br> 4 <br> Off <br> Off <br> Off <br> Off <br> Off |

Memory Locations.

| Description | Start Address <br> (M, Octal) | Number of Words <br> (N, Decimal) | Binary Format |
| :--- | :---: | :---: | :---: |
| Time Record | 70000 | 1024 | Numeric <br> Display |
| 74000 | 512 | Alphanumeric |  |
| Front Panel | 77454 | 5 | Numeric |
| Switches |  |  |  |

## SECTION IV

## PERFORMANCE TESTS

### 4.1. INTRODUCTION.

4-2. The Performance Test section is divided into three parts:
a. Part I is the Operational Verification which uses common manually operated test equipment to check the 3582A against selected specifications to yield a high ( $95 \%$ ) confidence level of instrument performance. This test should be used after minor repairs are made and for incoming inspection. An Operational Verification Test Card is located at the end of this section.
b. Part II is the Automated Performance Test which uses a calculator to run a fully automatic and a semi-automatic test that entirely checks the 3582 A against specifications. This test takes approximately four hours to complete and requires HP-IB compatible test equipment.
c. Part III is the Manual Performance Test which fully checks the 3582A against specifications using common manually operated test equipment. Note however, that because of its reiterative nature, the test takes approximately $91 / 2$ hours to finish. This test is not as complete as the automatic test.

## SECTION IV PART I OPERATIONAL VERIFICATION

## 4-3. OPERATIONAL VERIFICATION.

4-4. The following set of tests check selected specifications in their worst-case condition to provide a relatively short but high ( $\mathbf{9 5 \%}$ ) confidence level verification for proper operation of the 3582A. This verification should be used for incoming inspection and instrument check out after a minor repair has been completed.

## 4-5. Required Test Equipment.

4-6. If the recommended equipment is not available, equipment meeting the critical specifications given in Table 4-1 may be substituted. Listed in Table 4-2 are recommended test accessories.

### 4.7. Preset.

4-8. Preset refers to a mode in which the 3582A front panel switches should be set prior to the initiation of each test sequence. The switch settings are given (line switch excepted) on Page 4-2.
4-9. Instrument Warmup.
4-10. Before any of the Operational Verification tests are performed, be sure that all equipment associated with the test is functioning within specified operating limits. The 3582A requires at least 30 minutes of warmup before any test is performed.
Button Positions: - ON OFF
Set both framed buttons. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ON
Set AMPLITUDE A. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ON
Set SCALE..................................................... . $10 \mathrm{~dB} / \mathrm{DIV}$
Set PASSBAND SHAPE . . . . . . . . . . . . . . . . . . . . . . . . . . . FLAT TOP
Set AVERAGE NUMBER 4.......................................... . . ON
Set all other buttons................................................. OFF
AMPLITUDE REFERENCE LEVEL. . . . . . . . NORM (Position 1)
FREQUENCY MODE. . . . . . . . . . . . . . . . . . . . . . . . . . . . . $0-25 \mathrm{kHz}$
SPAN................................................................. 25 kHz
TRIGGER LEVEL. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . FREE RUN
INPUT CHANNEL A SENSITIVITY.................. +30 dBV
VERNIER....................................................... . . . CAL
INPUT CHANNEL B SENSITIVITY................... +30 dBV
VERNIER.......................................................... . . CAL
INPUT MODE............................................................ . A

Table 4-1. Recommended Test Equipment for Operational Verification.

| Test | Instrument | Critical Specification | Recommended Modal |
| :---: | :---: | :---: | :---: |
| Amplitude <br> Accuracy and <br> Flatness | Sine wave source | Amplitude accuracy of $\pm 0.2 \mathrm{~dB}$, flatness $(1 \mathrm{kHz}-25 \mathrm{kHz})$ $\pm 0.1 \mathrm{~dB}$ output $\geq 3.2 \mathrm{~V}$ rms into $50 \Omega$ | $\begin{aligned} & \text {-hp- 3330B Opt. } 005 \\ & \text { or } \\ & \text {-hp- 3320B } \\ & \text { or } \\ & \text { hp- 3325A Opt. } 002 \end{aligned}$ |
| Harmonic Distortion | Sine wave source | All harmonics down at least 80 dB from the fundamental | -hp- 239A |
| Phase Accuracy | Function Generator | NA | -hp- 3310A <br> -hp- 3311A <br> -hp-3312A <br> -hp- 3325A |
| Common Mode Rejection | Sine wave source | NA | Any recommended signal source. |
| Frequency Accuracy | Sine wave source with counter or Frequency Synthesizer | Frequency accuracy $\pm 0.001 \%$ of setting at 25 kHz | $\begin{array}{\|l} \text {-hp- 3330B Opt. } 005 \\ \text { or } \\ \text {-hp- } 3320 B \\ \text { or } \\ -h p-3335 A \\ \hline \end{array}$ |

Table 4-2. Recommended Test Accessories.

| Description | Pert Mo. (Model Mo.) |
| :---: | :---: |
| Test Leads: |  |
| 112 cm (44 in): dual banana both ends 112 cm (44 in): dual banana to BNC | -hp-Model 1 1000A -hp- Model 11001A |
| Adapters: |  |
| Shielded dual banana to BNC male | Pamona 1555-C-18 |
| Dual banana to BNC male | -hp- Part No. 1251-2277 |
| Dual banana to BNC female | hp-Model 10110A |
| Termination: |  |
| $50 \Omega$ feedthrough | -hp- Model 11048 C |
| $1 \mathrm{k} \boldsymbol{\Omega} \mathrm{1/4W} 5 \%$ | -hp- Part No. 0683-1025 |

4-11. Perform the following steps:
a. Verify that all test equipment is operating under the proper conditions.
b. Connect the 3582A to a suitable power receptacle using the power cord provided with the instrument. DO NOT FLOAT THE 3582A USING A POWER PLUG ADAPTER!
c. Set the 3582A front panel switches to the preset mode and turn the LINE switch to ON.
d. Allow at least 30 minutes of warmup time for the 3582 A before performing any of the Operational Verification tests.

## 4-12. DC BAL Verification.

4-13. Before performing any of the following tests, verify that the DC BAL (offset) is not excessively out of adjustment.

4-14. Perform the following steps:
a. Verify that the 3582A switches are in the preset mode.
b. Short the input terminals of channel A and set the INPUT SENSITIVITY to 10 mV .
c. Press the TIME A button and verify that the trace is at the center horizontal graticule. If it is not, correct its position by adjusting the channel A BAL control.
d. Perform steps $b$ and $c$ for channel $B$ after setting the INPUT MODE switch to $B$, AMPLITUDE A to OFF, and AMPLITUDE B to ON.

## 4-15. ROM Self Test.

4-16. Because the 3582A is highly dependent upon internal firmware for operation, it is recommended that the ROM Self Test be performed before other tests are initiated. If the test fails, refer to Troubleshooting, Section VIII of the Service Manual.

## NOTE

The following test requires that the 3582 A be in the LOCAL mode of operation.

4-17. The ROM self test checks the firmware program stored in each ROM by summing together the data bits in a known binary sequence. This sum is then compared to a known result which is stored in the last two locations in each ROM.

4-18. Perform the following steps:
a. Set AVERAGE NUMBER 32 to ON.
b. Hold AVERAGE RESTART button in while RESET (orange button) is pressed and then released. Release the AVERAGE RESTART button and press and release it again.
c. The test will then begin to run as indicated in the upper left-hand corner of the display by a mnemonic RU.
d. After approximately 5 seconds, the RU will change to OK indicating that the test passed or an ER indicating that the test failed. Press RESET to return the instrument to the normal operating mode.

## 4-19. Display Accuracy.

4-20. The display accuracy test checks the alignment of the trace relative to the CRT graticules.

4-21. Required Test Equipment. None.
4-22. Instrument Control Setup.
a. Enter the Front Panel self-test mode by holding RESTART while pushing and releasing RESET.
b. Select average \#8 and push RESTART. Continue pushing RESTART until test \#2 is displayed.

4-23. Perform the following steps.
a. Move the marker to the second graticule from the left. The lower number in the upper right-hand corner of the display should read between 000021 and 000041 (nominally 000031).
b. Move the marker to the center graticule. The corresponding number should be between 000165 and 000205 (nominally 000175).
c. Move the marker to the second graticule from the right. The corresponding number should be between 000331 and 000351 (nominally 000341 ).

4-24. Calibrator Accuracy.
4-25. This procedure checks the level and flatness of the internally generated "CAL'" signal.
4-26. Required Test Equipment. None.
4-27. Instrument Control Setup.
3582A: Preset

SCALE.......................................................... . . $2 \mathrm{~dB} /$ DIV
CHANNELSENSITIVITY(bothchannels)..................... CAL
4-28. Perform the following steps:
a. Move the marker to 1 kHz . The marker level readout should be $22.0 \mathrm{dBV} \pm 0.2 \mathrm{~dB}$.
b. Set the 1 kHz level as a relative reference by pressing the Marker SET REF button first and the REL button next. Using this relative reference, measure the amplitudes of all other harmonically related spectra displayed (i.e., $2 \mathrm{kHz}, 3 \mathrm{kHz}$, etc.). The levels should be within $\pm 0.3 \mathrm{~dB}$ of the 1 kHz relative reference level.
c. Repeat Steps a and b for channel B after setting the INPUT MODE switch and AMPLITUDE switch for channel $B$ readings.

## 4-29. Amplitude Accuracy and Flatness.

4-30. This procedure checks the amplitude accuracy and flatness at selected cardinal points
in amplitude and frequency. These points exhibit a worse case condition due to the accumulated errors throughout the instrument. Passing this test assures that all other points are at least as accurate as these points.

## 4-31. Required Test Equipment.

-hp- 3330B Option 005 or 3320B Synthesizer or 3325A Synthesizer/Function Generator Compatible shielded (coax) interconnecting cables with appropriate adapters
Termination: $\mathbf{5 0}$ ohms

## 4-32. Instrument Control Settings.

```
3582A: Preset
MARKER
ON
3330B:
FREQUENCY................................................ . . . . . . kHz
AMPLITUDE............................................. . 22.01 dBm
LEVELING(3330B/3320B only). . . . . . . . . . . . . . . . . .FAST (ON)
```

4-33. Perform the following steps.
a. Connect the output of the 3330B to channel A via suitable cables and adapters and terminate in 50 ohms.
b. Verify the amplitude accuracy and flatness by performing the operations indicated in Table 4-3.
c. Connect the 3330 B output to channel B. Repeat Step b for channel B by switching the INPUT MODE switch and AMPLITUDE buttons for channel B.

Table 4-3. Amplitude Accuracy and Flatness.

| Set 3330B <br> AMPLITUDE <br> dBm 50 | Set 3582A <br> SENSITIVITY <br> dBV | Vrms |  | Set 3330B FREQUENCY and <br> read MARKER at frequency <br> $22.5 ~ k H z ~$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 22.01 | +30 | 2.818 | +9 | $+9 \pm 0.5$ | $+9 \pm 0.5$ |
| 22.01 | +10 | 2.818 | +9 | $+9 \pm 0.5$ | $+9 \pm 0.5$ |
| 2.01 | -10 | .2818 | -11 | $-11 \pm 0.5$ | $-11 \pm 0.5$ |

### 4.34. Noise Level.

4-35. The noise level test insures that all noise internal to the analyzer is at least 70 dB below full scale. The test requires a source with a signal-to-noise ratio of at least 80 dB .

## 4-36. Required Test Equipment.

-hp- 239A Oscillator
Compatible shielded (coax) interconnecting cables with appropriate adapters
Termination: $1 \mathrm{k} \Omega 1 / 4 \mathrm{~W} 5 \%$, -hp- Part No. 0683-1025

4-37. Instrument Control Settings.
3582A: Preset
MARKER ..... ON
SENSITIVITY (both channels) ..... $-10 \mathrm{dBV}$
AVERAGE NUMBER ..... 32
FREQUENCY MODE ..... $0-S T A R T$
239A:
OSCILLATOR OUTPUT LEVEL. . . . . . . . . . . . . . . . . . . 0.3 V rms FREQUENCY................................................... . 25 kHz

4-38. Perform the following steps.
a. Connect the oscillator output of the 239 A to channel A of the 3582 A terminated with a $1 \mathrm{k} \Omega$ resistor. Verify that the output level is set at 0.3 V rms and the 3582A SENSITIVITY is set to -10 dBV .
b. Set the 239A output level vernier for a full-scale amplitude on the 3582 without overloading the 3582A. Press AVERAGE RMS and RESTART. The progress of the averaging sequence may be observed by temporarily setting the MARKER ON button to OFF. This will cause the average number to be displayed.
c. Use the marker to verify that all frequencies below 25 kHz have noise less than -85 dBV . Then set the AVERAGE to OFF.
d. Set the 239A output to 3 mV rms. Set the 3582A INPUT SENSITIVITY to -50 dBV .
e. Repeat Steps $b$ and $c$ verifying that the noise levels are less than -120 dBV .
f. Set the 3582A SPAN to 500 Hz and repeat Steps d and e to check for line related noise.
g. Repeat Steps a through f for channel B.
h. Set the 3582A SPAN to 25 kHz , MODE to SET CENTER, and INPUT SENSITIVITY to -10 dBV . Set the FREQUENCY ADJUST control for a center frequency of 5001 Hz . Set AVERAGE to OFF.
i. Set the 239A FREQUENCY to 5 kHz and the output to 0.3 V rms .
j. Repeat Steps $b$ through e verifying that all non-harmonically related noise (do not include 0 Hz and negative frequencies) is within the stated limits. This test checks for Digital Local Oscillator spurs.

### 4.39. Harmonic Distortion.

4-40. The harmonic distortion test checks for harmonically related signals which are generated within the instrument when a full scale input is present. To perform this test requires a signal source which has a signal with harmonic distortion products less than -80 dB below the fundamental.

## 4-41. Required Test Equipment.

-hp- 339A Distortion Measuring Set or 239A Low Distortion Oscillator Compatible shielded (coax) interconnecting cables with appropriate adapters

## 4-42. Instrument Control Settings.

3582A: Preset
SPAN ..... 50 Hz
SENSITIVITY (both channels) ..... 0 dBV
AVERAGE NUMBER ..... 8
AVERAGE ..... OFF
FREQUENCY MODE ..... 0-START
MARKER ..... ON
239A:
FREQUENCY ..... 10 Hz
OSCILLATOR OUTPUT LEVEL ..... 1.0 V

4-43. Perform the following steps.
a. Connect the output of the 239A to the channel under test via suitable cables and adapters.
b. Set the MARKER POSITION to 10 Hz and adjust the 239A output level for a full scale display without overloading the 3582A. (This can be done faster with a SPAN of 500 Hz .) Set AVERAGE to TIME and 30B to channel A via suitable cables and adapters and terminate in 50 ohms.
c. Set the 3582A AMPLITUDE REFERENCE LEVEL to position 2 (NORM is position 1) and press AVERAGE RESTART.
d. After the average is complete (this takes about 40 seconds), move the marker to the second harmonic. The amplitude of the second harmonic should be less than -70 dB below full scale.
e. Repeat Step d for the third harmonic.
f. Repeat Steps b through e for the other channel after switching the INPUT MODE switch and AMPLITUDE buttons, resetting the AMPLITUDE REFERENCE LEVEL to NORM, and setting AVERAGE to OFF.

### 4.44. Common Mode Rejection.

4-45. The common mode rejection test verifies the capability of the 3582A to ignore a signal which appears simultaneously and in phase at both input terminals of a single channel.

## 4-46. Required Test Equipment.

Any recommended signal source
Compatible shielded (coax) interconnecting cables with appropriate adapters

4-47. Instrument Control Settings.

```
3582A: Preset
MARKER........................................................ . . ON
```



```
SPAN........................................................... . . . Hz
3330B (3320B):
AMPLITUDE. ...........................................4V)26.89 dBm
FREQUENCY............................................... . . 50 Hz
LEVELING(3330B or 3320B only). . . . . . . . . . . . . . .SLOW (ON)
```

4-48. Perform the following steps.
a. Switch the 3582A ISOL-CHAS switch to ISOL and connect the 3330B output, without a load, to the input of the 3582 A channel A .
b. Using the MARKER POSITION control, set the marker to 50 Hz and press the MARKER SET REF button.

## NOTES

1. If not using a Synthesizer, adjust Oscillator frequency.
2. The NOISE SOURCE OUTPUT BNC connector may be used for a chassis ground.
c. Disconnect the 3330B at the input terminal of channel A. Short the input terminals together. Connect the "high" side of the 3330B output to the shorted connection (input terminals) and the "low'" side of the 3330B output to the 3582A chassis.
d. Switch the 3582A SENSITIVITY to +10 dBV and press the MARKER REL button. The amplitude reading should be less than -66 dB .
e. Repeat Steps a through d with the 3330B FREQUENCY set to 60 Hz . The reading in Step d should be less than -64 dB .
f. Repeat Steps a through e for channel B by setting the INPUT MODE switch and AMPLITUDE switches for channel B.
g. Disconnect the signal source from the input terminals.
h. Set ISOL-CHAS switch to CHAS.

### 4.49. Frequency Accuracy.

4-50. The frequency accuracy test checks the frequency measuring capability in the band analysis (SET START, SET CENTER) mode under narrow bandwidth conditions.

## 4-51. Required Test Equipment.

-hp- 3330B or 3320B or 3325A Synthesizer
Compatible shielded (coax) interconnecting cables with appropriate adaptersTermination: 50 ohms
4-52. Instrument Control Settings.
3582A: Preset
SENSITIVITY (both channels) ..... 0.3 V
SPAN ..... 5 Hz
FREQUENCY MODE SET CENTER
FREQUENCY ADJUST ..... 25 kHz
MARKER ..... ON
SCALE ..... LINEAR
3330B:
FREQUENCY ..... 25 kHz
AMPLITUDE ..... 2.05 dBm
LEVELING(3330B/3320B only) ..... FAST
4-53. Perform the following steps.
a. Connect the output of the 3330 B to input channel A of the 3582 A using a 50 ohm termination.
b. Using the MARKER POSITION control, set the marker to the maximum amplitude of the 25 kHz signal spectra. The marker frequency displayed should be $25000 \mathrm{~Hz} \pm 0.5 \mathrm{~Hz}$.
c. Repeat Steps $a$ and $b$ for channel B by setting the INPUT MODE switch and AMPLITUDE switches for channel B.

### 4.54. Phase Accuracy.

4-55. The phase accuracy test checks the phase accuracy by comparing the phase spectral components associated with the harmonics of a triangle wave input.

## 4-56. Required Test Equipment.

-hp- 3312A or 3325A Function Generator
Compatible shielded (coax) interconnecting cables with appropriate adapters

## 4-57. Instrument Control Settings.

3582A: PresetSENSITIVITY (both channels)0 dBV
FREQUENCY MODE SET CENTER
SPAN ..... 1 kHz
FREQUENCY ADJUST ..... 2750 Hz
MARKER .....  ON
3312A:
AMPLITUDE ..... 1 V
RANGE ..... 1 kHz


4-58. Perform the following steps.
a. Connect the output of the 3312 A to the inputs of channels A and B using appropriate cables and adapters.
b. Adjust the frequency of the 3312A to place the fundamental at the center graticule ( $2750 \mathrm{~Hz} \pm 20 \mathrm{~Hz}$ ). Adjust the 3312 A amplitude output to place the amplitude of the fundamental within 3 dB of full scale.
c. Set the 3582A AMPLITUDE A to OFF and the PHASE A to ON. Set the FREQUENCY MODE to $0-25 \mathrm{kHz}$ and the TRIGGER SLOPE to - .
d. Adjust the TRIGGER LEVEL until the phase spectra of the harmonics are as near to zero degrees as possible. Use the MARKER to verify that the center of the sloping portion of the phase components are between $\pm 10^{\circ}$. If they are not, repeat the TRIGGER LEVEL SETTING. Set the TRIGGER REPETITIVE button to OFF.
e. Using the MARKER POSITION control, set the marker to the center of the sloping segment of the phase spectra of the 5th harmonic. Press the MARKER SET REF button.
f. Put the TRIGGER back into the REPETITIVE mode. Press the MARKER REL button and check that the relative phase variation is less than $\pm 10^{\circ}$.
g. Repeat Steps d through for channel B by setting the INPUT MODE switch and PHASE switches for channel B. Set the MARKER REF to OFF.

### 4.59. Amplitude and Phase Match Between Channels.

4-60. The amplitude and phase match between channels should be within the given tolerances so that comparative functions such as Transfer Function and Coherence will be accurate.

## 4-61. Required Test Equipment. None.

## 4-62. Instrument Control Settings.

3582A: Preset
SENSITIVITY (both channels) ..... $+10 \mathrm{dBV}$
INPUT MODE ..... BOTH
AMPLITUDE XFR ..... ON
AMPLITUDE A ..... OFF
PASSBAND SHAPE ..... UNIFORM
NOISE SOURCE ..... PERIODIC
MARKER ..... ON
AVERAGE TYPE ..... RMS
AVERAGE NUMBER ..... 8

4-63. Perform the following steps:
a. Connect the NOISE SOURCE OUTPUT to the inputs of channels A and B via suitable cables with adapters.
b. Using the MARKER POSITION control, move the marker across the screen noting that each marker amplitude reading does not exceed $\pm 0.8 \mathrm{~dB}$. ( $\pm 0.4 \mathrm{~dB}$, Option 001)
c. Set the AMPLITUDE XFR button to OFF and set the PHASE XFR button to ON.
d. Move the marker across the screen noting that each marker phase reading does not exceed $\pm 5$ degrees. ( $\pm 2$ degrees, Option 001)

## SECTION IV PART II

## AUTOMATED PERFORMANCE TEST

### 4.64. INTRODUCTION.

4-65. The Automated Performance Test uses equipment controlled via the Hewlett-Packard Interface Bus (HP-IB) by a 9825A Calculator. A portion of the test uses the calculator to prompt an attendant for performing manual operation of non HP-IB equipment. These tests provide a quick and efficient means to verify that the 3582A meets performance specifications.

### 4.66. APPLICABILITY.

4-67. The Automated Performance Test takes approximately four hours to run and should be used only when complete specification testing is required. For incoming inspection and testing after small repairs are made, the Operational Verification, given in Section IV Part I is recommended.

### 4.68. THE TAPE CARTRIDGE.

4-69. A tape cartridge (3582A/9825A Test Cartridge) is available with the manual for use in the 9825A Calculator. Do not attempt to use this cartridge with other controllers, since the incompatibility may result in the erasure of data on the tape. The part number of the tape cartridge is 03582-10002.

### 4.70. Cartridge Organization.

4-71. The cartridge contains an HP-IB Verification, a short adjustment program and Performance Tests.

4-72. The Performance Tests are divided into two groups: Semi-Automatic and Automatic. Subroutines for each group are contained in relatively large files with tests within the group on individual files. When a test is to be run, the test program is loaded into the subroutine file after the subroutines.

4-73. For each test, the Special Function keys (f0-f11) on the calculator select the test to be run by loading the appropriate file. Thus the user does not need to know file numbers beyond those of the subroutines. Key overlays are included to define the keys. If these aren't available, the key functions can be listed at the start of each performance test group.

4-74. As an example, say that you wish to check Harmonic Distortion. This test is in the Semi-Auto group (test listings are in Table 4-5.) The first thing to do is load the subroutine file. From the list below, this is File 3. After File 3 is loaded, it is run to initialize and dimension variables, and to identify the instrument by serial number. When this has been completed, the display will instruct the operator to "PRESS f-KEY FOR TEST DESIRED." From the overlay or Table 4-5, this is f 3 . When this test has run, "END" will be displayed and another test can be run in the same fashion.

4-75. Tape contents are listed below. Note that either an -hp- 3330B or 3325A can be used as the test synthesizer. Track 1 is written for the 3330B while track 0 is written for the 3325A.

Track 0:3325A Track 1:3330B
File 0: Contents
File 1: HP-IB Verification
File 2: Basic Adjustments
File 3: Semi-Auto Subroutines
File 4: Auto Subroutines
File 5: Key File (Semi-Auto)
File 6: Key File (Auto)
File 7-18: Test Files (Semi-Auto)
File 19-31: Test Files (Auto)
4-76. The Semi-Auto Test is calculator based, but requires an attendant to change inputs, etc. The Auto Test is fully automatic and should not require attention once it has started. The Semi-Auto Test will typically take a little over an hour while the full Auto Test takes about $21 / 2$ hours.

## NOTE

For complete testing, BOTH the Semi-Auto and Auto Tests must be performed.

### 4.77. EQUIPMENT REQUIRED.

4-78. The equipment required for performing these tests and adjustment is given in Table 4-4. Note that other than the allowance for two different synthesizers, there is no real provision for using other than the specified equipment without extensive program modification.

4-79. One exception would be that a different printer (e.g. -hp-9871A) can be used with modification only to the "wrt" statements. The modification will probably include at least address changes and may include the addition of "wait" statements if a relatively slow printer (such as the 9871 A ) is used.

4-80. The following points concerning test equipment should be noted:
a. A separate printer is required only if test data is to be printed out. The tests can be run on a pass/fail basis that uses the 9825A's printer.
b. A function generator is required only if the 3330 B is used as the synthesizer since the 3325 A is a synthesizer/function generator.
c. For the performance tests, almost any HP-IB compatible voltmeter can be used (with program modification). In fact, since the voltmeter is used only for the relatively short plotter output tests, which can easily be done manually, an HP-IB voltmeter is not strictly required.

However, for greatest accuracy of calibration for the Adjustment program using the 3325A, a voltmeter with AC accuracy equal to the 3455 A should be used. (Note that the 3455A is required for the 3325A version of the Adjustment Program and use of a different voltmeter will require program modification.)
d. A low distortion oscillator is required for the Semi-Auto Harmonic Distortion Test. The requirement is that all harmonics be at least 80 dB below the fundamental. It may be possible to use a low pass filter to clean up the output of an oscillator for these purposes. The frequencies required are $10 \mathrm{~Hz}, 8 \mathrm{kHz}$ and 12 kHz .

Table 4-4. Equipment Required.

| Instrument | Important Characteristics | Required Model | Use* |
| :---: | :---: | :---: | :---: |
| Calculator | NA | -hp- 9825A (Opt. 001 ) | A, S, P, H |
| Calculator ROMs | String Variable/Advanced Programming | -hp-98210A | A, S, P, H |
|  | Matrix | -hp-98211A | S, P |
|  | General I/O-Extended I/O | -hp-98214A | A, S, P, H |
| HP-IB Interface | NA | -hp-98034A | A, S, P, H |
| Printer Interface | Necessary for Data Print-out | -hp-98032A Opt. 066 | S, P |
| Printer | Necessary for Test Data Print-out. Not Required for Pass/Fail | -hp-9866B | S,P |
| HP-IB Cables | 2 Required, Length Depends on Test Setup | ```hp-10631A (1 meter) -hp- 10631B (2 meters) -hp- 10631C (4 meters)``` | A, S, P |
| Synthesizer | Amplitude Accuracy: $\pm 0.2 \mathrm{~dB}$ at 10 kHz | -hp-3330B <br> (Opt. 004 \& 005) or -hp-3325A (Opt. 002) | A, S, P |
| Digital Voltmeter | AC Accuracy $0.1 \%$ at 20 kHz | -hp-3455A | A, S, P |
| Low Distortion Oscillator | Harmonics $>80 \mathrm{~dB}$ below Fundamenatal | $\begin{aligned} & -h p-339 A \dagger \text { or } \\ & -h p-239 A \end{aligned}$ | A, S, P |
| Function Generator | Required only if 3330 B used as Synthesizer | -hp-3311At or -hp- 3310A $\dagger$ or hp-3312A $\dagger$ | S |
| Terminations | Short-Banana Plug | 1251-2816 w/short | S |
|  | $\begin{aligned} & 1 \mathrm{k} \Omega \text { - Banana Plug (2) } \\ & 1 \mathrm{k} \Omega \text { - Series (2) } \end{aligned}$ | $\begin{gathered} 1251-2816 \mathrm{w} / 1 \mathrm{k} \Omega \\ \mathrm{NA} \end{gathered}$ |  |
|  | 1 MEG Series | NA |  |
|  | 50 Ohm Feedthrough | -hp-11048C $\dagger$ |  |
| Miscellaneous | Shielded Banana Plug | Pomona $1645 \dagger$ | S |

### 4.81. CONNECTING THE TEST EQUIPMENT.

8-82. Using compatible HP-IB cables, connect the test equipment as shown in Figure 4-1. Check that each cable connector is securely mounted to the appropriate mating connector and that mounting fasteners are firmly screwed into place.
\{CAUTION\}

Excessive leverage placed on stacked connectors may result in damage to the HP-IB receptacle on the rear panel of an instrument.


Figure 4-1. HP-IB Connection Diagram.

### 4.83. GENERAL CONSIDERATIONS.

### 4.84. Warm-up Time.

4-85. Thirty minutes should be sufficient for warm-up. Note that the DC offsets will change as the instrument warms up so this adjustment should be done only after 30 minutes.

## 4-86. Order Of Testing.

4-87. Tests and adjustments should be carried out in the order which they appear on the tape unless only some specific parameter is to be tested. The idea here is to test first those things that will prevent further testing (HP-IB Verification) or are most likely to fail and make further testing ill-advised.

4-88. Note that the Adjustment procedure can be quickly carried out with the covers on to check amplitude and frequency calibration. Note also that the first two tests in the Semi-

Auto group are Noise Floor and Harmonic Distortion. If there is a malfunction in the instrument, these two tests are the most likely to fail.

### 4.89. Operator Instructions.

4-90. Operator actions are prompted by the 9825A's display. When an instruction is given, the calculator will "beep" and stop program execution until CONTINUE is pressed. There will be times (e.g. during long calculations) when nothing seems to be happening. In these cases, let the 9825A's red 'run light'' be your guide. If the light is not on the program has either ended (in which case "END" should be displayed) or has given an instruction and is waiting for CONTINUE to be pressed. If the light is on, be patient. A subroutine is provided to inform the operator of an error in execution.

## 4-91. Print Mode.

4-92. At the beginning of each performance test (Semi-Auto and Auto), the operator will be asked to select the Print Mode. This is accomplished by pressing special function key f0 until the desired mode is displayed and then pressing CONTINUE.

The Print Modes are as follows:
a. Print All: Prints all data on 9866B.
b. Print Errors: Prints only error data on 9866B.
c. Print Pass/Fail: Prints Pass/Fail on 9825A's Printer.

### 4.93. Channel Selection.

4-94. There will be times when it is desired to test only one channel. This is easily accomplished by using special function key f17 (shifted f5) as in Print Mode selection above.

## 4-95. Instrument Identification.

4-96. At the beginning of each performance test, the operator will be asked for the date and instrument serial number. Note that the serial number field is 16 characters long and can be any combination of numbers and text.

## 4-97. Auto Or Manual.

4-98. At the beginning of the Auto Test and Harmonic and IM Tests in the Semi-auto Test, the operator will be asked whether to run the test Auto or Manual. Selecting Auto will cause the Auto Test to sequence through all the tests (actually complete all tests that follow the first one selected). You would choose Manual for the Auto Test if only one test were to be run.

4-99. Selecting Manual in the Semi-Auto Test will allow testing at one frequency in the Harmonic Distortion Test (normally 3 frequencies). Intermodulation distortion is measured at four combinations of input sensitivity and vernier position. Manual mode allows testing at any one of the combinations.

## 4-100. DC Balance.

4-101. DC offsets in the input section are minimized by adjusting the Bal potentiometer
below each channel's coupling switch. The recommended adjustment procedure is as follows:
a. Short the input.
b. Adjust sensitivity to the 3 mV or 10 mV range.
c. While holding in the TIME button, adjust the pot until the trace is at the center graticule.

4-102. Alternatively, a 3 or 10 mV signal can be applied to the input and the adjustment made to clear the overload light.

4-103. It is extremely important to make this adjustment before testing, especially before the Auto Test. Misadjusted DC balance can cause premature overloads which will stop program execution.

## 4-104. Addresses.

4-105. Standard HP-IB instrument addresses are given below. These are easily changed in "dev" statements at the beginning of the performance tests. Note that the changes must be made in the Adjustment program and both performance test programs. the HP-IB Verification allows the user to enter the correct 3582A address during program execution.

Standard Addresses

$$
\begin{aligned}
& \text { 3582A(‘‘dut’'): } 711 \\
& \text { 3325A(‘‘syn’'): } 717 \\
& \text { 3330B(‘‘'syn'"): } 704 \\
& \text { 3455A(‘dvm'"): } 706
\end{aligned}
$$

4-106. As an example of changing the addresses via the dev statement, the following statement assigns address 702 to the 3582A and 710 to the synthesizer (either 3325A or 3330B):

$$
\text { dev '"dut", 702, "syn", } 710
$$

4-107. Note that " 7 "' in the above addresses is the interface select code. This can be checked by noting the position of the select switch on the interface (98034A). This is shown in Figure 4 -2. If the select code is not 7, it can be changed on the interface or the "dev" statements can be modified. The 98032A Option 066 Printer Interface should be select code 6. If this is incorrect, the interface select code must be changed. (There is no provision for simple program modification.)

## 4-108. Phase Accuracy.

4-109. The Phase Accuracy Test requires a square wave source and can be done automatically with the 3325A, though obviously not with the 3330B (which has only sine wave output). Thus, phase accuracy is checked in the 3325A Auto Test and the 3330B SemiAuto Test.


Figure 4-2. HP-IB Interface, Select Code 7.

## 4-110. RUNNING THE TESTS.

4-111. This section gives the test procedures in the order that they should be performed. If you choose to run the tests in a different order, always run the HP-IB Verification first followed by the tests of your choice.

## 4-112. Inserting the 3582A/9825A Test Cartridge.

4-113. Insert the tape cartridge so that the label on the cartridge faces the back of the calculator as shown in Figure 4-3.


Figure 4-3. Inserting the Tape Cartridge.

## 4-114. Loading a Tape File.

4-115. To load a tape file into the calculator, perform the following steps:
a. Press calculator buttons

$\underbrace{\text { U }}_{\text {( } 1 \text { is given as an example) }}$
b. When the tape stops running and the red run light is out, press $m$.

## NOTE

When finished with the tests and before removing the tape car. tridge, rewind the tape by pressing ${ }^{\text {®ewivo }}$. This protects the contents of the tape from accidental erasure and foreign object damage.

## 4-116. HP-IB Verification (File 1).

4-117. This test checks bus operation by programming the 3582A and checking displayed data. The tests are as follows:
a. Program the 3582A for a CAL signal display and read out the marker level and frequency at 1 kHz .
b. Program the 3582A so that the status indicators will light. These are checked by the operation.
c. Generate a numerical time record and load it directly into the 3582A's read/write memory. This data is then read out and checked against the input.

4-118. As in all tests, the HP-IB address must be correct. The 3582A is set for address 11 at the factory. If this has been changed, the correct address can be inserted during program execution. (The calculator will ask if the address is 711 and if not, what the correct address is. Note that 7 is the address of the interface.)

4-119. The HP-IB address can be changed rather easily, although the top cover must be removed.

## WARNING

Removing the top cover exposes potentially lethal voltages and should be carried out by service trained personnel only!

4-120. Facing the instrument, the switch is located on the A2 assembly toward the front, right side of the card nest. It is not necessary to remove the shield for purposes of changing the address. Starting at the rear of the instrument the switches are numbered 1 through $\mathbf{6}$, with 1 being the least significant digit. (Switch 7 is used for testing.)

4-121. To change an address, simply enter the binary equivalent of the desired address moving the bits to be set to the right. for example, for address 11 , switches 1,2 and 4 should be to the right of the instrument and all others to the left.

## 4-122. Basic Adjustments (File 2).

4-123. This program runs the technician through the following adjustments for both channels.

## WARNING

To carry out the adjustments below, the top cover must be removed, exposing potentially lethal voltages. These adjustments should be carried out by service trained personnel only.
a. A1-R 101: Amplitude calibration at 1 kHz .
b. A1-R45: Amplitude calibration at 22.5 kHz .
c. A1-R8: CAL signal amplitude calibration.
d. A4-R33: Noise source DC adjustment.
e. A1-C2: 20 dB Attenuator compensation.
f. A1-C1: 40dB Attenuator compensation.
g. A3-C1: Frequency calibration.

4-124. When using the 3325A (trk 0 ), the 3455 A is used to calibrate the 3325 A before the adjustments are made.

4-125. The following points should be noted:
a. The synthesizer used must be a high output voltage option. This is Option 005 for the 3330 B and Option 002 for the 3325A.
b. The first amplitude calibration adjustment level should be within a few mV of 95 mV . If it isn't, double-check the setup.
c. Adjustment tolerance is 1 digit. That is, the tolerance for 900 mV would be $\pm 1 \mathrm{mV}$ while that for 900.1 mV would be $\pm 0.1 \mathrm{mV}$.

## 4-126. Semi-Auto Performance Test (File 3).

4-127. This test requires changing of inputs or settings on non-HP-IB instruments and thus requires an operator during testing.

4-128. Subroutines for this test are contained in File 3 with the programs for each test contained in Files 7 through 18. When a test is to be run, the body of the test is loaded into File 3 after the subroutines. This minimizes memory requirements while eliminating repetition of subroutines. Table $4-5$ summarizes the tests.


Figure 4-4. Adjustment Locations.
4-129. The following points should be noted:
a. Harmonic Distortion. This test is the longest in the group and requires several settings of frequency and level. The hints below should help to speed the process.

1. Frequency is set first using the marker on the 3582 A . Be sure to clear overloads before adjusting the frequency.
2. The operator will be asked repeatedly to set the level of the oscillator to $1-3 \mathrm{~dB}$ below full scale on the 3582A. This is most easily accomplished using the overload lights. That is, adjusting the oscillator output until the light comes on and backing off until it just goes out should insure you of the correct setting.

Note also that the level changes in multiples of 10 dB . The same step size as the 339 A (or 239A) Attenuator. Thus the oscillator amplitude vernier should not have to be changed once the first amplitude has been set.
3. Run the test manually if only one frequency is to be tested. Also remember that one channel only can be tested by pressing special function key f17 (shifted f5) until the desired test mode is displayed.
4. For best results, the 339A should not be in the oscillator level function. If a 239 A is used, the ground should be set to chassis ground. Also, both channels should not be connected at the same time.


Figure 4-5. Test Set-up Intermodulation Distortion.

## NOTE

Although the special function key overlay refers to this test as THD for easy identification, only individual harmonic levels are measured and THD is not calculated.
b. The Intermodulation Distortion test requires the use of 1 K ohm isolation resistors (see Figure 4-6. A small box with the appropriate connectors works well for this. Note that the 50 ohm termination required for the synthesizer must come before the isolation resistor. (Also see Figure 4-5).
c. A handy place to get at chassis ground for the CMR test is the noise souce output BNC.
d. A shielded banana plus (such as Pomona 1645) is required to meet Crosstalk specifications.
e. The Input $\mathbf{Z}$ (impedance) test requires a 1 meg series load. This load must come after the 50 ohm termination required for the synthesizer. (See Figure 4-5.)


Figure 4-6. Constructing A Feedthrough Load.

## 4-130. Auto Performance Test (File 4).

4-131. This test is fully automatic and can be run without attention once started. The only test equipment required in addition to the calculator, ROM's, and interface is a 3330B or 3325 A , a 50 ohm termination and cables.

4-132. While the tests in the Semi-Auto Test are easily identified with published specifications for the 3582A, some tests in this group require further explanation.

4-133. Amplitude accuracy is specified to be 0.5 dB at full scale in the center of the passband. The accuracy specification is completed by specifying linearity to be $+/-0.2 \mathrm{~dB}+$ $-0.02 \%$ of full scale. These specifications include attenuator accuracy and flatness, and A/D flatness.

Table 4.5. Semi-Automatic Performance Test Summary

| Test Name | Special Function | File \# | Equipment Required* | Possible Causes of Failure |
| :---: | :---: | :---: | :---: | :---: |
| Noise Floor | f2 | 7 | 1 K ohm Banana Plug Terminations (2) | A1: Comparator, DAC |
| Harmonic Dist. | f3 | 8 | -hp- 339A or 239A or Oscillator w/Harmonics down at least 80 dB | A1: Comparator, DAC |
| IM Dist. | f4 | 9 | -hp- 3330B or 3325A and Oscillator as above. 1 K Series Resistors (2). 50 ohm Termination |  |
| CMR | f5 | 10 | -hp-3330B or 3325A |  |
| Crosstalk | f6 | 11 | -hp- 3330B or 3325A. Shielded Banana Plug (Pomona 1645). |  |
| Input Z | f7 | 12 | -hp- 3330B or 3325A. I MEG ohm Series Resistor. 50 ohm Termination |  |
| Noise Source Output 2 | f8 | 13 | 50 ohm Feedthru Termination: -hp11048 C Recommended. | A4: U19 |
| Noise Source Flatness | f9 | 14 | None other than Cable. | Programming on A3; A4 |
| Amplitude \& | f10 | 15 |  | A1: Input Filters |
| Phase Match X-Axis Output | f11 | 16 | -hp- 3455A | A10 |
| Phase Accuracy | f16 $\dagger$ | 17 | Function Generator if 3325A not used. -hp-3311A or 3312A Recommended. | A1:LPF; A3, A4: Phase Latches |
| Channel Select | f17 | - | NA | NA |

4-134. This performance test checks not only absolute accuracy and linearity, but also attenuator flatness, input filter and A/D flatness, and attenuator accuracy. This makes it much easier to define the problem when absolute accuracy does not meet specifications.

4-135. The basic noise floor test is done in the Semi-Auto Test. This is essentially testing the input section (A1). To check that the digital filters are not adding noise, the Digital Filter Noise Test checks for excessive noise on all spans.

4-136. The basics of band translation consist of proper center frequency generation in the local oscillator (digital) and multiplication with the input on the digital filter chips. The
L.O./Digital Filter Test varies the center frequency and checks that the proper display is given. The Digital Filter Operation Test checks that the display is proper on each span.

4-137. It can be seen from the above that the two Digital Filter Tests are required for complete testing. However, since the measurement time is long on the narrow spans, these tests add roughly an hour and a half to testing time. For this reason, the operator has the option of running these two tests.

4-138. As an example, after a repair to the instrument, it may make sense to run the short version to insure proper repair and let the long version run overnight to double check.

4-139. Certain out-of-band frequencies can mix with the power supply switching frequency to produce in-band spurious responses. The Special Spurs Test checks for these responses.

## NOTE

The Special Spurs Test includes a test of the out-of-band overload circuit. Units with serial number prefix 1747A will FAIL this test.

4-140. Table 4-6 summarizes the auto tests.
Table 4-6. Automatic Performance Test Summary.

| Test Name | Special Function Key | File | Possible Causes of Failure |
| :---: | :---: | :---: | :---: |
| Cal Signal Accuracy | f2 | 19 | Both channels bad implies A3. Otherwise, check A1U14 or A1K7 |
| Frequency Accuracy | f3 | 20 | Check that A3-C1 is adjusted correctly |
| Amplitude Linearity | f4 | 21 | A1: DAC |
| Attenuator Accuracy | f5 | 22 |  |
| LPF and A/D Flatness | f6 | 23 |  |
| Attenuator Flatness | $f 7$ | 24 | Check that A1C1 and C2 are adjusted |
| L.O./Digital Filter | f8 | 25 | If both channels, check L.O. One channel implies digital filter. |
| Digital Filter Noise | f9 | 26 |  |
| Digital Filter Op. | f10 | 27 |  |
| AC Coupling | f1 1 | 28 |  |
| Special Spurs | f12 | 29 | A1: Comparator; Overload Circuits A1 or A5 |
| Phase Accuracy | $f 13$ | 30* | Phase counters and latches on A3 and A4 |
| Y-Axis Output Channel Select | f14 f1 | 31 | $\begin{aligned} & \text { A10 } \\ & \text { NA } \end{aligned}$ |

## 4-141. Basic Operating Instructions.

4-142. The 9825A Desktop Calculator is much closer to a mini-computer in computational power than to most desktop calculators. Although it is very powerful, the 9825 A is really quite easy to operate. This section is not intended to replace the Operating Manual, but will help the new user to quickly be able to use the test cartridge.

4-143. For these tests, the operator is required to load the proper program from the cartridge and run it, following connection instructions given on the tape.

4-144. There are certain keys that the operator should become familiar with:
a. LOAD - When pressed, 'ldf'" will appear on the display. Pressing this key and entering the desired file number will load the desired tape file into the 9825A's memory after "EXECUTE" is pressed.
b. RUN - Pressing this key will run the program in memory, starting at line number $\emptyset$.
c. CONTINUE - Pressing this key will continue the program from wherever it stopped. For example, the calculator will stop program execution when an instruction is given (e.g., connect 3325 A to channel A). After the instruction is carried out, pressing CONTINUE will cause the program to proceed with the test.


Figure 4-7. -hp- 9825A Calculator.
d. EXECUTE - This key executes what is displayed. For example, pressing LOAD and then a file number (e.g., Ø) will cause "ldf $\emptyset$ '' to be displayed. Pressing EXECUTE will load file $\emptyset$.
e. STOP - Pressing this key will stop the program. Pressing CONTINUE will continue the program from the stopping point.
f. SPECIAL FUNCTION KEYS - These keys, f0 - f11 (f12-f24 using shift) are user definable. For the test cartridge, these keys are automatically programmed to load test files. The overlays included with the tape fit over these keys.
g. SHIFT -This key works just like the shift key on a typewriter, with the additional function of adding 12 more special functions keys. That is, holding down SHIFT while pressing f0 will actually get you f12.

4-145. To load a program from the tape, insert the cartridge with the label toward the rear of the calculator. Note that the record tab should be away from the cartridge edge to prevent accidental erasure.

4-146. Select the track (as explained below) and file desired and press EXECUTE. Error 41 indicates that the cartridge is in backwards or not in all the way. The yellow light near the tape cartridge slot will be lit while the program is loading. Don't press RUN until this light goes out.

4-147. The process of stopping the program to give an instruction or ask a question is repeated over and over during the tests. Answering yes to a question is always done by typing in a one and pressing CONTINUE. To answer no, simply press CONTINUE (zero is assumed).

4-148. To select the proper tape Track, type in "trk" (must be lower case) and $\emptyset$ or 1 . When EXECUTE is pressed, that track will be selected. When the calculator is turned on, track $\emptyset$ is automatically selected.

4-149. Error messages are given when there is an operator or program error. Refer to Error Messges for a list of the most common errors.

4-150. The red RUN LIGHT in the left hand corner of the calculator's display will be on when a program is running. When the program stops to give an instruction, the light will go out. let this light be your guide as to when to press CONTINUE.

## NOTE

Some informational display statements are given without stopping the program.

If the light is out, the program has either ended (in which case "end" should be displayed) or is waiting for the operator to press CONTINUE. If the light is on but nothing seems to happening, be patient.

4-151. As an example, run the "CONTENTS" file as follows:

1. Type in "trk 0 "
2. Press EXECUTE
3. Press LOAD

This selects track 0
4. type in 0
"'Idf" should be displayed
"Idf" should be displayed
5. Press EXECUTE This loads file 0 from track 0
6. Press RUN This should print out a table of contents

4-152. After this listing, the calculator will "beep" and display "address info?(yes = 1)." Note that the run light should now be out. To get the address information, type in a " 1 " and press CONTINUE. Now address information should be printed out.

## 4-153. Error Messages.

05 - Operation not allowed. Usually caused by trying to execute a line out of the program.

15- Printer out of paper.

20
29 ROM missing. The second number (error 29) indicates the missing ROM.

8 - Extended I/O
9-Advanced Programming
10 - Matrix
12 - General I/O
30- Special function key not defined. Caused by pressing a special function key before running either File 3 or File 4, where the keys are defined.

31 - Non-exist program line. Same cause as 30.
40- Insufficient memory for operation. Option 001 (15, 036 Bytes) 9825 A is required. (Check inside tape cover.)

41 - No cartridge in tape transport. Insert cartridge and press EXECUTE.
42- Tape cartridge write protected. (Slide tab to other position for recording.)


When the tab is pushed in the direction of the arrow, write protection is defected and the contents of the tape can be accidentally erased.

44 - Verify has failed. Caused by dirty or bad spot in tape. Try the operation again.
57 - Improper file type. Caused by attempting to load a key file with the load key. To load key files 5 and 6, type in "ldk" and the file number.

60 - Attempt to load an empty file. Check your file number.
64 - Attempt to execute "ldf" or "ldk" while a program is running. Press STOP and then EXECUTE.

66 - Division by zero. This can happen in Phase Accuracy if the function is a sine wave instead of a square wave.

E4 - Timeout error. Caused by non-responding HP-IB instrument hanging the program up.

G8 - Peripheral device down. You'll get this if program is stopped during an I/O operation or an HP-IB instrument is down.

S7 - $\quad$ String not yet allocated. Caused by pressing RUN with only the test file loaded or with the subroutine file loaded but not run.

S9 - $\quad$ String length exceeded. Usually caused by trying to enter more than 16 characters into the serial number field. Shorten the list and press CONTINUE.

## SECTION IV PART III

## MANUAL PERFORMANCE TEST

### 4.154. INTRODUCTION.

4-155. The Manual Performance Test is conducted using common manually operated test equipment. Due to its reiterative nature, the test requires $91 / 2$ hours to complete. The more comprehensive automatic test is recommended over the manual test if the equipment is available.

## 4-156. APPLICABILITY.

4-157. The Manual Performance Test should be used only when complete and comprehensive testing of instrument performance to one or more specifications is desired. After minor repairs are made or for incoming inspection, the Operational Verification given in Section IV Part I is recommended.

## 4-158. ORGANIZATION.

4-159. The test is performed in the same order as the Automated Performance Tests with the most stringent requirements first. This is done so that areas that are most likely to fail are encountered early and repairs and/or adjustments may be carried out before large amounts of test time are accumulated.

## 4-160. REUUIIRED TEST EQUIPMENT.

4-161. If the recommended equipment is not available, equipment meeting the specifications given in Table 4-7 may be substituted.

Table 4.7. Recommended Test Equipment For Manual Performance Test.

| Instrument | Important Characteristics | Required Model |
| :---: | :---: | :---: |
| Synthesizer | Amplitude Accuracy: $\pm 0.2 \mathrm{~dB}$ at 10 kHz | -hp-3330B (Opt. 004 \& 005) or -hp- 3325A (Opt. 002) |
| Digital Voltmeter | AC Accuracy $0.1 \%$ at 20 kHz | -hp-3455A |
| Low Distortion Oscillator | Harmonics > 80 dB below Fundamental | $\begin{aligned} & \text {-hp-339At or } \\ & \text {-hp- 239A } \end{aligned}$ |
| Function Generator | Required only if 3330 B used as Synthesizer | -hp-3311At or -hp-3310A $\dagger$ or -hp- 3312 A $\dagger$ |
| Terminations | Short-Banana Plug | 1251-2816 w/short |
|  | $1 \mathrm{k} \Omega$ - Banana Plug (2) <br> $1 \mathrm{k} \Omega$ - Series (2) | $\begin{gathered} 1251-2816 \mathrm{w} / 1 \mathrm{k} \Omega \\ \mathrm{NA} \end{gathered}$ |
|  | 1 MEG Series | NA |
|  | 50 Ohm Feedthrough | -hp-11048C † |
| Miscellaneous | Shielded Banana Plug | Pomona $1645 \dagger$ |

## 4-162. Preset.

4-163. Preset refers to a mode in which the 3582A front panel switches should be set prior to the initiation of each test sequence. The switch settings are given as follows (line switch excepted):

Button Positions: ON OFF
Set both framed buttons ..... ON
Set AMPLITUDE A ..... ON
Set SCALE ..... $10 \mathrm{~dB} /$ DIV
Set PASSBAND SHAPE ..... FLAT TOP
Set AVERAGE NUMBER 4 ..... ON
Set all other buttons. ..... OFF
AMPLITUDE REFERENCE LEVEL NORM (Position 1)
FREQUENCY MODE ..... $0-25 \mathrm{kHz}$
SPAN ..... 25 kHz
TRIGGER LEVEL ..... FREE RUN
INPUT CHANNEL A SENSITIVITY ..... $+30 \mathrm{dBV}$
VERNIER ..... CAL
INPUT CHANNEL B SENSITIVITY ..... $+30 \mathrm{dBV}$
VERNIER ..... CAL
INPUT MODE ..... A
ISOL-CHAS ..... CHAS

## 4-164. INSTRUMENT WARMUP.

4-165. Before any of the performance tests are conducted, be sure that all equipment associated with the test is functioning within specified operating limits. The 3582A requires 30 minutes of warmup before any test is initiated.

4-166. Perform the following steps:
a. Verify that all test equipment is operating under the proper conditions.
b. Connect the 3582A to a suitable power receptacle using the power cord provided with the instrument. DO NOT FLOAT THE 3582A USING A POWER PLUG ADAPTER!
c. Set the 3582 A front panel switches to the preset mode and turn the LINE switch ON.
d. Allow at least 30 minutes of warmup time for the 3582 A before initiating any of the performance tests.

## 4-167. DC BAL VERIFICATION.

4-168. Before performing any of the following tests, verify that the BAL (offset) is not excessively out of adjustment.

4-169. Perform the following steps:
a. Verify that the 3582A switches are in the preset mode.
b. Short the input terminals of channel $\mathbf{A}$.
c. Set the CHANNEL A SENSITIVITY to -50dBV.
d. Press the TIME A button and verify that the trace is at the center horizontal graticule. If it is not, correct its position by adjusting the channel A BAL control.
e. Perform steps b through d for channel B after setting the INPUT MODE switch to B, AMPLITUDE A to OFF, and AMPLITUDE B to ON.

### 4.170. CONDUCTING THE PERFORMANCE TESTS.

4-171. Each test is written in flowchart form. Repetitious steps are included in subroutines to reduce complication. Exits to subroutines are indicated by an alphanumeric symbol in a circle. Proceed to the subroutine which starts with the same symbol. When finished with the subroutine, proceed to the RETURN step which immediately followed the exit step.

4-172. Example:


## NOTE

Unless otherwise stated, instructions indicated in each step will pertain to the 3582A.

### 4.173. NOISE FLOOR.

4-174. The noise floor test insures that all noise internal to the analyzer is at least -115 dBV between 800 Hz and 1.2 kHz and that it is at least -120 dBV between 2.5 kHz and 25 kHz .
4.175. Recommended Test Equipment:

Termination: 1 Kohm banana plug
4-176. Instrument Control Settings:
3582A: Preset
MARKER ON
SENSITIVITY (channel A only).......................... . . - 50dBV
AVERAGE NUMBER.............................................. . . . . 32
AMPLITUDE REFERENCE LEVEL. . . . . . . . . . . . . . . . Position 3
(NORM is position 1)

4-177. Perform the steps as indicated in the flow chart.


Figure 4-8. Noise Floor Test.

### 4.178. HARMONIC DISTORTION.

4-179. The harmonic distortion test checks for harmonically related signals which are generated within the instrument when a full scale input is present. To perform this test requires a signal source which has a signal with harmonic distortion products less than 80 dB below the fundamental.

4-180. As part of the test, the operator will be asked repeatedly to set the level of the oscillator $1-3 \mathrm{~dB}$ below full scale as indicated by the 3582A. This is most easily accomplished by increasing the 339A amplitude until the OVERLOAD lights on the 3582A come on and then reducing the amplitude until they go off. In most cases, the vernier amplitude adjustment will not need to be made often since the 339A/239A output attenuator has 10 dB increments like the 3582A INPUT SENSITIVITY control.

## 4-181. Recommended Test Equipment:

339A Distortion Measuring Set or 239A Low Distortion Oscillator
Compatible shielded (coax) interconnecting cables with appropriate adaptors.

4-182. Instrument Control Settings:
3582A: Preset
FREQUENCY MODE...................................... 0 -START
FREQUENCY SPAN............................................ 25 kHz
SENSITIVITY (channel A only).......................... . . . - 50dBV
AVERAGE NUMBER.................................................... . 4
339A:
FREQUENCY ...................................................... . . . 8kHz
AMPLITUDE . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3mV

4-183. Perform the steps as indicated in the flow chart.



### 4.184. INTERMODULATION DISTORTION AND VERNIER RANGE.

4-185. The intermodulation distortion test checks for excessive amplitudes of harmonic products which are produced when a complex signal is acted upon by a non-linear circuit. The vernier range is checked for the minimum allowable signal attenuation between the 10 dB steps of the INPUT SENSITIVITY switch.

4-186. The complex signal is generated across a resistor network which uses two oscillators for inputs (see test setup Figure 4-10).


Figure 4-10. Intermodulation Distortion Test Setup.

## 4-187. Recommended Test Equipment:

3325A Synthesizer/Function Generator
339A Distortion Measuring Set
Compatible interconnecting cables with appropriate adaptors
Terminations: 50 ohms, 2-1 Kohm resistors (-hp- Part No. 0575-0280).

4-188. Instrument Control Settings:
3582A: Preset
MARKER ON
SENSITIVITY (channel A only) . . . . . . . . . . . . . . . . . . . . . - 50dBV
AVERAGE NUMBER...................................................... . 4
3325A:
FREQUENCY . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 24 kHz
AMPLITUDE ............................................. . . . 39.99 dBm
FUNCTION.............................................. SINE WAVE
Termination........................................................ 50 ohms
339A:
FREQUENCY . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 25 k .
AMPLITUDE........................................................... . 3 mV

4-189. Perform the steps as indicated in the flow chart.


Figure 4-12. Intermodulation Distortion \& Vernier Range.

### 4.190. COMMON MODE REJECTION.

4-191. The common mode rejection test verifies the capability of the 3582A to ignore a signal which appears simultaneously and in phase at both terminals of a single channel.

## 4-192. Recommended Equipment:

3325A Synthesizer/Function Generator Option 002
Compatible shielded (coax) interconnecting cables with appropriate adaptors.

## 4-193. Instrument Test Setups.

4-194. Set up the instruments according to Figure $4-13$ and $4-14$ when instructed to do so by steps in the flow chart.


Figure 4-13. Test Setup A.


Figure 4-14. Test Setup B.
4-195. Instrument Control Setting.

| 3582A: Preset |  |
| :---: | :---: |
| FREQUENCY MODE. | 0-START |
| FREQUENCY SPAN. | 500 Hz |
| MARKER | ON |

FREQUENCY
AMPLITUDE (High Voltage ON) . . . . . . . . . . . . . . . . . . . 14.14Vrms
FUNCTION. SINE WAVE
196. Perform the steps as indicated in the flow chart.


Figure 4-15. Common Mode Rejection.

### 4.197. CROSS TALK.

4-198. The cross talk test measures the amount of undesirable energy in one channel that has been coupled across from the other channel. This is accomplished by placing a high signal level on one channel and then measuring the relative signal amplitude on the other channel which has a 1 K ohm load across the input terminals (see Figure 4-16).


Figure 4-16. Cross Talk Measured On Channel B.

## 4-199. Recommended Test Equipment.

3325A Synthesizer/Function Generator Option 002
Compatible shielded (coax) interconnecting cables with appropriate adaptors.

Hooded GR Connector
4-200. Instrument Control Settings.3582A: PresetFREQUENCY MODE.................................. SET CENTERFREQUENCY SPAN1 kHz
FREQUENCY ADJUST ..... 25 kHz
MARKER .....  ON
MARKER POSITION ..... Adjust to 25 kHz
SENSITIVITY (Channel B) ..... $-50 \mathrm{dBV}$
AVERAGE NUMBER ..... 8
3325A:
FREQUENCY ..... 25 kHz
AMPLITUDE (High Voltage ON) ..... 14.14Vrms
FUNCTION SINE WAVE

4-201. Perform the steps as indicated in the flow chart.


Figure 4-17. Cross Talk.

### 4.202. INPUT IMPEDANCE TEST

4-203. The input impedance test verifies that the input resistance is $1 \mathrm{Mohm} \pm 30 \mathrm{Kohm}$ and the capacitance is less than 60pf. The test uses the Periodic Noise source and an attenuator compensation network formed by a series resistance paralleled by a capacitor.


## Figure 4-18. Input Compensation Network.

4-204. The network may be made by soldering a 56pf capacitor -hp- Part No. 0140-0191 across a 1 Mohm resistor -hp- Part No. 0698-7332. The network is then connected beween the "high" input terminals of channels A and B (see Figure 4-18).

4-205. The test is then performed by placing the Noise Source Output on one input channel and then measuring the effect of the attenuator on the input of the second channel. By using a dual channel amplitude display and the amplitude transfer function, the input resistance can be measured (ideally a -6 dB drop) and the capacitance limits determined (using the


Input Resistance


Input Capacitance

Figure 4-19. Effects Of The Compensation Network On Input.
amplitude and slope of the transfer function at higher frequencies, ideally a flat trace indicating 56pf, see Figure 4-19). The input attenuator is checked by using three selected Sensitivity settings.

Compensation Network: Capacitor 56pf -hp- Part No. 0140-0191 Resistor 1 Mohm 1\% -hp- Part No. 0698-7332

4-207. Instrument Control Settings.
3582A: Preset

| INPUT SENSITIVITY (both channels). | 20dBV |
| :---: | :---: |
| AVERAGE NUMBER. | 32 |
| DISPLAY AMPLITUDE B. | ON |
| INPUT MODE | BOTH |
| MARKER. | ON |

4-208. Perform the steps indicated in the flow chart.


## 4-209. NOISE SOURCE OUTPUT IMPEDANCE.

4-210. The noise source output impedance test verifies that the impedance is less than 2 ohms by comparing amplitudes at 25 kHz with and without a 50 ohm load.

## 4-211. Recommended Test Equipment.

Termination: 50 ohms

Compatible shielded (coax) interconnecting cables with appropriate adaptors.

## 4-212. Test Equipment Setup.

4-213. Connect the IMPULSE output to the TRIGGER input on the rear panel of the 3582A. Then, set the TRIGGER switch to EXT. Connect the NOISE SOURCE OUTPLT to the Channel A input. The NOISE SOURCE LEVEL should be set to maximum and the function set to PERIODIC.

## 4-214. Instrument Control Setting.

3582A: Preset
INPUT SENSITIVITY (Channel A Only)....................... . 3 V
COUPLING..................................................................
TRIGGER LEVEL..................................... . . . . . . . . . . . .
MARKER................................................................. . . ON
SCALE.......................................................... . . . LINEAR
AMPLITUDE REFERENCE LEVEL. . . . . . . . . . . . . . Position \#5
AVERAGE NUMBER.................................................. . . . 8
MARKER POSITION.............................................. 25 kHz
PASSBAND SHAPE....................................... UNIFORM

4-215. Perform the steps as indicated in the flow chart.


Figure 4-21. Noise Source Output Impedance.

### 4.216. NOISE SUURCE AMPLITUDE.

4-217. The noise source amplitude test verifies that energy is outputed at a constant level for each span and resulting frequency displayed. In RANDOM, the noise is averaged and the results tested for constant amplitude for all frequencies of the selected span.

## 4-218. Recommended Test Equipment.

Termination: 50 ohms
Compatible shielded (coax) cables with appropriate adaptors.

## 4-219. Test Equipment Setup.

4-220. Connect the NOISE SOURCE OUTPUT to Channel A using a 50 ohm termination. Verify that the NOISE SOURCE LEVEL is in the detented position indicating maximum output amplitude.

4-221. Instrument Control Setting.

| 3582A: Preset |  |
| :---: | :---: |
| INPUT SENSITIVITY (Channel A only). | . 10 dBV |
| COUPLING | DC |
| MARKER. | ON |
| MARKER POSITION. | 1 kHz |
| FREQUENCY MODE | 0-START |
| PASSBAND SHAPE. | UNIFORM |
| AVERAGE NUMBER. | ........ 8 |

4-222. Perform the steps as indicated in the flow chart.


## 4-223. CAI.IBRATION ACCURACY.

4-224. The calibration accuracy test checks the amplitude of the calibration signal at selected frequencies.

## 4-225. Instrument Control Settings.

3582A: PresetINPUT SENSITIVITY (Both channels)...................... . . CAL
MARKER ..... ON
MARKER POSITION. ..... 1 kHz

4-226. Perform the steps as indicated in the flow chart.


Figure 4-23. Calibration Accuracy.

### 4.227. FREQUENCY ACCURACY.

4-228. The frequency accuracy test uses an external signal source to verify that the digital local oscillator and marker frequency readout are operating within specifications.

## 4-229. Recommended Test Equipment.

3325A Synthesizer/Function Generator
Termination: $\mathbf{5 0}$ ohms
Compatible shielded (coax) interconnecting cables with appropriate adaptors.

### 4.230. Test Equipment Setup.

4-231. Connect the 3325A to the Channel A input of the 3582A using a 50 ohm load.
4-232. Instrument Control Settings.
3582A: Preset
INPUT SENSITIVITY (Channel A only).................. . . 10 dBV
FREQUENCY MODE.................................. SET CENTER
FREQUENCY ADJUST. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 25 kHz
FREQUENCY SPAN................................................... 5 Hz
MARKER............................................................. . . . .
PASSBAND SHAPE....................................... HANNING
3325A:
FREQUENCY . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 25 kHz
AMPLITUDE . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2.05dBm
FUNCTION................................................. SINE WAVE

4-233. Perform the steps as indicated in the flow chart.


Figure 4-24. Frequency Accuracy.

## 4-234. LINEARITY.

4-235. The linearity test checks the amplitude accuracy of the 3582A when a signal of less than full scale level is present on the input.

## 4-236. Recommended Test Equipment.

## 3325A Synthesizer/Function Generator

Termination: 50 ohms
Compatible shielded (coax) interconnecting cables with appropriate adaptors.

4-237. Connect the 3325A to both channels A and B using one 50 ohm load.
4-238. Instrument Control Settings.
3582A: Preset
INPUT SENSITIVITY (Both channels). . . . . . . . . . . . . . . + . 10dBV
MARKER............................................................. . . . ON
MARKER POSITION. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 13.2 kHz
AVERAGE NUMBER.................................................. . . . 16
3325A:
FREQUENCY . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 13.2 kHz
AMPLITUDE . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 22.01 dBm
FUNCTION............................................... SINE WAVE

4-239. Perform the steps as indicated on the flow chart.
Table 4-8. 3582A Test Limits.

| Amplitude Reference Level | 3325A Amplitude (dBm) | 3582A Test Limits (dB) |
| :---: | :---: | :---: |
| $\# 2$ | 12.01 | $-10.2 /-9.80$ |
| $\# 3$ | 2.01 | $-20.2 /-19.8$ |
| $\# 4$ | -17.99 | $-30.3 /-29.7$ |
| $\# 5$ | -27.99 | $-40.4 /-39.6$ |
| $\# 6$ | -37.99 | $-50.8 /-49.2$ |
| $\# 7$ | -47.99 | $-62.5 /-58.1$ |
| $\# 8$ | $-81.4 /-65.2$ |  |



Figure 4-25. Linearity.

### 4.240. ATTENUATOR ACCURACY.

4-241. The attenuator accuracy test checks the 3582A input attenuator by using the marker amplitude readout to measure a known input level on each attenuator setting.

## 4-242. Recommended Test Equipment.

3325A Synthesizer/Function Generator

Termination: 50 ohms

Compatible shielded (coax) interconnecting cables with appropriate adaptors.

### 4.243. Test Equipment Setup.

4-244. Connect the 3325 A output to both channels A and B using one 50 ohm load.

## 4-245. Instrument Control Settings.

```
3582A: Preset
INPUT SENSITIVITY (Both channels). . . . . . . . . . . . . . + 10dBV
MARKER........................................................................
MARKER POSITION......................................................
CHAS-ISOL................................................................
3325A:
```



```
AMPLITUDE ....................................... . . . +22.01dBM
```



4-246. Perform the steps as indicated in the flow chart.

Table 4.9. 3582A Attenuator Accuracy.

| 3582A Sensitivity (dBV) | 3325A Amplitude (dBm) | 3582A Test Limit (dB REL) |
| :---: | :---: | :---: |
| +30 | 22.01 | $0 \pm .2$ |
| +20 | 22.01 | $0 \pm .2$ |
| +10 | 22.01 | $0 \pm .2$ |
| 0 | 12.01 | $-10 \pm .2$ |
| -10 | 2.01 | $-20 \pm .2$ |
| -20 | -7.99 | $-30 \pm .2$ |
| -30 | -17.99 | $-40 \pm .2$ |
| -40 | -27.99 | $-50 \pm .2$ |
| -50 | -37.99 | $-60 \pm .2$ |



* On channel under test.
** Both channels.

Figure 4-26. Attenuator Accuracy.

## 4-247. INPUT FILTER AND ANALOG TO DIGITAL CONVERTER FLATNESS.

4-248. A signal source is used to check the flatness of the input filter and analog to digital converter by providing a sine wave at selected frequency intervals. The variation between the amplitude of the reference frequency and the remaining frequencies is obtained by using the relative marker readout.

## 4-249. Recommended Test Equipment.

## 3325A Synthesizer/Function Generator

Termination: 50 ohms
Compatible shielded (coax) interconnecting cables with appropriate adaptors.

### 4.250. Test Equipment Setup.

4-251. Connect the 3325A to both channels A and B using one 50 ohm load.

## 4-252. Instrument Control Settings.

```
3582A: Preset
INPUT SENSITIVITY (Both channels). . . . . . . . . . . . . . . . OdBV
FREQUENCY MODE......................................START
```



```
MARKER...........................................................................
MARKER POSITION. . . . . . . . . . . . . . . . . . . . . . . . . . . . 2.5kHz
3325A:
FREQUENCY .............................................. . . 2.5kHz
AMPLITUDE ........................................... . . . . . . . . .01dBm
FUNCTION...........................................SINE WAVE
```

4-253. Perform the steps as indicated in the flow chart.
Table 4-10. 3325A Frequency Settings (kHz).

| 1.2 | 6.2 | 11.2 | 16.2 | 21.2 |
| :--- | ---: | ---: | ---: | ---: |
| 2.5 | 7.5 | 12.5 | 17.5 | 22.5 |
| 3.7 | 8.7 | 13.7 | 18.7 | 23.7 |
| 5.0 | 10.0 | 15.0 | 20.0 | 25.0 |

Table 4-11. 3325A Frequency Settings (kHz).

|  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- |
| 1.480 | 2.48 | 4.48 | 6.48 | 8.48 |
| 1.48 | 3 | 5 | 7 | 9 |
| 2 | 3.48 | 5.48 | 7.48 | 9.48 |



Figure 4-27. Input filter And Analog To Digital Converter Flatness.

### 4.254. ATTENUATOR FLATNESS.

4-255. The attenuator flatness test uses a signal source, to supply a constant amplitude for several frequencies, in conjunction with the relative marker readout to assure flatness at each attenuator setting.

## 4-256. Recommended Test Equipment.

3325A Synthesizer/Function Generator
Termination: 50 ohms
Compatible shielded (coax) interconnecting cables with appropriate adaptors.

## 4-257. Test Equipment Setup.

4-258. Connect the 3325A to both channels A and B using one 50 ohm load.
4-259. Instrument Control Settings.

```
3582A: Preset
INPUT SENSITIVITY (Both channels). . . . . . . . . . . . . . . . . 30dBV
FREQUENCY MODE....................................... 0 -START
MARKER............................................................... . . . . .
MARKER POSITION. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2.5 kHz
CHAS-ISOL............................................................. ISOL
3325A:
FREQUENCY . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2.5 kHz
AMPLITUDE . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 22.01 dBm
FUNCTION............................................... . . SINE WAVE
```

4-260. Perform the steps as indicated in the flow chart.
Table 4-12. 3325A Amplitude Settings.

| 3582A Sensitivity (dBV) | 3325A Amplitude (dBm) |
| :---: | :---: |
| +30 | 22.01 |
| +20 | 22.01 |
| +10 | 22.01 |
| 0 | 12.01 |
| -10 | 2.01 |
| -20 | 7.99 |
| -30 | -17.99 |
| -40 | -27.99 |
| -50 | -37.99 |



Figure 4-28. Attenuator Flatness.

### 4.261. LOCAL OSCILLATOR/MIXER SPURS.

4-262. To test for spurs, the local oscillator output is internally mixed with a reference signal (generated by an external source) by using the SET CENTER frequency mode of operation. The marker readout is then used to verify that all frequencies other than the reference frequency, the negative frequency, and 0 Hz contain spurious products below specified limits.

### 4.263. Recommended Test Equipment.

## 3325A Synthesizer/Function Generator

Termination: $\mathbf{5 0}$ ohms
Compatible shielded (coax) interconnecting cables with appropriate adaptors.

## 4-264. Test Equipment Setup.

4-265. Connect the 3325A to both channels A and B using one 50 ohm load.
4-266. Instrument Control Settings.
3582A: PresetINPUT SENSITIVITY (Both channels). . . . . . . . . . . . . . . . . . OdBVFREQUENCY MODE................................. SET CENTER
FREQUENCY ADJUST ..... 2.5 kHz
MARKER .....  ON
MARKER POSITION ..... 2.5 kHz
PASSBAND SHAPE ..... HANNING
AVERAGE NUMBER ..... 8
3325A:
FREQUENCY ..... 2.5 kHz
AMPLITUDE ..... 3.01 dBm
FUNCTION SINE WAVE

4-267. Perform the steps as indicated in the flow chart.


Figure 4-29. Local Oscillator Mixer Spurs.

## 4-268. DIGITAL FILTER NOISE.

4-269. To check for digital filter noise, a source signal is inputed and adjusted in frequency such that the fundamental is within the range of each span selected. Then for each span, noise (when found above a specified level) appears as spurious responses which are not associated with the fundamental or its harmonics.

### 4.270. Recommended Test Equipment.

## 3325A Synthesizer/Function Generator

Termination: 50 ohms

Compatible shielded (coax) interconnecting cables with appropriate adaptors.

### 4.271. Test Equipment Setup.

4-272. Connect the 3325A to both channels A and B using one 50 ohm load.
4-273. Instrument Control Settings.
3382A: Preset
INPUT SENSITIVITY (Both channels). . . . . . . . . . . . . . . . . . OdBV
FREQUENCY MODE.................................... . SET START
MARKER.............................................................. . . . ON
AVERAGE NUMBER.................................................. . . . . . 4
FREQUENCY ADJUST. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0 Hz

3325A:
FREQUENCY . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6.25 kHz
AMPLITUDE . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12.01 dBm
FUNCTION SINE WAVE

4-274. Perform the steps as indicated in the flow chart.
Table 4-13. 3325A Frequency Settings.

| 3582A Span | 3325A Frequency | Second Harmonic | Third Harmonic |
| :---: | :---: | :---: | :---: |
| 25 KHz | 6250 | 12500 | 18750 |
| 10 KHz | 2500 | 5000 | 7500 |
| 5 KHz | 1250 | 2500 | 3750 |
| 2.5 KHz | 650 | 1250 | 1875 |
| 1 KHz | 250 | 500 | 750 |
| 500 | 125 | 250 | 375 |
| 250 | 62.5 | 125 | 187.5 |
| 100 | 25 | 50 | 75 |
| 50 | 12.5 | 25 | 37.5 |
| 25 | 6.25 | 12.5 | 18.75 |
| 10 | 2.5 | 5 | 7.5 |
| 5 | 1.25 | 2.5 | 3.75 |



Figure 4-30. Digital Filter Noise.

## 4-275. DIGITAL FILTER DPERATION.

4-276. An external source is used to check digital filter operation by supplying signals to determine flatness between the frequency limits of each span and also a signal used to check for the aliasing of data about the effective sample rate for each span.

## 4-277. Recommended Test Equipment.

## 3325A Synthesizer/Function Generator

Termination: 50 ohms
Compatible shielded (coax) interconnecting cables with appropriate adaptors.

## 4-278. Test Equipment Setup.

4-279. Connect the 3325A to both channels A and B using one 50 ohm load.
4.280. Instrument Control Settings.
3582A: Preset
INPUT SENSITIVITY (Both channels) . . . . . . . . . . . . . . . . . . OdBV
FREQUENCY MODE.................................... . SET START
FREQUENCY ADJUST.............................................. . . 0 Hz
MARKER............................................................... . . . .
MARKER POSITION. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2.5 kHz
COUPLING........................................................... . . .
3325A:
FREQUENCY . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2.5 kHz
AMPLITUDE . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12.01 dBm
FUNCTION
SINE WAVE

4-281. Perform the steps as indicated in the flow chart.

Table 4-14. 3325A Frequency Settings.

| 3582A Span | 3325A Frequency $=1 / 10$ Span | 3325A Frequency $=3.996 \times$ Span |  |  |
| :---: | :---: | :---: | :---: | :---: |
| 25 | KHz | 2.5 KHz |  |  |
| 10 | KHz | 1 KHz |  |  |
| 5 KHz | 500 | 99.9 KHz |  |  |
| 2.5 KHz | 250 | 39.96 KHz |  |  |
| 1 KHz | 100 | 19.98 KHz |  |  |
| 500 | 50 | 9.99 KHz |  |  |
| 250 | 25 | 1996 |  |  |
| 100 | 10 | 999 |  |  |
| 50 | 5 | 399.6 |  |  |
| 25 | 2.5 | 199.8 |  |  |
| 10 | 1 | 99.9 |  |  |
| 5 | .5 | 39.96 |  |  |
|  |  |  |  |  |



Figure 4-31. Digital Filter Operation.

## 4-282. AC COUPLING.


#### Abstract

4-283. AC Coupling is checked by noting the change in amplitude when the frequency, from an external source, is reduced from 1 kHz to 1 Hz .1 Hz and lower frequencies are in the region of amplitude attenuation since the AC Coupling network acts as a high pass filter.


4-284. Recommended Test Equipment.
3325A Synthesizer/Function Generator
Termination: 50 ohms
Compatible shielded (coax) interconnecting cables with appropriate adaptors.

## 4-285. Test Equipment Setup.

4-286. Connect the 3325A to both channels A and B using one 50 ohm load.
4-287. Instrument Control Settings.
3582A: Preset
INPUT SENSITIVITY (Both channels) . . . . . . . . . . . . . . . - 10dBV
FREQUENCY MODE................................. SET CENTER
FREQUENCY SPAN............................................... 50 Hz
FREQUENCY ADJUST . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1 kHz
MARKER................................................................. . . .
MARKER POSITION............................................. 1 kHz
COUPLING................................................................... $A C$
3325A:
FREQUENCY . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1 kHz
AMPLITUDE . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2.56 dBm
FUNCTION................................................ . SINE WAVE

4-288. Perform the steps as indicated in the flow chart.


Figure 4-32. AC Coupling. 4-65/4-66

### 4.289. SPECIAL SPURS.


#### Abstract

4-290. The special spurs test uses an external source to supply signals which are above the upper frequency limit of the 3582A. The marker is then set to specific frequencies where the amplitude is checked to determine if any aliased products of the input appear in the spectral display.


## 4-291. Recommended Test Equipment.

3325A Synthesizer/Function Generator
Termination: 50 ohms
Compatible shielded (coax) interconnecting cables with appropriate adaptors.

4-292. Test Equipment Setup.
4-293. Connect the 3325A to both channels $A$ and $B$ using one 50 ohm load.
4-294. Instrument Control Settings.
3582A: Preset
INPUT SENSITIVITY (Both channels). . . . . . . . . . . . . . . - 10dBV
FREQUENCY MODE...................................... . 0 -START
FREQUENCY SPAN. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 10 kHz
MARKER. ............................................................ . . . .
MARKER POSITION. ......................................... . . 10 kHz
AVERAGE NUMBER................................................. . . 16
3325A:
FREQUENCY . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 71920 Hz
AMPLITUDE . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2.56 dBm
FUNCTION................................................ SINE WAVE

4-295. Perform the steps as indicated in the flow chart.


### 4.296. PHASE ACCURACY.

4-297. The phase accuracy test checks the relative phase relationship between the harmonics of a square wave signal to determine if the 3582A is within specification in phase with respect to frequency.

## 4-298. Recommended Test Equipment.

3325A Synthesizer/Function Generator
Termination: 50 ohms
Compatible shielded (coax) interconnecting cables with appropriate adaptors.

## 4-299. Test Equipment Setup.

4-300. Connect the 3325A to both channels A and B using one 50 ohm load.
4-301. Instrument Control Settings.3582A: PresetINPUT SENSITIVITY (Both channels) . . . . . . . . . . . . . . . . . . . dBV
DISPLAY AMPLITUDE A .....  OFF
DISPLAY PHASE A ..... ON
TRIGGER LEVEL ..... CENTERED
TRIGGER SLOPE ..... ON(-)
MARKER ..... ON
MARKER POSITION ..... 1 kHz
3325A:
FREQUENCY ..... 1 kHz
AMPLITUDE ..... 12.1 dBm
FUNCTION SQUARE WAVE

4-302. Perform the steps as indicated in the flow chart.


Figure 4-34. Sample Phase Display.


Figure 4-35. Phase Accuracy.

## OPERATIONAL VERIFICATION TEST CARD

Hewlett-Packard Model 3582A
Spectrum Analyzer
Serial No. $\qquad$
Test Performed By
Date $\qquad$

ROM Self Test: Pass Fail

Display Accuracy:

| Frequency $(\mathrm{Hz})$ | 012500 | 25000 |
| :--- | :---: | :---: |
| Reading $\pm 250 \mathrm{~Hz}$ |  |  |

## Calibrator Accuracy:

|  |  | Pass | Fail |
| ---: | :---: | :---: | :---: |
| 25 Amplitude Readings | CH A | - |  |
| $(1 \mathrm{kHz}$ to 25 kHz$) 22.0 \pm 0.2 \mathrm{dBV}$ | CHB | - |  |

Amplitude Accuracy and Flatness:

| Frequency ( kHz ) |  | $\mathrm{CHA}( \pm 0.5)$ |  | $\mathrm{CHB}( \pm 0.5)$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 2.5 | 22.5 | 2.5 | 22.5 |
| Sensitivity | $+30$ |  |  |  |  |
|  | +10 |  |  |  |  |
|  | -10 |  |  |  |  |

Noise:


## Harmonic Distortion:

|  | CH A | CH B |  |
| :--- | :---: | :---: | :---: |
| Harmonic | 2nd | 3rd | 2nd | 3rd

## Common Mode Rejection:

|  |  | Frequency | CH A | CHB |
| :--- | :---: | :---: | :---: | :---: |
| Marker | $<-66 \mathrm{~dB}$ | 50 Hz | - |  |
| Amplitude | $<-64 \mathrm{~dB}$ | 60 Hz |  |  |
| Reading |  |  |  |  |

Frequency Accuracy:

| Reading at $25 \mathrm{kHz} \pm 0.5 \mathrm{~Hz}$ | $\mathrm{CHA} \quad \mathrm{CH} \mathrm{B} \quad-$ |
| :--- | :--- | :--- |

Phase Accuracy:

|  |  | Pass | Fail |
| :--- | :--- | :--- | :--- |
| Maximum Variation at | CH A |  |  |
| 5th Harmonic $< \pm 10^{\circ}$ | CH B | - | - |

Amplitude and Phase Match Between Channels:

|  |  | CHA |  |
| :--- | :--- | :--- | :--- |
|  |  | Pass | Fail |
| Marker Reading | $< \pm 0.8 \mathrm{~dB}$ | - |  |
| Variation | $< \pm 5^{\circ}$ | - | - |

## MANUAL PERFORMANCE TEST CHECK LIST

Test Description PassFail
Noise Floor
$\qquad$
Harmonic Distortion$\underline{ }$
Intermodulation Distortion and Vernier Range

$\qquad$
Intermodulation Distortion and Vernier Range
$\qquad$
$\qquad$
Common Mode Rejection
$\qquad$
Cross Talk
$\qquad$$\underline{ }$
Input Impedance
$\qquad$
Noise Source Output Impedance
Noise Source Amplitude
$\qquad$
$\qquad$
Calibration Accuracy
$\qquad$
$\qquad$
Frequency Accuracy$\underline{ }$
$\qquad$
Linearity
$\qquad$
Attenuator Accuracy-
$\qquad$
Input Filter and Analog to Digital Converter Flatness

$\qquad$
$\qquad$Attenuator Flatness-
$\qquad$Local Oscillator Spurs
$\qquad$
$\qquad$
Digital Filter Noise
$\qquad$
$\qquad$Digital Filter Operation
$\qquad$
AC Coupling $\qquad$
$\qquad$
Special Spurs
$\qquad$Phase Accuracy

## WARNING

Maintenance described herein is performed with power supplied to the instrument, and protective covers removed. Such maintenance should be performed only by service-trained personnel who are aware of the hazards involved (for example, fire and electrical shock). Where maintenance can be performed without power applied, the power should be removed.

# SECTION V ADJUSTMENT PROCEDURES 

## 5-1. INTRODUCTION.

5-2. This section describes adjustments and checks required to return the 3582A to peak performance when repairs have been made. Adjustments are presented in the following order:
a. Power Supply Adjustments.
b. CRT Control Adjustments.
c. CRT Calibration Adjustments.
d. 45.8752 MHz Adjustment.
e. Back-gate Bias Adjustment.
f. Input Board Adjustment.
g. Pseudo-random Noise Source DC Adjustment.

## NOTE


#### Abstract

An automated adjustment procedure is included in the 3582A/9825A Test Cartridge. (See Section IV Paragraph 4-I22 of the Service Manual.)


### 5.3. TEST POINT AND ADJUSTMENT LOCATIONS.

5-4. Test point and adjustment locations are supplied as assembly locators within the text and as an instrument locator (foldout) at the end of this section. Most of the test points and adjustments are accessable with the assemblies in their card nests. Those adjustments requiring extender boards to access these points will indicate so. The High Voltage Adjustment requires access to the high voltage box through the bottom cover of the instrument as well as to the A13 assembly through the top cover. Most other adjustments can be made with only the top cover and metal shield removed.

## NOTE

> The adjustments requiring extender boards also require the removal of the 3582A metal shield for accessing test points. It is easiest to remove this shield before beginning the adjustment sequence until it is required for the Input Board Adjustments.

### 5.5. SAFETY CONSIDERATIONS.

5-6. This section contains warnings and cautions that must be followed for your protection and to avoid damage to the instrument.

## WARNING

Maintenance described herein is performed with power supplied to the instrument and protective covers removed. Such maintenance should be performed only by service trained personnel who are aware of the hazards involved (for example, fire and electrical shock).

## ECAUTION\}

Always turn the 3582A power "off"' before removing or replacing any of the printed circuit assemblies.

## WARNING

The A13 Display board and A65 High Voltage board contain hazardous voltages capable of causing death. Use extreme caution when working in the proximity of these areas.

### 5.7. ADJUSTMENT SEQUIENCE.

5-8. The adjustment procedures are presented in a logical sequence that will minimize interaction between adjustments. Although the Performance Tests or a servicing process might indicate that only one or two adjustments are needed, we recommend that you start at the beginning and do all of the adjustments in the order in which they are given.

### 5.9. CONTROL SETTINGS.

5-10. The proper control settings for the 3582A are given in the individual adjustment procedures. If control settings are not given, they do not affect the adjustment being performed.

### 5.11. Pre-Adjustment Set-Up.

5-12. This procedure will reset the 3582 A into its turn-on state and insure minimum instrument-to-instrument discrepency.
a. Set all FRAMED buttons ..... On
b. Set SCALE 10 dB /DIV ..... On
c. Set AVERAGE NUMBER 4 ..... On
d. Set all other buttons ..... Off
e. AMPLITUDE REFERENCE LEVEL ..... Normal
f. FREQUENCY SPAN ..... 0-25 kHz
g. TRIGGER LEVEL ..... Free Run
h. INPUT CHANNEL A SENSITIVITY ..... Ca
VERNIER ..... Cal
i. INPUT CHANNEL B SENSITIVITY ..... Cal
VERNIER ..... Cal
j. INPUT MODE ..... A
k. ISOL-CHAS ..... Chas

## 5-13. POWER SUPPLY ADJUSTMENTS.

5-14. These adjustments set the 27 kHz Power Supply Clock, the + and - 18 V References, the +5 V supply voltage and current limit point, the -15 volt power supply, and the CRT high voltage power supply.

## \{CAUTION

The power supply assemblies are located close to the 3582 A fan and should be checked to verify adequate fan clearance after reinstallation.

Equipment required:
Electronic Counter (-hp-5328A)
Digital Voltmeter (-hp- 3455A)
Oscilloscope (-hp- 1740A)
High-Voltage Probe (-hp- 3440A-K05)
10:1 Probe (-hp- 10006D)
Extender board (No. 1) (-hp- 03582-66533)
Load resistor $2.5 \Omega 10$ watt $5 \%$ (-hp- 0811-2844)
Alligator clips (2) (-hp- 1400-0051)

## 5-15. A17 Adjustments.

a. Verify that the 3582A power is OFF.
b. Remove the metal shield to allow access to adjustments and test points.
c. Place the A17 board on the extender board (No. 1).


Figure 5-1. Power Supply Control Board, A17 (Rev C).
d. Set the Digital Voltmeter (DVM) to the DCV function, auto-range.
e. Turn the 3582A power ON.
f. Connect the DVM to A17TP +18 V , low lead to Chassis. Adjust A17R9 for a DVM reading between +18.080 V and +18.120 V . A check of the other supplies on A 17 would be in order here (no adjustment is required for these). Check the following XA17 edge connector pins for the approximate voltages listed:

| Pin | Approximate Voltage |
| :---: | :---: |
| 3 | -24 V |
| 4 | +24 V |
| 5 | -5 V |
| 6 | +5 V |
| 8 | -18 V |
| 15 | +150 V |

g. Connect the Counter To A17TP27 kHz. Adjust A17R15 for a Counter reading between 26.9000 kHz and 27.1000 kHz . (It may take several seconds for the reading to stabilize.)
h. Turn the power OFF, disconnect the DVM and Counter and replace the A17 assembly into its card nest.

### 5.16. A16 Adjustments (+5.1 Volt Power Supply).

a. Set the DVM to the DCV function, auto-range.


Figure 5-2. +5 V Power Supply Board, A16 (Rev D).
b. Turn the 3582 A power ON .
c. Connect the DVM to A16TP +5 , low lead to Chassis. Adjust A16R31 for a DVM reading between +5.0900 V and +5.1100 V . This adjustment is made under steady-state current demands of the 3582A (about 4.5 amps ).
d. Turn the power OFF and connect the $2.5 \Omega$ current-limit load between A16TP +5 and chassis. Alligator clips are a convenient way to connect the load.
e. Turn the power back ON and adjust R19 until DS3 (red current limit LED) just comes on. This adjusts the +5 V power supply at approximately 2 amps above steady-state demands (about 6.5 amps ).
f. Turn the power OFF and disconnect the current-limit load and DVM.

## 5-17. A18 Adjustment ( -15 Volt Power Supply).

a. Set the DVM to the DCV function, autorange.
b. Place the ISOL-CHAS switch in the CHAS position.
c. Turn the 3582A power ON.
d. Connect the DVM to A18TP ( -15 V ), low lead to Chassis. Adjust A18R2 for a DVM reading between -14.8500 V and -15.4500 V .
e. Turn the power OFF and disconnect the DVM.


Figure 5.3. Linear Supply Board, A18 (Rev B).

### 5.18. A13 Adjustments (High Voltage).

## WARNING

Lethal voltages are present on surface components of the A13 board. Use extreme care when working in proximity of this board and always leave the protective plexiglass shield in place. Adjustments and test points are accessable through the shield.

## NOTE

Foldout and refer to Figure 5-12 (shown at end of Section V) throughout the high voltage CRT control and CRT calibration adjustments as necessary.
a. Verify that the 3582A power is OFF.
b. Set the DVM to the DCV function, autorange.
c. Connect the DVM to A13TP +100 V and adjust A13R38 for a DVM reading between +99.000 V and +101.000 V .
d. Turn the power OFF and disconnect the DVM.
e. Set the 3582A front panel controls as follows:

| INTENSITY | ) |
| :---: | :---: |
| ASTIGMATISM | Center |
| FOCUS | Center |
| RATICULE | Fully CCW |

f. Adjust A13R6 (INT. THRESHOLD) full CCW.
g. Turn the 3582 A on its right side and remove the bottom cover.
h. Remove the aluminum cover from the high-voltage box.

## WARNING

Lethal voltages up to 18 kV are present inside the high-voltage box. Use extreme caution when the cover is removed.
i. Connect the calibrated High-Voltage Probe to the DVM and set the DVM to the DCV function, 100 V RANGE (an input resistance of $10 \mathrm{M} \Omega$ is required by the HV probe).
j. Connect the High-Voltage probe to the plated-hole test point on the High Voltage board. The location of this test poin is shown in Figure 5-4.
k. Turn the 3582A power ON.

1. Adjust A13R46 (HV ADJ) for a DVM reading equal to the voltage marked on the high voltage tag in the high voltage box + or $-.25 \%$. If unable to perform this adjustment, recheck the DVM for the proper 100 V range and input resistance before referring to Section VIII, SERVICE.


Figure 5-4. High Voltage Board, A65.

## NOTE

The closer this adjustment is made, the greater the expected life of the CRT will be. An overall adjustment accuracy better than $1 \%$ is desired when the contributions from HV probe, DVM, and tagging accuracy are included.
m . Turn the 3582A power OFF.
n . Make the following preliminary adjustment on the A13 board:
A13R6 (INT THRESHOLD).............................. Fully CW
o. Turn the 3582A power ON.
p. Slide A9S1 into the "TEST" position (back). The display should appear similar to Figure 5-5.
q. Adjust A13R6 (INT THRESHOLD) until the display just disappears.
r. Turn the front panel INTENSITY control until the display reappears.
s. Adjust A65R13 (GROSS FOCUS) for the best display focus.
t. Adjust the front panel ASTIGMATISM control for the sharpest, most well-defined display.
$u$. Repeat Steps $s$ and $t$ to obtain the best display focus.
v. Turn the 3582A power OFF. Replace the high voltage box aluminum cover and the bottom cover. Set the 3582A down off its side (normal upright position).

## WARNING

Be sure all wires are securely inside the high-voltage box before replacing the aluminum cover.

### 5.19. CRT CONTROL ADJUSTMENTS.

5-20. These adjustments set the CRT display intensity, positioning, gain, and alignment to optimum levels.

## Preliminary

a. Make the following preliminary front panel adjustments:

| INTENSITY. | Fully CCW |
| :---: | :---: |
| GRATICULE ILLUMINATION. | . .Fully CW |

b. Turn the 3582A power ON.
c. Adjust A13R105 (FGD) for the most uniform intensity throughout the CRT.
d. Adjust A13R112 (FGN) for a dim flood intensity on the CRT.
e. Verify that A9S1 is still in the "TEST" position from the previous adjustments.

## GRAPHICS ALIGNMENT

f. Refer again to Figure 5-5. Graphics alignment should result in a display quality of this order.
g. Adjust A13R59 (X POS), Al3R85 (Y POS), A13R54 (X GAIN), and Al3R80 (Y GAIN) so that the display is vertically and horizontally aligned with the CRT graticule (Preliminary).
h. Adjust A13R3 (PATT) for the straightest row of A's.
i. Adjust A13R1 (X ALIGN) for the best alignment along the X axis. Align using the row of A's.
j. Adjust A13R2 (ORTHO) for the best vertical alignment. Align using the square wave edges.
k. Repeat Steps $h$ and $j$ for optimum alignment as in Figure 5-5. Some variations cannot be helped. Use the center of the display as a basis for judging the adjustment quality.

1. Adjust A10R14 to critically damp the square waves (eliminate overshoot and overdamping).
m . This completes the graphics alignment. Slide A9S1 back into the "RUN" position (forward) and turn the 3582 A power OFF.


ADJUSTMENT SUMMARY
$X$ POS
$Y$ POS
Y GAIN
X GAIN
PATT
ALIGN
ORTHO
INTEGRATOR

Centers display horizontally (between 16th and 17th A).
Centers display vertically (top of square waves).
Fills graticule vertically (bottom of square waves).
Fills screen horizontally (1st and 32nd A's).
Straightens rows of A's (pincushion adjustment).
Tilts display about X axis.
Adjusts rising and falling square wave edges to be mutually perpendicular to vertical graticule lines.
Adjusts damping on square wave edges.

## NOTE

Some variations in these adjustments cannot be helped. The center of the display is the most critical and should be used as a basis for judging adjustment quality.
Figure 5-5. "Test" Display and Graphics Alignment Adjustment Summary.

## 5-21. DISPLAY CAI.IBRATION ADJUSTMENTS.

5-22. These adjustments calibrate the CRT display using the internally generated self-test displays.

Equipment required:
Digital Voltmeter (-hp- 3455A)
a. Set the DVM to the DCV function, autorange.
b. Connect the DVM to A10TP +10 V .
c. Turn the 3582A power ON. Adjust A10R202 for a DVM reading between +9.9000 V and +10.1000 V .
d. Set the front panel controls as follows:

$$
\begin{aligned}
& \text { NUMBER . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . } 8 \text {. } 128 \text { (released) } \\
& \text { SHIFT. . . . . . . . . . . . . . . . . . . . . . }
\end{aligned}
$$

e. Enter the self-test mode by holding in the restart pushbutton and momentarily pressing the reset pushbutton. Step to display number 3 with the restart pushbutton.
f. Adjust A13R59 (X POS) to place the start of the graphics on the first vertical graticule line.
g. Adjust A10R53 (X REG) to place the start of the alphanumerics on the first vertical graticule line.
h. Adjust A13R54 (X GAIN) to place the end of the alphanumerics on the last (1lth) vertical graticule line. Readjust A13R59 (X POS) to keep the start of the alphanumerics in place as necessary.
i. Adjust A10R 19 (RAMP) to place the last (4th) negative pulse on the last (11th) vertical graticule line.
j. Adjust A13R80 (Y GAIN) and A13R85 (Y POS) to fill the graticule vertically with the graphics.
k. Adjust A10R41 (Y REG) to place the top row of alphanumerics 1 minor division (1/16 inch) below the bottom horizontal graticule line.

1. Adjust A14R42 (Y CHAR) to place the bottom row of the heading 1 minor division above the top horizontal graticule line.
m. Repeat GRAPHICS ALIGNMENT Steps $g$ through $\mathbf{j}$, and $m$, and DISPLAY CALIBRATION Steps a through 1, to obtain the optimum display. All of these adjustments are slightly interactive.


## ADJUSTMENT SUMMARY

$X$ POS Places beginning of graphics on first vertical graticule line.
$X$ REG Places beginning of alphanumerics on first vertical graticule line.
$X$ GAIN Fills graticule horizontally with alphanumerics.
RAMP Places last negative pulse on last vertical graticule line.
Y GAIN Fills graticule vertically with graphics.
$Y$ POS Keeps display centered about the horizontal axis.
$Y$ REG Sets vertical position of alphanumerics.
Y CHAR Sets vertical position of heading.

NOTE
Some variations in these adjustments cannot be helped. The center of the display is the most critical and should be used as a basis for judging adjustment quality.

Figure 5.6. Self-Test Display 3 and Display Calibration Adjustment Summary.


Figure 5.7. Analog Display Driver Board, A10 (Rev C).
n. Step to display number 2 with the RESTART pushbutton, move the marker position potentiometer fully clockwise and back off 1 complete turn.
o. Adjust A10R71 (marker) to just change the marker bin position from 000376 to 000377 as displayed by the 2 nd number from the top on the right side of the display.


Figure 5-8. Self-Test Display 2 and Marker Bin Position.
p. Adjust A13R6 (INT THRESHOLD) so that the vertical and horizontal lines are equally bright. This occurs when they extinguish at the same time with the front panel intensity control.
q. Set the front panel intensity control to maximum (FULLY CW).
r. Set the oscilloscope controls as follows:
VERTICAL..................................................... . . 1 V/DIV
HORIZONTAL . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $1 \mu \mathrm{~s} /$ DIV
INPUT COUPLING . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . DC
s. Connect the oscilloscope to A13TPIL with a $10: 1$ probe. Use the vertical position control on the oscilloscope to position the peaks of the waveform on the top horizontal graticule line.
t. Connect the probe to A13TPZG. Adjust A13R109 for waveform peaks 4 minor divisions ( 8 V ) below the top graticule line on the oscilloscope.
u. Reduce the front panel intensity control to a comfortable level.
v. Turn the 3582A power OFF and disconnect the oscilloscope.

### 5.23. 45.8752 MHz ADJUSTMENT.

Method I.

Equipment required:

Frequency synthesizer: (-hp- 3325A or -hp- 3330B)

Instrument control settings:
3582A: Preadjustment settings
FREQUENCY MODE . . . . . . . . . . . . . . . . . . . . . . . SET CENTER
FREQUENCY ADJUST.......................................... . 25 KHz
SPAN . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 250Hz
SENSITIVITY (Channel A) . . . . . . . . . . . . . . . . . . . . . . . +10 dBm
MARKER . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ON
MARKER POSTION. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 25 KHz

3325A (or 3330B):
FREQUENCY. . . . . . . . . . . . . . . . . . . . . . . . . . . . 25 KHz (sine wave)
AMPLITUDE . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . + 13.01 dBm
a. Connect the synthesizer output to the 3582A CHANNEL A INPUT.
b. Verify that the marker is at the peak of the displayed spectrum. If it is not, adjust A3-C4.
c. Switch the 3582A FREQUENCY SPAN to 250 Hz . In this span the spectrum will be completed in 10 seconds.
d. Repeat Step b. This insures that frequency calibration is within 0.1 Hz . The specification is 0.75 Hz .


Figure 5-9. Timing and Digital Interface Board, A3 (Rev B).
Method II.
Equipment required:
Electronic counter (-hp- 5328A)
Extender board (No. 2) (-hp- 03582-66531)
a. Verify that the 3582 A power is turned OFF.
b. Place the A3 assembly on the extender board (No. 2).
c. Connect the ELECTRONIC COUNTER to A3TP1 (OSC).
d. Turn the 3582A power ON.
e. Adjust A3C4 for a counter reading of $45.8752 \mathrm{MHz} \pm .0001 \mathrm{MHz}$.
f. Turn the 3582A power off, disconnect the ELECTRONIC COUNTER and replace the A3 assembly into its card nest.

## 5-24. BACK-GATE BIAS ADJUSTMENT.

Equipment required:
Digital Voltmeter (-hp- 3455A)
a. With instrument power OFF, remove the A2 assembly and note the voltage marked on A2U16.
b. Set the DVM to the DCV function, autorange.
c. Turn the 3582 A power ON .


Figure 5-10. HP-IB Board, A2 (Rev B).
d. Connect the DVM to A2TP1 (VBG), adjust A2R5 for a DVM reading equal to the voltage noted in Step A $\pm 1 \%$.
e. Turn the power OFF and disconnect the DVM.

## 5-25. INPUT BOARD ADJUSTMENTS (Channels A and B).

5-26. These adjustments set the A to D Clock frequency, Sample-and-Hold DC noise floor, amplitude calibration, and attenuator compensation.

Equipment required:
Oscilloscope (-hp- 1740A)
Synthesizer (-hp- 3330B) Option 005
10:1 probes (2) (-hp- 10006D)
1:1 probe (-hp-10007A)
Extender board (No. 2) (-hp- 03582-66531)
$50 \Omega$ feed thru termination (-hp-11048C)

## NOTE

Foldout and refer to Figure 5-12 (shown at end of Section V) throughout the input board adjustments as necessary.

## 5-27. A-to-D Clock Adjustment.

a. Verify that the 3582A power is OFF.
b. Place A1 (Channel A) on the extender board (No. 2).
c. Set the 3582A front panel controls to:
INPUT MODE ..... A
SENSITIVITY ..... 30 mV
A COUPLING ..... AC (~)d. Set the OSCILLOSCOPE controls to:
Channel A
VERTICAL ..... 1V/DIV
INPUT COUPLING ..... DC
Channel B
VERTICAL .....  005 V/DIV
INPUT COUPLING ..... AC
Others
HORIZONTAL ..... $1 \mu \mathrm{~s} / \mathrm{DIV}$
DISPLAY Alternate
TRIGGER SLOPE (negative)
TRIGGER MODE External
BANDWIDTH LIMIT. ..... Off
e. Connect the OSCILLOSCOPE external trigger input to A1TPH/C with a $10: 1$ probe. Connect the OSCILLOSCOPE Channel A input to A1TPCLK with a 10:1 probe.
f. Turn the 3582A power ON . Adjust A 1 C 145 for $7.7 \mu$ s to $7.9 \mu \mathrm{~S}$ between the rising edges of the 1 st and 13th pulses.

## 5-28. Sample-and-Hold DC Adjustment (also see pictures on page 8-1-10).

g. Short A1TPLPF to ground (A1TPGND) and set the Oscilloscope BANDWIDTH LIMI'T control to ON.
h. Connect the OSCILLOSCOPE Channel B. Input to A1TPS/H using a $1: 1$ probe with a low inductance tip.
i. Adjust A1C141 until the DC (noise) levels between $\mathrm{H} / \mathrm{C}$ pulses are equal.
j. Verify that the droop between the 2 nd and 13 th pulse is $\leq 1 \mathrm{mV}$.
k. Turn the 3582A power OFF. Remove the ground from A1TPLPF and disconnect the OSCILLOSCOPE, then replace the A1 (Channel A) board into its card nest.

1. Repeat Steps a through k for Channel B.

## 5-29. Amplitude Calibration.

m. Set the 3582A front panel controls to:
AMPLITUDE ..... A \& B
SCALE ..... Linear
AMPLITUDE REFERENCE LEVEL ..... Fully CCW
PHASE ..... Both Off
PASS BAND ..... Flat Top
AVERAGE ..... Off
TRACE 1 \& 2 ..... Off
MARKER ..... On
REL ..... Off
FREQUENCY MODE .....  $0-25 \mathrm{kHz}$ Span
INPUT MODE ..... Both
SENSITIVITY. ..... 3 mV (both channels)
A \& B COUPLING ..... AC (~)
TRIGGER LEVEL .....  Free Run
REPETITIVE ..... On
n. Place a short across the Channel A input. Depress and hold the TIME A pushbutton and adjust the front panel Channel A DC BAL for a display line at the center horizontal graticule. Switch through each Channel A sensitivity to verify a DC level within 1 minor division of center for each. Also verify the 3 mV range with DC coupling to within 1 minor division of center. Release the TIME A pushbutton.
o. Repeat Step n for Channel B.
p. Remove any input shorts. Connect the synthesizer to Channels A and B using a 50 ohm feed thru termination and reset the following 3582A front panel controls to:
AMPLITUDE . . . . . . . . . . . . . . . . . . . . . . . . . . A Only (Release B)
INPUT MODE. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 300 mV
q. Set the synthesizer to:

AMPLITUDE. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -7.44 dBm
FREQUENCY. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1 kHz
LEVELING.................................................................. .
r. Set the 3582A marker to 1 kHz . Adjust A1R101 (GAIN) for a marker amplitude reading of 95.0 mV .
s. Set the SYNTHESIZER and the 3582A marker to 22.5 kHz . Adjust A1R45 (LPF) for a marker amplitude reading of 95.0 mV .
t. Set the 3582A sensitivity to CAL and the marker to 1 kHz . Adjust A1R8 (CAL) for a marker amplitude reading of 20.0 volts.
u. Repeat Steps p through t for the Channel B A1 board.
v. Turn the 3582A power OFF.

### 5.30. Input Attenuator Compensation.

w. Verify that the 3582A power is OFF.
x. Re-install the metal shield which was removed for the previous 3582A adjustments.
y. Turn the 3582A power ON .
z. Set the 3582 A front panel controls to:

AMPLITUDE . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . A(Only)
INPUT MODE . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . A(Only)
SENSITIVITY (Both Channels) . . . . . . . . . . . . . . . . . . . . . . . . . 3 V
MARKER POSITION . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1 kHz
aa. Set the SYNTHESIZER to:
AMPLITUDE
12.5 dBm
FREQUENCY
1 kHz
bb. Record the marker amplitude reading, $\mathrm{V}_{10}$
cc. Set the SYNTHESIZER and the 3582A marker to 22.5 kHz . Adjust A1C2(10) for the marker amplitude reading, $\mathrm{V}_{10}$, obtained in the previous step.
dd. Repeat Steps z through cc for the Channel B A1 board. Use the "B" setting for the amplitude and input mode controls.
ee. Remove the 50 ohm feed thru termination and set the 3582A front panel controls to:

> AMPLITUDE . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . A(Only)
> INPUT MODE...................................................... A(Only)
> SENSITIVITY (Both Channels)................................ . . 30 V
> MARKER POSITION................................................ 1 kHz
ff. Set the Synthesizer to:
AMPLITUDE. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 26.54 dBm
FREQUENCY.......................................................... . . 1 kHz
gg. Record the marker amplitude reading, $\mathrm{V}_{100}$ $\qquad$ .
hh. Set the SYNTHESIZER and the 3582A marker to 22.5 kHz . Adjust A1C1 (100) for the marker amplitude reading $\mathrm{V}_{100}$, obtained in the previous step.
ii. Repeat Steps ee through hh for the Channel B Al board. Use the " $B$ " setting for the amplitude and input mode controls.
jj. Disconnect the SYNTHESIZER and turn the 3582A power OFF.

## 5-31. PERIODIC-RANDOM NOISE SOURCE DC ADJUSTMENT.

a. Set the 3582 A front panel controls to:
AMPLITUDE.................................................. A (Only)
SCALE ..... $2 \mathrm{~dB} / \mathrm{DIV}$
PASSBAND ..... UNIFORM
SENSITIVITY ..... $+10 \mathrm{dBV}$
AMPLITUDE REFERENCE LEVEL. . . . . . . - 20 dBV Full Scale
NOISE SOURCE ..... Random
SPAN Set Center-500 Hz Span
CENTER FREQUENCY ..... 1800 to 2000 Hz
b. Connect the noise source output to the Channel A input and turn the noise source level to maximum (FULLY CW). Turn the 3582A power ON.
c. Adjust A4R33 (DC) to eliminate the spike at center frequency.
d. Remove the connection from the noise source output to the Channel A input. Turn the 3582A power OFF.


Figure 5-11. Pseudo-Random Noise Generator Board, A4 (Rev D).


Figure 5.12. X, Y, Z Amplifier and Display High Voltage Control Board, A13 (Rev C).



Figure 5-13. Adjustment and Test Point Locations.

## SECTION VI

## REPLACEABLE PARTS

### 6.1. INTRODUCTION.

6-2. This section contains information for ordering replacement parts. Table 6-3 lists parts in alphanumeric order of their reference designators and indicates the description, HewlettPackard Part Number of each part, together with any applicable notes, and provides the following:
a. Total quantity used in the instrument (Qty column). The total quantity of a part is given the first time the part number appears.
b. Description of the part. (See list of abbreviations in Table 6-1.)
c. Typical manufacturer of the part is a five-digit code. (See Table 6-2 for list of manufacturers.)
d. Manufacturer's part number.

6-3. Miscellaneous parts are listed in Table 6-3 following their respective assemblies. General miscellaneous parts are listed at the conclusion of Table 6-3.

## 6-4. ORDERING INFORMATION.

6-5. To obtain replacement parts, address order or inquiry to your local Hewlett-Packard Field Office. (See Appendix A for list of office locations.) Identify parts by their HewlettPackard part numbers. Include instrument model and serial numbers.

### 6.6. NON-LISTED PARTS.

6-7. To obtain a part that is not listed, include:
a. Instrument model number.
b. Instrument serial number.
c. Description of the part.
d. Function and location of the part.

### 6.8. PROPRIETARY PARTS.

6-9. Items marked by a dagger ( $\dagger$ ) in the reference designator column are available only for repair and service of Hewlett-Packard instruments.

## 6-10. PRINTED CIRCUIT ASSEMBLIES.

6-11. Printed circuit assemblies are listed in Table 6-3. An itemized parts listing of each assembly is located in the service group associated with the assembly. Table 6-3 indicates the service group associated with each printed circuit assembly.

Table 6-1. List of Abbreviations.


Table 6-2. Code List Of Manufacturers.

| Mfr Mo. | Manufacturer Mame | Address |
| :---: | :---: | :---: |
| 00853 | Sangamo Elec Co S Carolina Div | Pickens, SC 29671 |
| 01121 | Allen-Bradley Co | Milwaukee, WI 53204 |
| 01295 | Texas Instr Inc Semicond Cmpnt Div | Dallas, TX 75222 |
| 01928 | RCA Corp Solid State Div | Somerville, NJ 08876 |
| 02111 | Spectrol Electronics Corp | City of Ind, CA 91745 |
| 03888 | KDI Pyrofilm Corp | Whippany, NJ 07981 |
| 04713 | Motorola Semiconductor Products | Phoenix, AZ 85062 |
| 06665 | Precision Monolithics Inc | Santa Clara, CA 95050 |
| 06915 | Richco Plastic Co | Chicago, IL 60648 |
| 07263 | Fairchild Semiconductor Div | Mountain View, CA 94042 |
| 08484 | Breeze Corporations Inc | Union, NJ 07083 |
| 11236 | Cts Of Berne Inc | Berne, IN 46711 |
| 12954 | Siemens Corp Components Group | Scottsdale, AZ 85252 |
| 12969 | Unitrode Corp | Watertown, MA 02172 |
| 13103 | Thermalloy Co | Dallas, TX 75234 |
| 13606 | Sprague Elect Co Semiconductor Div | Concord, NH 03301 |
| 14099 | Semtech Corp | Newbury Park, CA 91320 |
| 18324 | Signetics Corp | Sunnyvale, CA 94086 |
| 19701 | Mepco/Electra Corp | Mineral Wells, TX 76067 |
| 22526 | Berg Electronic Inc. | Cumberland, PA 17070 |
| 23936 | Pamotor Div William J. Purdy | Burlingame, CA 94010 |
| 24355 | Analog Devices Inc. | Norwood, MA 02062 |
| 24546 | Corning Glass Works (Bradford) | Bradford, PA 16701 |
| 27014 | National Semiconductor Corp | Santa Clara, CA 95051 |
| 27167 | Corning Glass Works (Wilmington) | Wilmington, NC 28401 |
| 28480 | Hewlett-Packard Co Corporate HQ | Palo Alto, CA 94304 |
| 29832 | Teledyne Philbrick Nexus | Dedham, MA 02026 |
| 34335 | Advanced Micro Devices Inc. | Sunnyvale, CA 94086 |
| 34371 | Harris Semicon Div Harris-Intertype | Melbourne, FL 32901 |
| 52763 | Stettner-Trush Inc | Cazenovia, NY 13035 |
| 54294 | Cutler-Hammer-Inc Shallcross Mfg Co | Selma, NC 27576 |
| 56289 | Sprague Electric Co | North Adams, MA 01247 |
| 72136 | Electro Motive Corp Sub IEC | Willimantic, CT 06226 |
| 72982 | Erie Technological Products Inc | Erie, PA 16512 |
| 75042 | TRW Inc Philadelphia Div | Philadelphia, PA 19108 |
| 75915 | Littelfuse Inc | Des Plaines, IL 60016 |
| 91637 | Dale Electronics Inc | Columbus, NE 68601 |
| 98291 | Sealectro Corp | Mamaroneck, NY 10544 |
| 99515 | Marshall Ind Capacitor Div | Monrovia, CA 91016 |

Table 6.3. Replaceable Parts.

| Reference Designation | HP Part Number | Oty | Description | $\begin{aligned} & \mathrm{Mfr} \\ & \text { Code } \end{aligned}$ | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }_{\text {A1 }}{ }^{\text {a }}$ | ${ }_{\substack{03582.6550 \\ 0 \\ 0358826502}}$ | $\stackrel{2}{1}$ | INPUT-A/D (ITEMIZED PARTS LIST IN SERVICE GROUP 1) | ${ }_{28480}^{28880}$ | ¢ 0358268501 |
| ${ }^{\text {A }}$ | ${ }^{035982.66503}$ | , |  | 28480 | ${ }^{035582.66503}$ |
| ${ }^{\text {A4 }}$ | ${ }^{\text {03582-65504 }}$ | 1 |  | 28880 | 035622.65504 |
| ${ }^{\text {a }}$ | 03582.66505 | 1 |  | 28880 | 03582.6656 |
| ${ }_{\text {A7 }}{ }_{4}^{66}$ | 03582.66506 03582.66507 | i | * Rom IItemized parts LIST in SERVICE GROUP 4) processor IItemize pahts List in senvice | ${ }_{28880}^{28480}$ | -03582.6556 |
| ${ }_{49}^{48}$ |  | ; |  | $\substack{28480 \\ 2888}^{28180}$ | (03562.6558 |
| ${ }_{4} 10$ | ${ }^{0} 35$ | ; | ITEMIZED PARTS LIST <br> IN SERVICE GROUP 5 ) | 28880 | 03588.66510 |
| ${ }^{411}$ | 03582:65551 | 1 | Front panel switch assy litemized pants list | 28880 | ${ }^{0356286551}$ |
| ${ }^{\text {A12 }}$ | 03588.66512 | , | MSERVICEGROUP MS | 28880 | ${ }^{03882665512}$ |
| ${ }^{\text {A13 }}$ | 035882.68513 | , |  | 28880 | 03362.66513 |
| A14 | 03582685514 | 1 |  | 284 | 0358286514 |
| A15 | 03582.66515 | 3 | SERVICE GROUP 11) | 28880 | 03582.66515 |
| ${ }^{46}$ | 03582.66516 |  | +5v power supply litemized parts list in sehvice | 28880 | 03582.66516 |
| 417 | ${ }^{03582,66517}$ | 1 | Powersuply controller IItemized parts list | 2848 | 03562.66517 |
| ${ }^{\text {A } 18}$ | ${ }^{03562.65518}$ | 1 |  | 28880 | ${ }^{\text {03592.65518 }}$ |
| A19 | ${ }^{03882.68519}$ | 1 |  | 28480 | ${ }^{035822.66519}$ |
| A20 | 03882.65520 | 1 | DIGITAL MOETHER BOARD UTEMIZED PARTS LIST IN SEAVICE GROUP 12) | 2888 | ${ }^{03588266520}$ |
| a65 | 0358264201 |  | HIGH VOLTAGE POWER SPLY (ITEMIZED PARTS LIST IN SERVICE GROUP CHASSIS MOUNTED COMP (ITEMIZED PARTS LIST IN SERVICE GROUP 12) | 28480 | 03562:64201 |

## NOTES

The A7 assembly, 03582-66507 does not include a processor or processor gasket. Order P/N's:

| 09825-67907 | Processor hybrid-new |
| :---: | :--- |
| 03582-69507 | Processor hybrid-exchange |
| 5001-1861 | Processor gasket (Included w/exchange <br> assembly) |

A new processor gasket must be used when replacing the processor. This gasket is fragile and bending can quickly ruin it. The exchange processor assembly includes the gasket.

## SECTION VII <br> BACKDATING

### 7.1. INTRODUCTION.

7-2. This section contains backdating changes which make this manual applicable to earlier instruments. The section is divided into procedural changes and schematic changes. Procedural changes are listed by instrument serial number while schematic and parts list changes are listed by board revision designations.

### 7.3. GENERAL INFORMATION.

7-4. All newer revision circuit boards are usable in older instruments. However, the older instrument may not be able to utilize some of the additional functions (present on the newer circuit boards) which were not supplied as an original capability in the main frame instrument.

## 7-5. Example:

In instruments with serial numbers prefixed 1747A, replacement of the A4 Pseudo Random Noise board with a later revision board will not permit the utilization of the 'RANDOM" noise source capability unless modifications are also made to the Front Panel (All board) and the Mother Board (A20). Note that the "PERIODIC" pseudom random noise source capability is still usable as in the original revision board.

## 7-6. PROCEDURAL CHANGES.

7-7. Current procedures as indicated in the manual apply to all instruments.

SCHEMATIC CHANGES
TABLE OF CONTENTS

| Assembly | Schematic | Begins on Page |
| :---: | :---: | :---: |
| Gen Info | --- | $7-1$ |
| A1 | A | $7-\mathrm{A}-1$ |
| A2 | 0 | $7-0-1$ |
| A4 | E | $7-\mathrm{E}-1$ |
| A4 | P | $7-\mathrm{P}-1$ |
| A5 | D | $7-\mathrm{D}-1$ |
| A6 | G | $7-\mathrm{G}-1$ |
| A7 | F | $7-\mathrm{F}-1$ |
| A8 | H | $7-\mathrm{H}-1$ |
| A9 | J | $7-\mathrm{J}-1$ |
| A10 | K | $7-\mathrm{K}-1$ |
| A13 | M | $7-\mathrm{M}-1$ |
| A17 | U | $7-\mathrm{U}-1$ |

Table 7-1. Circuit Board Revisions.


## REV A.

Schematic:
Use backdating schematic A(A1) REV A.

## Component Locator:

Use component locator on backdating schematic A(A1) REV A.

## Parts Lists:

Use parts list for Rev E A1 board with the following exceptions:

## A1 Backdated Parts Changes REV A

## Change:

| A1C17 | $0160-2585$ | C-F 2000PF 100V |
| :--- | :--- | :--- |
| A1C30 | $0160-3622$ | C-F 0.1UF |
| A1C31 | $0160-3622$ | C-F 0.1UF |
| A1C38 | $0160-3622$ | C-F 0.1UF |
| A1C39 | $0160-3622$ | C-F 0.1UF |
| A1R38 | $0683-1336$ | R-F 13K .05 $1 / 4 \mathrm{~W}$ |
| A1R39 | $0683-1336$ | R-F 13K .05 $1 / 4 \mathrm{~W}$ |
| A1R41 | $0683-6845$ | R-F 680K .05 |
| A1R52 | $0683-6845$ | R-F 680K .05 |
| A1R118 | $0757-0160$ | R-F 604 OHM .01 |
| A1R121 | $0757-0161$ | R-F 604 OHM .01 |
| R1U10 | $1826-0026$ | V CMPTR LM311H |
| A1U17 | $1990-0444$ | PHOTO-ISO |

Delete:

| C149 | $0106-0576$ C-F $.1 \mu \mathrm{f}, 50 \mathrm{~V}$ |
| :--- | :--- |
| C150 | $0160-0576 \mathrm{C}-\mathrm{F} .1 \mu \mathrm{f}, 50 \mathrm{~V}$ |
| R54 | $0757-1094 \mathrm{R}-\mathrm{F} 1.4 \mathrm{ke}$ |
| C23 | $0160-4571 \mathrm{C}-\mathrm{F} .1 \mu \mathrm{f}$ |
| C148 | $0160-2055 \mathrm{C}-\mathrm{F} .01 \mu \mathrm{f}, 100 \mathrm{~V}$ |





## A1, SCHEMATIC A: INPUT BACKDATING

## REV B

Schematic:
Use A1 REV E schematic.
Component Locator:
Use A1 REV E locator.
Parts List:
Use parts list for REV E with the following exceptions

## A1 Backdated Parts Changes REV B

Change:

## A1R118 0757-0160 R-F 604 OHM . 01 <br> A1R121 0757-0160 R-F 604 OHM . 01

Delete:
C149 0160-0576 C-F . $1 \mu \mathrm{f}, 50 \mathrm{~V}$
C150 0160-0576 C-F . $1 \mu \mathrm{f}, 50 \mathrm{~V}$
R54 0757-1094 R-F 1.4ke
C23 0160-4571 C-F $11 \mu \mathrm{f}$
C148 0160-2055 C-F . $01 \mu \mathrm{f}, 100 \mathrm{~V}$

## REV C

Schematic:
Use A1 REV E schematic.
Component Locator:
Use A1 REV E locator.
Parts List:
Use parts list for REV E with the following exceptions.

## A1 Backdated Parts Changes REV C

Delete: C23 0160-4571 C-F. $1 \mu \mathrm{f}$
C148 0160-2055 C-F . $01 \mu \mathrm{f}, 100 \mathrm{~V}$
C149 0160-0576 C-F.1 1 f , 50V
C150 0160-0576 C-F.1 $\mu \mathrm{f}, 50 \mathrm{~V}$
REV D
Schematic:
Use Al REV E schematic.
Component Locator:
Use Al REV E locator.
Parts List:
Use parts list for REV E with the following exceptions:
Delete: C149 0160-0576 C-F .1 1 f, 50V
Cl50 0160-0576 C-F $.1 \mu \mathrm{f}, 50 \mathrm{~V}$

## REV E.

Correct schematic and parts locator are given in this section.



## A5, SCHEMATIC D: DIGITAL FILTER BACKDATING

## REV A.

Schematic:
Use backdating schematic D(A5) REV A.
Component Locator:
Use component locator on backdating schematic D(A5) REV A.
Parts List:
Use current parts list D (A5) with the exception of the parts listed as follows:

## A5 Backdated Parts Changes REV A.

| A5C1 | $0160-2204$ | C-F 100PF 300V |
| :--- | :--- | :--- |
| A5C2 | $0160-2204$ | C-F 100PF 300V |
| A5C3 | To C21 Inclusive |  |
| A5C21 | $0160-3847$ | C-F .01 50V |
| A5C25 | $0160-3847$ | C-F .01 50V |
| A5R3 | $0683-9515$ | R-F 5.1 OHM .05 |
| A5R4 | $0683-0515$ | R-F 5.1 OHM .05 |
| A5R9 | $0683-1025$ | R-F 1000 OHM .05 |
| A5R10 | $0683-1025$ | R-F 1000 OHM .05 |
| A5U12 | $1820-1199$ | TTL INV 74LSON |
| A5U18 | $1820-1197$ | TTL GATE 74LSOON |

## REV B.

Schematic:
Use backdating schematic $\mathrm{D}(\mathrm{A} 5)$ REV A modified by the addition of the following circuit. See current schematic $\mathrm{D}(\mathrm{A} 5)$ for information pertaining to the connection of signal lines into and out of the circuit.


## Component Locator:

Use backdating component locator D(A5) REV A and note the exceptions indicated for REV B.

## Parts List:

Use the current parts list $\mathrm{D}(\mathrm{A} 5)$ with the exception of the components listed as follows:

## A5 Backdated Parts Changes REV B.

| A5C1 | $0160-2204$ | C-F 100PF 300V |
| :--- | :--- | :--- |
| A5C2 | $0160-2204$ | C-F 100PF 300V |
| A5C3 | To C21 Inclusive |  |
| A5C21 | $0160-3847$ | C-F .01 50V |
| A5C25 | $0160-3847$ | C-F .01 50V |
| A5R3 | $0683-0515$ | R-F 5.1 OHM .05 |
| A5R4 | $0683-0515$ | R-F 5.1 OHM .05 |
| A5R9 | $0683-1025$ | R-F 1000 OHM .05 |
| A5R10 | $0683-1025$ | R-F 1000 OHM .05 |

## REV C.

Schematic:
Use backdating schematic D(A5) REV A modified by the addition of the following circuit. See current schematic D (A5) for information pertaining to the connection of signal lines into and out of the circuit. Include REVISION B.


## Component Locator:

Use backdating component locator $\mathrm{D}(\mathrm{A} 5)$ REV A and note the exceptions indicated for REV C.

## Parts List:

Use the current parts list D(A5) with the exception of the components listed as follows:

## A5 Backdated Parts Changes REV C.

A5C3 To C21 Inclusive

| A5C21 | $0160-3847$ | C-F .0150 V |
| :--- | :--- | :--- |
| A5C25 | $0160-3847$ | C-F 0150 V |




## A4, SCHEMATIC E: LOCAL OSCILLATOR

REV A, B, C.
Schematic:
Use the REV D schematic found in service group \#3 with the following change:


## REV B\&C:

Schematic:
Use the REV C schematic as provided in this section.

## Parts Locator:

Use the REV C parts locator as provided in this section.

## Parts List:

(REV B only) use the REV D parts list in service group three with the following exceptions:

Delete: U132

Parts List:
(REV C only) use the REV D parts list with the following exceptions.

> Delete: U132


## A7, SCHEMATIC F: PROCESSOR BACKDATING

## REV A\&B:

Use the REV D schematic except remove the buffers U23C and U22B. Also, modify the clock circuit as follows:

Schematic:


## Parts Locator:

Use the REV A,B parts locator as shown.


## Parts List:

Use the REV D parts list with the following exception.

| Change: | C3 | 0140-0195 | C-F, 130pf 300V |
| :---: | :---: | :---: | :---: |
|  | J2 | 1200-0458 | Socket IC, TL5 |
|  | R25 | 0638-5105 | R-F, 518, 05 |
| Add: | L1 | 9100-1651 | Coil Choke $750 \mu \mathrm{~h}$ |
| Delete | C26,27 | 0160-3847 | C-F . $01 \mu \mathrm{f}, 50 \mathrm{~V}$ |
|  | JR2 | 1258-0141. | Jumper-removeable |
|  | Q23 | 1854-0215 | XSTR-2N3904 |
|  | C25 | 0160-4571 | C-F . $1 \mu \mathrm{f}, .20$ |
|  | R31 | 0683-1015 | R-F 100n, 05 |
|  | R33 | 0683-1025 | R-F 1000』, . 05 |
|  | R29 | 0683-4715 | R-F 470n, 05 |
|  | R32 | 0683-4725 | R-F 4.7k $\Omega$, 05 |
|  | R27,28 | 0683-4735 | R-F $47 \mathrm{k} \Omega .05$ |
|  | R30 | 0683-5625 | R-F 5.6k』, .05 |

## REV C:

REV $C$ is the same as REV D except that the buffers U22B and U23C are not used. The parts locator and parts lists are identical and the schematic is modified by deleting U22B and U23C.


## A6, SCHEMATIC G: ROM BACKDATING

## NOTE 1

Some early ROM boards (instruments with serial number prefixes 1747A-have them) contain an 1816-1195 in the U28 position and an 1816-1196 in the U27 position. In addition these boards contain different ROMS for U1 and U2.

$$
\begin{array}{ll}
U 1 & 1816-1197 \\
U 2 & 1816-1198 \\
U 27 & 1816-1196 \\
U 28 & 1186-1195
\end{array}
$$

To retrofit these boards to the current (REV B) status remove U27 and U28 completely. Remove jumper wire W1 and install jumper wire W2. In addition, order and install the following ROMS:

$$
\begin{array}{ll}
U 1 & 1818-0957 \\
U 2 & 1818-0958 \\
U 3 & 1818-0959 \\
U 4 & 1818-0961
\end{array}
$$

When this modification is complete the new software datecode will be 020151.

## NOTE 2

At serial number 1819A01006 approximately, a new set of ROMS was installed in all 3582A's. The new software datecode is now 020151. If you have software datecode 017536, and should U1, U2, U3 or U4 need to be replaced you must order an entire set of the new software as follows:

U1 1818-0957
U2 1818-0958
U3 1818-0959
U4 1818-0961
Signature analysis for the software is provided in this section.

## REV A.

Use the REV B schematic, parts locator and parts list with the following exception.
Delete: J1-19 7175-0057 Jumper Wire 19ea

Part 2: Overall Data
Datacno. $\mathbf{n 7 0 1 5 1}$
Place A7 J2 to Test

| Place A7 J2 to Test |  |  |  | Place A7 J2 to Test |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Setup: | Clk: | J2(3) | 0000 - | Setup: | CLK | J2(3) $\Gamma$ |
|  | Stop: | J2(4) | HH26 ¢ |  | Stop: | J2(4) |
|  | Start: | J2(5) | HH26 $\Gamma$ |  | Start: | J2(5) |

## Address Bus

| Pin \# |  | Address Bus |
| :---: | :---: | :---: |
| $(1)^{*}$ | 4 PU2 | 7 |
| 2 | 4326 | 6 |
| 3 | $306 C$ | 5 |
| 4 | P9UU | 4 |
| 5 | 1688 | 3 |
| 6 | $7 P O A$ | 2 |
| 7 | 8620 | 1 |
| 8 | $8 A 61$ | 0 |
| 19 | U57U | 10 |
| 22 | $5 H F 8$ | 9 |
| 23 | CAP2 | 8 |

*On any ROM chip except $41,2,28$ and
29.

## Select Addresses

| U24(10) | PPP6 | A11 |
| ---: | ---: | ---: |
| 11 | 7044 | $\overline{\text { A11 }}$ |
| 6 | U616 | A12 |
| 14 | P254 | A13 |
| 2 |  | HH26 |


| Chip Selects |  |
| :---: | :--- |
| 6CC6 |  |
| SACO |  |
| UP98 | $\overline{S C 1}$ |
| 1FFF | $\overline{S C 2}$ |
| 6338 | $\overline{S C 4}$ |
| CP1P | $\overline{\text { SC5 }}$ |
| 4384 | $\overline{S C 45}$ |

## $\overline{\text { STROMS }}$

U26(3) 0000
110000
60000
nata for U7，8，and U15．1
ata for U9，10，and U17．18
Date code 017536

U, 6, \&

826P＋5 Signature 7A70
U7，8，\＆15， 16
U7 and 8 only
9，10，\＆17， 18
Clk：J2（3）」
Clk：J2（3）」

Stop：TP6 $\longleftarrow$ Stop：TP2 」
Start：TP6 ᄀ
Start：TP6 L
+5 Signature 826P＋5 Signature 7A70

U9 and 10 only
Part 3：Data Test For Patch ROMS U1， 2

| M．S．Byte <br> U6 \＆U14 |  | M．S．Byte <br> U6 |  |
| :---: | :---: | :---: | :---: |
|  |  |  |  |
|  |  |  |  |
| 7 | $74 U C$ | 7 | 7PP8 |
| 6 | F9FH | 6 | P656 |
| 5 | F39H | 5 | UAU6 |
| 4 | P68F | 4 | 10F6 |
| 3 | $52 O H$ | 3 | $5 F P H$ |
| 2 | A23U | 2 | APO1 |
| 1 | $973 F$ | 1 | P5F7 |
| 0 | $5 H 98$ | 0 | $42 F A$ |

## M．S．Byte M．S．Byte

$\underset{\text { M．S．Byte }}{\text { U10 } \mathbf{U 1 8}} \underset{\mathbf{U 1 0}}{\text { M．S．Byte }}$

| 7 | 331 H | 7 | $5 P P 3$ |
| :--- | :--- | :--- | :--- |
| 6 | 8766 | 6 | 462 U |
| 5 | 1684 | 5 | $7 C U 7$ |
| 4 | CC2O | 4 | P633 |
| 3 | PCO2 | 3 | 1 C7H |
| 2 | FAHA | 2 | $7 C O 6$ |
| 1 | $41 U A$ | 1 | FA12 |
| 0 | $88 H 7$ | 0 | F39C |

C406
CHC4
5 C 3 H
$63 F P$
61 C 3
O9FA
P7CF
14 AO

| L．S．Byte | L．S．Byte |
| :---: | :---: |
| $\mathbf{U 5} \& 13$ | $\mathbf{U 5}$ |

$\begin{array}{lc}\text { L．S．Byte } & \text { L．S．Byte } \\ \text { U7 \＆} 15 & \mathbf{U 7}\end{array}$

| L．S．Byte | L．S．Byte |
| :---: | :---: |
| U．\＆U17 | U9 |

L．S．Byte
U1

| 7 | 2309 |
| :--- | :--- |
| 6 | 0649 |
| 5 | 8306 |
| 4 | 2AF2 |
| 3 | HC7C |
| 2 | UU18 |
| 1 | CCF2 |
| 0 | $7 C 49$ |

## AB, SCHEMATIC H: RAM BACKDATING

## REV A\&B:

These boards are electrically identical to the REV C board except for the following exceptions:

| Change: | C20 | $0180-0210$ | C-F 3.3 $\mu$ f, 15V |
| :--- | :--- | :--- | :--- |
|  | J1 | $1200-0458$ | Socket IC, T05 |



## A10, SCHEMATIC K: ANALOG DISPLAY DRIVER BACKDATING

## REV A:

Schematic:
Use the REV C schematic with the following changes:


Parts Locator:
Use the REV C parts locator, deleting the above four components.
Parts List:
Use the REV C parts list with the following exceptions:

| Delete: | C46,47 | $0140-0191$ | C-F 56pf, 300V |
| ---: | :--- | :--- | :--- |
|  | C48 | $0160-2199$ | C-F 30pf, 300V |
|  | R23 | $0683-1035$ | R-F 10k, $5 \%, 1 / 4 \mathrm{~W}$ |
| Change: | R40 | $0698-4495$ | R-F 37.4k |
|  | R41 | $2100-3353$ | R-F 20k |
|  | R42 | $2100-3352$ | R-F 1k |
|  | R43 | $0698-4443$ | R-F 4.53k |
|  | R105,106,107 | $1810-0136$ | RSTR NTWRK 216C |
|  | Q6 | $1854-0071$ | XSTR-NPN sps5103 |

## REV B:

Schematic:
Use the REV C schematic with the following changes:


## Parts Locator:

Use the REV C parts locator, deleting R23, C46, C47 and C48.
Parts List:
Use the REV C parts list with the following exceptions:

| Delete: | C46,47 | $0140-0191$ | C-F 56pf, 300V |
| :--- | :--- | :--- | :--- |
|  | C48 | $0160-2199$ | C-F 30pf, 300V |
|  | R23 | $0683-1035$ | R-F $10 \mathrm{k} .051 / 4 \mathrm{~W}$ |

## A2, SCHEMATIC O: HP-IB BACKDATING

## REV A.

Use the REV B schematic, parts list and component locator found in the HP-IB service group. REV B is electrically identical to REV A with the jumper J 4 removed.

## A4, SCHEMATIC P: PSEUDORANDOM NOISE GENERATOR

## REV A:

Schematic:
Use the REV A schematic as provided in this section.

## Parts Locator:

Use the REV A parts locator as provided in this section.

## Parts List:

Use the REV D parts list with the following exceptions.
Add: R64-67 1810-0136 Resistor Network 216C
Delete: R50 0683-1025 R-F 1000 0 , 5\% U11 1820-1197 TTL Gazte 74LS00N

Change: J1-4 1200-0458 Socket, IC T05

## REV B:

Schematic:
Use the REV A schematic as provided in this section with the following changes:


## Component Locator:

Use the REV D component locator found in service group \#3.

## Parts List:

Use the REV C parts list located in this section with the following exceptions:
REV A:

$$
\begin{array}{llll}
\text { Delete: } & \text { U11 } & 1820-1197 & \text { TTL GATE 74LS00N } \\
& \text { R50 } & 0683-1025 \text { R-F, 1000 } \mu .05
\end{array}
$$

Change: R64-67 1810-0136 Res. Ntwrk

## REV B:

Change: J1-4 1200-0458 Socket IC - T05
REV C: No changes.




## A13, M SCHEMATIC: DISPLAY HIGH VOLTAGE BACKDATING

## REV A:

Schematic:
Use the REV C schematic with the following change:


## Parts Locator:

Use the REV A AND B parts locator found in this section.
Parts List: Use the REV C parts list with the following exceptions:

| Change: | R33 | $0698-3228$ | R-F 49.9k $1 \%$ |
| ---: | :--- | :--- | :--- |
|  | R34 | $0757-0442$ | R-F 10k $1 \% 1 / 8 \mathrm{~W}$ |
|  | R112 | $2100-3253$ | R-V 50k $10 \%$ |
| Delete: | CR31 |  |  |
|  | R223,224 | $1901-0041$ | Dio-SI .05Z, 30V |
|  | R225 | $0757-0280$ | R-F $1000 \Omega 1 \%$ |
|  | $0698-3620$ | R-F $100 \Omega 2 \mathrm{~W}$ |  |

## REV B:

Schematic:
Use the REV C schematic with the following change:


Parts List:

Use the REV C parts list with the following exceptions.

| Change: | R33 | $0698-4479$ | R-F 14k, 1\% 1/8W |
| ---: | :--- | :--- | :--- |
|  | Q10 | $1854-0234$ | XSTR 2N3440 |
|  | R105 | $2100-3253$ | R-V 50k $10 \%$ |
| Delete: | R223,224 | $0757-0280$ | R-F $1000 \Omega 1 \%$ |
|  | R225 | $0698-3620$ | R-F $100 \Omega 2 \mathrm{~W}$ |

## Parts Locator:

Use the REV A/B parts locator shown:


## A17, SCHEMATIC U: POWER SUPPLY CONTROL.

## REV A\&B:

Schematic:
Use Schematic U except replace diodes CR20 thru CR23 with a diode bridge, CR1.
Component Locator:
Use A17 REV C except replace diodes CR20 thru CR23 with a diode bridge, CR1.
Parts List:
Use the A17 parts list except replace diodes CR20 thru CR23 (p/n 1901-0924) with CR1 (p/n 1906-0069).

## SECTION VIII

SERVICE INFORMATION

## Circuit Board, Schematic, and Service Group Cross Reference

| Circuit <br> Reference Designator | Schematic Designator | Description | Service Group |
| :---: | :---: | :---: | :---: |
| Al | A | Input Attenuator, LPF | SG1 |
|  | B | Analog to Digital Converter | SG1 |
| A2 | O | HP-IB Interface | SG8 |
| A3 | C | Timing | SG2 |
| A4 | E | Local Oscillator | SG3 |
|  | P | Pseudo Random Noise | SG9 |
| A5 | D | Digital Filter | SG3 |
| A6 | G | ROM | SG4 |
| A7 | G | Processor | SG4 |
| A8 | H | RAM | SG4 |
| A9 | I | Digital Display Controller | SG5 |
|  | J | Digital Display Driver | SG5 |
| A10 | K | Analog Display Driver | SG5 |
|  | Q | X-Y Recorder | SG10 |
| Al1 | N | Front Panel Switches | SG7 |
| A12 | N | Rotary Pulse Generator | SG7 |
| A13 | L | XYZ Amplifiers | SG6 |
|  | M | Display High Voltage | SG6 |
| A14 | R | - 18 Volt Power Supply | SG11 |
| A15 | S | +18, + 12, + 7 Volt Power Supply | SG11 |
| A16 | T | + 5 Volt Power Supply | SG11 |
| A17 | U | Power Supply Controller | SG11 |
| A18 | V | Linear Power Supply | SG11 |
| A19 | U | Power Supply Mother Board | SG11 |
| A20 |  | Digital Mother Board | SG12 |
| A65 | M | High Voltage Power Supply | SG6 |
|  |  | Chassis Mounted Components | SG12 |

## SECTION VIII

## SERVICE INFORMATION

## NOTE

Do not remove any of the covers of the 3582A until you have read the following information.

### 8.1. GETTING STARTED.

8-2. The 3582A has been designed for ease of maintenance. Built-in self test features and dual input channels aid in isolating a problem to a specific area of the instrument or in some cases to a specific component. In order to obtain a minimum of instrument down time and to provide for the greatest amount of troubleshooting efficiency and safety, it is recommended that the Service Information found in General Troubleshooting be read before initiating any troubleshooting procedures.

## NOTE

Before removing any of the instrument covers, be aware of the following cautions and warnings.

GAUTION\}

1. The 3582A contains MOS devices which may become damaged as a result of static discharge.
2. Do not remove circuit boards when the LINE switch is on.
3. Improper adjustment of CRT HIGH VOLTAGE may lead to a shortened CRT life.

## WARNING

The display section of the 3582 A contains high voltages (up to +18 KV ) which may remain present in circuit components EVEN WHEN THE INSTRUMENT IS OFF.

## 8-3. SERVICE SECTION ORGANIZATION.

8-4. The Service Section is divided into General Troubleshooting and 12 service groups.

## 8-5. General Troubleshooting.

8-6. General Troubleshooting contains procedures which aid in determining the area, board, or components in the instrument which contribute to a malfunction. From this information, the determination of the service groups concerning the problem can be made. The five major areas of General Troubleshooting consist of the following:
a. Preliminary Troubleshooting
b. Troubleshooting Hints
c. Self Tests
d. Block Diagram Description
e. Block Diagram

## 8-7. Service Groups.

8-8. The service groups consist of schematics, component locators, parts lists, and troubleshooting procedures for one or more related circuit boards. The service groups are arranged in signal flow order as indicated on the main block diagram. There are also service groups for supporting circuit boards such as Front Panel, HP-IB, Pseudo Random Noise, X-Y Recorder Output, Power Supplies, and Chassis Mounted Components.

### 8.9. GENERAL TROUBLESHOOTING.

8-10. The goal of this section is to define the problem and determine the assembly or assemblies that are the most likely cause. There will be cases when a specific component is isolated as the cause (possibly by the self-tests). Other circumstances may point to several possible assemblies. The point is that different malfunctions will dictate different troubleshooting strategies and we highly recommend following the procedures of this section.

8-11. Unless the technician is very familiar with the instrument and has clearly defined the problem, it is desirable to perform the Preliminary Troubleshooting procedures and then proceed to the troubleshooting hints. These hints will discuss the possible causes of the problem and refer to the appropriate service group(s) for detailed troubleshooting information.

## 8-12. Troubleshooting Guidelines.

8-13. These are generalized hints that the technician should keep in mind while troubleshooting the 3582A.
a. Use the two channels to help troubleshooting!

1. The input (A1) assemblies, containing attenuator, trigger and A/D conversion functions, are identical. They can be exchanged to isolate a problem to the A1 assembly.
2. The digital local oscillator is shared by the two channels while there are separate digital filters for each. Problems in band-analysis modes especially are usually traceable to one or the other. Therefore, if the problem is with both channels, suspect the local oscillator. Problems with one channel only would indicate the digital filters.
b. Use the built-in self-tests; these are described in this section. In some cases, these tests can lead directly to the bad component and in any case they can be used to eliminate possible problem areas if the test for that function passes.
c. Make sure there is actually a malfunction. This is a complicated instrument and some normal operating characteristics may be interpreted as malfunctions. Look in the Hints Section under the malfunction for more detailed information.
d. Don't condemn the processor prematurely. A 'hung-up'" instrument that doesn't respond to the front panel, whose data loading light doesn't flash, or whose display is random dots and flashes is a common failure mode for any microprocessor-based instrument. These problems are usually caused by a periferal assembly malfunction (e.g. the digital filter) causing an error or halt in program execution, not a defective processor. Look in the Hints or Service Group 4 for more information.
e. Refer to the block diagram description for more background on the malfunction after referring to the hints section.
f. Use "cool spray" to help isolate problems. Circuit cooler sprays are widely available and can be very helpful in isolating problems. The most generally used method is to spray selected components to see if the malfunction can be temporarily "cured". If this can be accomplished, the bad component is then isolated. This method will not work all the time, but can be a great time saver.
g. Use signature analysis. The -hp- 5004A signature analyzer is an extremely powerful troubleshooting tool that allows a "window" on a digital node to give a go/no-go test. Without the analyzer, troubleshooting the digital sections of the instrument is difficult and requires much trial and error. If a 5004A is not available, keep in mind that most digital failures involve a line that is stuck high or low. Thus, a little guided probing using an oscilloscope in the suspected area may find the problem, although this can be very time consuming.

## 8-14. Preliminary Troubleshooting.

8-15. Preliminary Troubleshooting is organized according to the following flowchart.


## 8-16. Basic Instrument Operation (Preset Conditions).

$8-17$. Verify that the instrument is non-responsive by the following procedure.
a. Set the instrument controls as follows: (preset conditon)
Button Positions: - ON OFF
Set both framed buttons ..... ON
Set AMPLITUDE A ..... ON
Set SCALE 10 dB /DIV ..... ON
Set AVERAGE NUMBER 4 ..... ON
Set PASSBAND SHAPE ..... FLAT TOP
Set all other buttons ..... OFF
AMPLITUDE REFERENCE LEVEL ..... NORM
FREQUENCY MODE ..... $0-25 \mathrm{kHz}$
TRIGGER LEVEL ..... FREE RUN
INPUT CHANNEL A SENSITIVITY ..... CAL
VERNIER ..... CAL
INPUT CHANNEL B SENSITIVITY ..... CAL
VERNIER ..... CAL
INPUT MODE .....
CRT INTENSITY 3/4 fully clockwise
TRIGGER (Rear Panel) ..... INT
b. Verify that the rear panel line switches are set for the proper line voltage.
c. Connect line power to the instrument and set the LINE switch to ON. The instrument cooling fan should began to run. If it does not run, check the line fuse for proper value and condition. If a good fuse does not restore operation, set the LINE switch to OFF and proceed to Primary Troubleshooting.

## CAUTION\}

If the instrument is not responding, do not leave it running as permanent damage to NMOS II devices may result.
d. If the instrument produces a display as shown in Figure 8-1, then fundamental operation can be assumed and specific operating problems can be pursued. In this case, if the areas of deficiency in performance are known, go to the Troubleshooting Hints and see if the problem is listed. If it is not listed, proceed to the Self Test Section.

## 8-1B. Primary Troubleshooting.

8-19. Primary Troubleshooting provides a procedure whereby a basic determination can be made as to whether the display, the processor, or the power supplies are causing improper instrument operation. Where necessary, branching to a service group will be indicated.

8-20. Perform the following procedure:
a. Verify that the instrument is preset as indicated in the Instrument Operation procedure.
b. Verify the line power is connected and the proper line voltage is set on the rear panel switches.
c. Turn the LINE switch to ON.
d. Observe indications on the front panel and proceed immediately to the following paragraph which has the heading which is most applicable to the situation.


Figure 8-1. The Channel A CAL Signal.

## 8-21. Blank Display.

8-22. If the display is blank, TURN OFF POWER and remove the top instrument cover by first removing the rear corner top feet. Then while unscrewing the retaining screw on the rear center of the cover, slide the cover backward. Remove the shield covering the card nest. Perform the following checks.
a. Low Voltage Power Supply Check. Observe the LED's on the power supply cards located in the rear of the instrument. A green light indicates that there is a voltage output from that power supply. A red light indicates that the power supply is in a current limit condition and further troubleshooting will be necessary. In this case, proceed to Service Group 11, Power Supplies.
b. High Voltage Power Supply Check. While observing the CRT face, slowly increase the GRAT ILLUM control on the front panel. A glowing CRT screen indicates that the high voltage supplies are probably working. If there is no glow whatsoever, proceed to Service Group 6, High Voltage Power Supply, for further troubleshooting.
c. Display Test Pattern Check. Place the slide switch (S1), located on top of the A9 board, to TEST. A display similar to that shown in Figure $8-2$ should be present. If it is not, then proceed to Service Group 5, Display Control, for further troubleshooting.


Figure 8-2. Display Test Signal.

## 8-23. Data Loading Light Not Flashing.

8-24. The DATA LOADING LIGHT on the front panel can give several clues as to the proper operation of the data handling section of the instrument. The main areas of concern are processor operation and digital filter operation. Before beginning the following checks, verify that the instrument is in the preset condition previously described. Perform the following checks.
a. Input Mode Switch Check. Switch the INPUT MODE switch between A and BOTH while observing the SINGLE CHANNEL and BOTH CHANNEL annunciator lights, located in the DISPLAY control grouping. Proper operation is indicated if the lights correspond to the INPUT MODE switch setting. If they do not change, proceed to Service Group 4, Processor.
b. Trigger Lever Check. Verify that the TRIGGER LEVEL control is in the FREE RUN position and the instrument is in the preset state. If the DATA LOADING light is not flashing but the INPUT MODE SWITCH CHECK passed, proceed to Service Group 3, Digital Filter and Local Oscillator. If the problem is not found there, proceed to Service Group 4, Processor.

## 8-25. TROUBLESHOOTING HINTS.

## 8-26. Introduction.

8-27. These hints are intended to simulate what a technician, experienced with the 3582A, would give as advice for fixing a specific malfunction. To save time, they are referenced by malfunction. Find the malfunction from the list below that most closely fits the problem(s) experienced, then go to Table 8-1.

> Band-analysis problems
> Data loading light not flashing
> Display problems
> Distortion
> Frequency adjust inoperative
> Front Panel not responding
> Front Panel programming errors
> HP-IB problems
> Marker problems

No spectrum
Noise source problems
Noisy spectrum
Overload indication
Processor not running
Trace shift
Trigger problems
Turn-on problems
X-Y recorder output

Table 8-1. Troubleshooting Hints.
Band-Analysis Problems. These are problems that are associated with these frequency modes only (set-start and set-center). Typically, the noise floor may meet specifications in $0-25 \mathrm{kHz}$ and 0 -start and fail in band-analysis. These problems are invariably caused by the digital local oscillator or the digital filters. Fortunately, it is quite easy to isolate the problem.
a. Since the local oscillator signal is shared by both channels, it is most likely the cause if the problem appears on both channels.
b. The front panel digital filter self-test is quite complete and can lead directly to the bad digital filter IC.

If the problem is that the local oscillator frequency is not right, realize that there is a circuit for 100 Hz multiples and one for interpolating between these. It is thus possible for the L.O. to be correct for a frequency of 500 Hz and incorrect for 501 Hz . Note that the L.O. frequency is always the programmed center frequency.

Service information for the L.O. and digital filters is contained in Service Group 3.
Data Loading Light Not Flashing. This light indicates that a new time record is being taken. It won't flash if the processor is "hung-up" or if there is no trigger signal (or a problem with the trigger circuit). The first thing to do is to check for a non-running processor, as in Primary Troubleshooting. If the processor is running and the trigger level control is in free run, check the trigger circuits on the A5 assembly (digital filter), Service Group 3. See also Hints under trigger problems. The signal line for this function is labeled "DLITE".

Display Problems. Display problems can be caused by the display circuits themselves, a defective power supply or the processor, ROM or RAM. The problem can be easily isolated using the test switch on the A9 assembly. This switch, in TEST, will display all " $A$ ' $s$ ' in the alpha, and a square wave. If this test passes, the display circuits are working and the problem is most likely with the processor, ROM or RAM. Test failure points to the display circuits, A9,A10 or High Voltage.
a. Low voltage power supply troubleshooting information can be found in Service Group 11.
b. Processor, ROM and RAM information is in Service Group 4.
c. If graticule illumination is working, the High Voltage Power supplies are probably OK. Refer to Service Group 5 for the display circuits and Service Group 6 for the high voltage section.

## NOTE

Graticule illumination is not highly visible in normal room light. This is normal and there is sufficient illumination for taking photographs.

Distortion. Distortion is most usually caused by the buffer, S/H or A/D converter circuits on the input (A1) assembly. The easiest way to track down a bad distortion problem is to probe on the bad channel and run that signal into the working channel. That is, a signal that is taken off the S/H test point on the bad channel should look undistorted when run through the input of the other channel - unless the cause of distortion is before the $\mathrm{S} / \mathrm{H}$. The same holds for points before the S/H TP.

The above of course assumes that the problem is on the input board. Always exchange the input boards to make sure that the problem "follows" the suspected assembly. Distortion problems can also be caused by a bad shift register on the data reverse interface (A3, Service Group 2), a bad L.O. or bad digital filter.

Table 8-1. Troubleshooting Hints (Cont'd).
Frequency Adjust Inoperative. This is the control that can be used to adjust the center and start frequencies in band-analysis. There is a test in the front panel switch test. If this doesn't work, first check that the cable is connected to the RPG (Rotary Pulse Generator).

Note that this is not a potentiometer, but rather a pulse generator that puts out pulses proportional to rotational speed and distance. The processor counts the pulses and increments the frequency accordingly. The control actually has three speeds that can increment the frequency in 1 Hz to kHz steps.

Front Panel Not Responding. If the instrument is in a valid operating mode, this is caused by a non-running processor (Service Group 4). For valid operation, make sure that there are no diagnostic messages on the screen. If there is no response to the frequency adjust control (RPG), refer to the hints under "Frequency Adjust Inoperative'". If there is no response to the trigger level control when out of free run, check that the rear panel int/ext trigger switch is in the correct position.

Keep in mind that the instrument will not respond to any switch except "Local" when in the remote mode as programmed over the HP-IB. However, all the potentiometers will be fully operational. This also holds when the instrument is in the "Plot" mode. It will not respond to front panel inputs until the plot is finished or the RESET button is pushed.

Front Panel Programming Errors. Programming information is latched off the processor I/O bus by A4 U1 29 and then sent to the A1 assembly. Refer to Service Group 1 for the A1 assembly and Group 3 for the A4.
HP-IB Problems The HP-IB board (A2, Service Group 8) can cause a variety of problems. It can cause the processor to "hang-up" all the time or only in certain modes of operation. It may cause data to be false even though normal bus activity seems to be taking place.

To establish that the HP-IB board is at fault, remove the board from the instrument after turning off the LINE switch. Then, turn the LINE switch to the ON position and check the instrument to see if it functions properly in the manual modes of operation. Other problems with the HP-IB board may be established by consulting Service Group 8.

Marker Problems. If the marker is not working, first check the front panel cable connection to the position control.

The marker control adjusts a voltage that is compared to the sweep ramp. At coincidence, the address in RAM of that display point is latched and sent to the processor upon request. The processor determines the amplitude and frequency of the point and returns instructions to the A9 board which intensify the dot. If an HP-IB controller is available, the problem can be localized as follows:
a. If the marker works when programmed over the HP-IB, the problem is probably with the A9 or A 10 boards.
b. If the marker does not work over the HP-IB, the problem is probably with the Processor or RAM circuits (A7 or A8).

No Spectrum (Alphanumerics are OK). If the DATA LOADING light is flashing, the triggering circuits are probably working. If it is not flashing, refer to the Data Loading light hints.

Data passes through the Input board (A1), the Timing board (A3), and the Digital Filter board (A5). See the Block Diagram and check these areas if no spectrum is

Table 8-1. Troubleshooting Hints (Cont'd).
displayed. The Local Oscillator must be operating even if the instrument is not in the band analysis modes. Check the Local Oscillator (A4) for proper data output.

Noise Source Problems. The Noise Source Output (A4 Service Group 9) is derived from a pseudo random binary sequence generator. It receives its inputs from the Timing board (A3) and the Local Oscillator board (lower half of A4). Some apparent problems may be caused by the DC Adjustment being out of tolerance (see Adjustments, Section V). For malfunctions, see Service Group 9 and/or Service Group 3.

Noisy Spectrum. The hints under Band Analysis Problems. Also see Service Group 1.
Dverload Indication. The front panel LED's indicate an overload when there is an input which is at or above full scale (in the LOG mode) and will go out when the signal is removed or the SENSITIVITY is increased. CRT indicated overloads remain in effect after the signal is removed for one additional time record period. In the case of an averaging sequence, the overload will remain on until the end of the sequence.

Analog overloads are detected on the Input board (A1), converted to a TTL level, and OR'd with a data overload signal on the Digital Filter board (A5).

Overloads may appear as a result of an illegal turn-on condition (i.e. cycling the LINE switch on and off rapidly).

Processor Mot Running. The processor may be "hung-up" by the HP-IB board (A2 Service Group 8), by the Digital Filter board (A5 Service Group 3), by the ROM board (A6 Service Group 4), or by the Front Panel (A11,A12 Service Group 7). It is possible that any board connected to the I/O Bus may hold data lines down giving the appearance of a locked up processor. For troubleshooting, see Service Group 4.

Trace Shift (of recalled or second trace). This is usually caused by A10C20 (Service Group 5) not discharging fully for the second sweep.

Triggering Problems. The trigger circuits initiate data loading except when the instrument TRIGGER LEVEL control is in the FREE RUN position. If the DATA LOADING light does not operate when the TRIGGER LEVEL is in the FREE RUN position, go to the hints concerning the DATA LOADING LIGHT.

With a proper input signal, the TRIGGER LEVEL centered, and no data loading taking place, check the rear panel EXT TRIGGER switch to be sure it is in the INT position. If problems still persist, check the trigger signal paths on the A1 board in Service Group 1 or the trigger generating circuits on the A5 board, Service Group 3.

Turn-On Problems. Instrument turn-on problems are almost always associated with the processor. If the main processor is "hung-up" for any reason, digital data and even some analog paths may be interrupted or completely non-functional. The processor is associated with boards A1 through A12. A most likely suspect is the A2 HP-IB board, see HP-IB Problems in the hints section. The A11 and A1 2 front panel boards handle the processor CLEAR command and may possibly prohibit turn-on.

On the A7 Processor board itself is the power up circuit. Rapid cycling of the LINE switch may cause the processor to jump into illegal subroutines from which exit is impossible. Allow five seconds between OFF and ON cycles of the LINE switch to assure proper operation of the power up circuit. For more information, see Processor Not Running hints or refer to Service Group 4.

X-Y Recorder Output. The X-Y Recorder outputs are analog signals which are derived form digital to analog converters that receive latched data directly off of the instrument I/O Bus. Therefore, the processor must be operating correctly for proper recorder data output. For troubleshooting, see Service Group 10, A10 X-Y Recorder.

## 8-28. FRONT PANEL ACCESSIBLE SELF-TEST.

## 8-29. To Start.

8-30. Hold "AVERAGE RESTART" key in while RESET key is pressed and released.

## NOTE

The RESET key will not work if HP-IB status is REMOTE. Return HP-IB status to LOCAL before running self-test.

The self-test software will execute Test 0 , the front panel test, when AVERAGE RESTART is released.

### 8.31. To Select A Test Routine.

8-32. Select the desired test from the list below with the AVERAGE NUMBER and SHIFT keys, then press and release AVERAGE RESTART. Test programs in RU status will not recognize the AVERAGE RESTART key until the test is completed, and some programs in CY status will only recognize the AVERAGE RESTART key afer a noticeable delay. The display is blanked when the AVERAGE RESTART key is recognized.


Figure 8-3. Display Test Readouts.

## 8-33. Display.

8-34. Information concerning the test pragram and the results of its test is presented on the CRT display in the format shown in Figure 8-3. The top line of the alphanumeric display gives the test ID number as a 6-digit octal number, the test status ( 2 -character alphanumeric) and the software date code ( 6 -digit octal). The meaning of these codes is explained further below.

8-35. Twelve test condition codes 0 thru 11 may be displayed on the remaining lines of the
display in the positions indicated. Test condition codes are always either 6 -digit octal numbers or blanks, except for the display test program, where the bottom two lines of the display are used for an alpha test pattern.

### 8.36. Status Code.

8-37. The test status code may be one of the five codes listed below. The status code indicates the status of the current test and whether or not errors have occurred. Refer to the descriptions of individual test programs for more information.

## Status <br> Meaning

CY Cycle. The test is cycling and may or may not be testing for errors. If the program is testing for errors, none have occurred.

RU Run. The test is running and testing for errors. At the end of the test, the status will change to either OK or ER. Programs in RU status ignore the AVERAGE RESTART key.

OK Test Passed. The test is halted after finding no errors. The AVERAGE RESTART key will be recognized.

ER Error. The test is halted and errors have occurred. Information about the error or errors which occurred is contained in the condition codes.

XT No Test. There is no test program running. Choose a different test number.

## 8-38. Test Programs.

8-39. The following test programs are accessed by setting the AVERAGE NUMBER and SHIFT keys for the average number indicated.

| Test ID No. (Octal) | Average Number | Test Function |
| :---: | :---: | :--- |
| 000000 | 4 | Al1 \& A12 Front panel board test |
| 000001 | 8 | Display \& marker test |
| 000002 | 16 | A4 digital filter board test |
| 000003 | 32 | A6 ROM board test |
| 000004 | 64 | A8 RAM board GALPAT test |
| 000005 | 128 | Recorder output test |
| 000006 | 256 | Special - Refer to Paragraph 8-79 |

8-40. Front Panel Test (000000).
8-41. Function. Test the switches, RPG circuits, and I/O bus buffers on the A11 \& A12 front panel board. Six of the front panel LED indicators (SRQ, LISTEN, TALK, REMOTE, SINGLE CHAN, and DUAL CHAN) are lit when the test is selected. Since these same indicators are extinguished when the AVERAGE RESTART KEY IS RECOGNIZED, THEY SHOULD LIGHT WHEN THIS TEST IS SELECTED AND GO OUT WHEN AVERAGE RESTART is depressed.

8-42. Status Code. CY only. The program does no internal checks for errors.
8-43. Condition codes 6 and 7 show the current RPG count and the most recent RPG increment, respectively. With the FREQUENCY MODE switch in the $0-25 \mathrm{kHz}$ SPAN or 0 START positions these numbers should remain unchanged when the FREQUENCY ADJUST knob is turned. When the FREQUENCY MODE switch is in the SET START or SET CENTER positions, however, condition codes 6 and 7 should respond to the FREQUENCY ADJUST knob.

8-44. Condition code 6, RPG count, should count up or down as the FREQUENCY ADJUST knob is turned right or left, with limits on the RPG count of 000000 thru 061777 (octal).

8-45. Condition code 7, RPG increment, shows the most recent change in the RPG count, and it should be possible to see the values 000001,000005 , and 000036 while turning the FREQUENCY ADJUST knob right at low, medium, and high velocity, respectively. Similarly, turning the FREQUENCY ADJUST knob left at low, medium, and high velocities should give RPG increments of 177777, 177773, and 177742, respectively. When the RPG count arrives at either of its limits, the RPG increment may be left with a value different from those listed above; but, otherwise, errors in the RPG increment indicate front panel malfunctions. In particular, negative increments while adjusting right, or positive increments while adjusting down indicate errors.

8-46. Condition codes 0 thru 4 show the current values of the switch status registers 0 thru 4, respectively, as read from the front panel board. The bits of the switch status words correspond to front panel switches as shown in Table 8-2. Note that the displayed words are an octal representation of the bit pattern (e.g. LSB of displayed word corresponds to bits 0,1 and 2).

Table 8-2. Condition Codes.

| Cond. Code 0: |  | Bit \# |
| :---: | :---: | :---: |
| Start Freq Band Analysis Baseband (default: 025 kH ) |  | 15 |
|  |  | 14 |
| Unused (always set) Freq Range (default: $\times 1$ ) |  | 13 |
|  | $\times 10$ | 12 |
|  | $\times 100$ | 11 |
|  | $\times 1 \mathrm{~K}$ | 10 |
|  | $\times 10 \mathrm{~K}$ | 9 |
| Unused |  | 8 |
| Freq (default: 1) | 2.5 | 7 |
|  | 5 | 6 |
| Repetitive Mode <br> Trigger Arm <br> Trigger Mode |  | 5 |
|  |  | 4 |
|  |  | 3 |
| Hann Passband Flat Top |  | 2 |
|  |  | 1 |
| Center Freq Band Analysis |  | 0 |

Table 8-2. Condition Codes (Cont'd).

| Cond. Code 1: |  | Bit \# |
| :---: | :---: | :---: |
| Trace 1 Store Trace 2 Store |  | 15 |
|  |  | 14 |
| Channel Select | B | 13 |
| (default: both) | A | 12 |
| Trace 1 Recall Trace 2 Recall |  | 11 |
|  |  | 10 |
| Time B <br> Time A |  | 9 |
|  |  | 8 |
| Ampl Scale (default: Lin) | 10dB/Div | 7 |
|  | $2 \mathrm{~dB} / \mathrm{Div}$ | 6 |
| Phase | XFR FCTN | 5 |
|  | B | 4 |
|  | A | 3 |
| Amplitude | XFR FCTN | 2 |
|  | B | 1 |
|  | A | 0 |
| Cond. Code 2: |  | Bit \# |
| Amplitude Reference (default: pos 1) | Pos 2 | 15 |
|  | 3 | 14 |
|  | 4 | 13 |
|  | 5 | 12 |
|  | 6 | 11 |
|  | 7 | 10 |
|  | 8 | 9 |
|  | 9 | 8 |
| Channel B* Input Sensitivity | D | 7 |
|  | C | 6 |
|  | B | 5 |
|  | A | 4 |
| Channel $\mathrm{A}^{*}$ Input Sensitivity | D | 3 |
|  | C | 2 |
|  | B | 1 |
|  | A | 0 |
| *See Schematic N. |  |  |
| mote |  |  |
| Interpreting Table 8-2: An Example. |  |  |
| Say condition code $O$ reads 105321. The octal equivalent of the rightmost bit (LSB) is 001. From the table, this implies thast SET CENTER band analysis mode is selected and neither FLAT TOP nor HANNING passband shapes are selected. The binary equivalent of octal 2 is 010. From the table, this implies that the trigger is armed, in free run (not trigger mode) and non-repetitive. The interpretation continues in this fashion. |  |  |

Table 8-2. Condition Codes (Cont'd).


## 8-47. Display Test (000001).

8-48. Function. Writes one of 5 display test patterns and 2 lines of alphanumerics test pattern to test the display circuitry. The display test pattern is changed by re-selecting this same test with the AVERAGE NUMBER and AVERAGE RESTART keys. The display marker should appear, and the MARKER POSITION knob should function regardless of the MARKER ON key in display test pattern 2.

8-49. Status Code. CY only. The program performs no internal tests for errors.
8-50. Condition Codes. Condition code 8 shows the current display test pattern number. There are 5 display test patterns numbered 0 thru 4 , which all consist of the same basic bit pattern in the RAM display area, displayed with different display board program modes. The correspondence between display test pattern number and display mode is as follows.

| Test Pattern \# | Display Mode | Blanking |
| :---: | :---: | :---: |
| 0 | $4 \times 128$ | last $3 \times 128$ |
| 1 | $4 \times 128$ | last $2 \times 128$ |
| 2 | $2 \times 256$ | last $1 \times 256$ |
| 3 | $2 \times 256$ | none |
| 4 | $1 \times 512$ | none |

8 -51. Condition code 11 shows the current marker register only in display test pattern 2 . In addition, the marker dot should appear on the display trace and move with the MARKER POSITION knob. Condition code 11 should increment and decrement smoothly between 000000 and 000377.

8-52. Hardware SA tests are available to verify that the A9 digital display driver is receiving the proper data from the A8 RAM board during the display test (see Service Group 5).

### 8.53. A5 Digital Filter Board Test (000002).

8-54. Function. The digital filter board is tested in one of 8 filter test modes, automatically stepping to the next mode if no errors occur. If an error is detected, the test program is halted, and re-selecting the program with the AVERAGE NUMBER and AVERAGE RESTART keys will manually step the filter test mode.

8-55. The DATA LOADING indicator on the front panel is controlled by the digital filter board, and this indicator should remain on except for a slight flicker when filter test mode changes. This indicator should go out when the test halts because of an error, or when a different test program is selected. The two OVERLOAD indicators may or may not flash regularly or sporadically during this test.

8-56. Status Codes. CY when cycling thru the filter tests modes without error. Status changes to ER when an error is detected, and the program halts.

8-57. Condition Codes. Condition code 8 indicates the filter test mode in which the digital filter board is currently being tested. The 8 test modes are numbered 0 thru 7 and they test the board as follows.

| Test Mode (oct) | Filter Chips Tested | Corresponding <br> Instrument Mode |
| :---: | :---: | :--- |
| 000000 | 2 | None |
| 000001 | 1 | Chan A Baseband |
| 000002 | 3 | Chan B Baseband |
| 000003 | 1,3 | Dual Chan. Baseband |
| 000004 | 4 | None |
| 000005 | 1,2 | Chan A Zoom |
| 000006 | 3,4 | Chan B Zoom |
| 000007 | $1,2,3,4$ | Dual Chan Zoom |

8-58. When the test status changes from CY to ER, condition code 9 indicates the type of error detected and the digital filter chip or chips from which erroneous outputs were detected. If condition code 9 is 177777, it means that not enough DMA output requests were given by the digital filter board in the allotted time. No tests are made on the data actually received, and no further information is displayed in the condition codes.

8-59. A condition code 9 of other than 177777 means that enough data was received from the digital filter board, but that the data was erroneous. The testing procedure consists of initializing one or more of the digital filter chips in a test configuration, then examining the first 6 samples of the output transient response. If any of these outputs is in error, the program notes the number of the digital filter chip outputting the erroneous data in an octal digit of condition code 9 . Thus the digits of condition code 9 form a list of chips from which bad data was received.

8 -60. For example, if condition code 9 is 000003 , bad data was received from filter chips 1 and 3. If chips 2 and 4 were involved in that particular test mode (condition code 8), their outputs were correct.

8-61. When erroneous output data is received, condition codes 0 thru 5 are the exclusive OR of the 6 samples received and the expected data. That is, a 1 bit in one of these condition codes indicates that the data bit received in that position was wrong - either a 0 for an expected 1 or a 1 for an expected 0 . When more than one erroneous chip is indicated in condition code 9 , the errors in condition codes 0 thru 5 are from the chip indicated by the rightmost digit of condition code 9 .

## 8-62. A6 ROM Board Test (000003).

8-63. Function. Performs a chip-by-chip signature analysis test on the ROM board to detect malfunctioning ROM chips. The last 2 bytes of each ROM chip are special words which make the internal SA-type signature of that chip be 000000 . If a signature is found to be other than this, an error has occurred somewhere in the bits output from the ROM chip under test. Since the signature register for each chip is preset with bits representing the start address and byte position (high or low), this test also detects improperly loaded ROMs.

8-64. This program does not test software consistency. If, for example, a software revision requires two ROMs to be replaced, and only one of these has been replaced, the software is inconsistent in that only half the revision has been made. The instrument would probably not function with such a ROM board, but the ROM board test would not indicate any errors.

8-65. Status Codes. Test program status is RU while the test is being performed. After approximately 5 seconds, the status changes to OK or ER, depending upon whether errors were detected. During RU status, the AVERAGE RESTART button is ignored.

8-66. Condition Codes. Condition codes 0 thru 9 indicate the chips from which errors were detected. Condition codes are not written for chips from which no errors are detected. The left-most 4 octal digits of the condition code are a "ROM address" which indicates the pair of ROM chips from which errors were detected. The right-most two digits are set to 1 or 0 to indicate whether or not errors were detected in the high byte and the low byte as in this example:

Rom Address


High Byte
Error
8-67. Table 8-3 relates error codes to the corresponding bad I. C. for both the ROM and RAM front panel self tests.

Table 8-3. Error Codes for ROM and RAM Tests.

| Error Code |  | Bad Ram Chip |
| :--- | :--- | :--- |
| 000 | 001 | U1 |
| 000 | 002 | U 2 |
| 000 | 004 | U 3 |
| 000 | 010 | U 4 |
| 000 | 020 | U 5 |
| 000 | 040 | U 6 |
| 000 | 100 | U 7 |
| 000 | 200 | U 8 |
| 000 | 400 | U 9 |
| 001 | 000 | U 10 |
| 002 | 000 | $\mathrm{Ul1}$ |
| 004 | 000 | U 13 |
| 010 | 000 | U 14 |
| 020 | 000 | U 15 |
| 040 | 000 | U 16 |

8-68. A8 RAM Board "GALPAT" Test (000004).
8-69. Function. Performs a "GALPAT" test of the RAM board to try to detect infrequent bit errors, data-sensitive errors, etc. For more catastrophic RAM board malfunctions, the self test programs will probably not work anyway.

8-70. This test produces a number of effects on the display which may seem to be errors or program "bombs". These arise from the fact that the display buffer is tested along with the rest of the RAM array, and the effects are discussed further under "Status Codes" which follow.

8-71. Status Codes. When first selected, the test program goes into the RU status and displays the RU status code in the normal manner. However, this display remains for only a few seconds, until the memory test actually begins. During the memory test, which lasts approximately 12 minutes, the display may have blanked alpha and a bright line at the top of the screen or 4 lines of A's and a line at the bottom of the screen. Each of these patterns lasts about 6 minutes and is marked by a moving dot and alpha character about 4 minutes after
the pattern begins. Throughout the 12 -minute test, the program is in RU status and cannot be interrupted by the AVERAGE RESET key.

8-72. At the end of the test, the status OK or ER is displayed in the normal status code location, but the test ID number and software date code remain blank.
8.73. Condition Codes. Only in ER status, condition code 9 shows accumulated error bits. Since each RAM chip stores one bit of the 16 bit word, a single bit set in condition code 9 would focus suspicion on a unique RAM chip on the RAM board. See table 8-3.

## 8-74. Recorder Output Test (000005).

8-75. Function. To test the X-Y recorder DAC's and the pen-up relay. The X-Y recorder output registers are loaded with a word containing a single 1 bit and all the rest zeroes. Both the X and Y registers are loaded with the same number, and the 1 bit is shifted each time this test is re-selected with the AVERAGE NUMBER and AVERAGE RESTART keys. Thus, a voltmeter can be used to check each bit of the DAC outputs.

8-76. For the X-Y output registers, bits $0-9$ are X-Y output bits, while bit 10 controls the pen-up relay. When the X-Y output word (see "Condition Code" Paragraph 8-78) is octal 002000 , the pen-up relay should close, and the X-Y outputs should be zero.

8-77. Status Code. CY only. Performs no internal checks for errors.
8-78. Condition Code. Condition code 8 displays the octal number loaded into the $\mathrm{X}-\mathrm{Y}$ output registers.

## 8-79. Special Test (000006).

8-80. Function. This test is normally not accessible and no test is run if test 6 is selected in the usual manner.

8-81. However, if jumper J4 on the A7 Processor board is shorted, and test 6 is selected, a test program to produce stable SA signatures on the I/O bus is run. The program performs no internal tests for errors, and a digital SA instrument must be used to check for I/O bus errors.

8-82. Note that having jumper J4 on the Processor board shorted at the time the RESET key is released will cause the primitive ROM self-test to be run, rather than these self-test programs. Thus, the Processor board must not be shorted when these self-test procedures are started, but should be shorted before test 6 is selected.

8-83. The test exercises one of the $16 \mathrm{I} / \mathrm{O}$ select codes ( 0 thru 17 octal) one at a time. Reselecting test 6 with the AVERAGE NUMBER and AVERAGE RESTART keys steps the I/O select code number. Since octal 14 is the display mode program I/O select code, running the test for this case produces anomalous behavior of the display which is not harmful to the display hardware, and should not be mistaken for a display malfunction.

8-84. Status Codes. Status code XT is displayed when the Processor board jumper is not present and no test is being run. Status code CY is displayed while the test is actually running.

8-85. Condition Codes. Condition code 8 shows the octal I/O select code currently under test in status CY.

## 8-86. BLOCK DIAGRAM DESCRIPTION.

### 8.87. Understanding The Instrument.

8-88. The 3582A incorporates Discrete Fourier Analysis which is primarily a firmware function. Therefore, the majority of the instrument contains the digital logic necessary to implement these functions leaving the analog circuits for input and display purposes. Fold out the block diagram at the end of the Service Section.

8-89. Notice on the block diagram that most of the boards have some connection with the I/O Bus. The I/O bus transmits data and instructions between the processor and other bus connected boards. Each of the boards has an interface buffer that permits the appropriate sequencing to allow only two devices to communicate at one time. The processor controls the I/O buffers and, except for the display section and power supplies, should be operating to facilitate troubleshooting other areas of the instrument.

## 8-90. Signal Flow.

8-91. With the processor operating the instrument, the signal data flows from the input boards to the CRT display as given by the following description.

## 8-92. Input p/o A1 (A).

8-93. The channel A and channel B input boards are identical with their function depending on the installed location in the instrument. The signal enters the input boards via a coaxial cable from the front panel. The 1 megohm input termination is located on the board and follows the input attenuator. The signal passes through the termination and into the attenuator, which is programmed by data retained in the program buffer.

8-94. The program buffer receives its data from an I/O buffer located on the A4 Local Oscillator board. Except for the analog input and power supplies, all other inputs and outputs from the board are TTL in nature and optically isolated to allow for a floating input. The attenuator uses reed relays to switch in and out different sections. The CAL signal (which is a pseudo random binary sequence) is switched into the input circuits following the attenuator. Two gain controlled input amplifiers are separated by a $0-11 \mathrm{~dB}$ variable attenuator. The programmable amplifier gains and the programmable input attenuator offer combinations of gain and attenuation which allow an input signal to be referenced to a full scale value on one of ten input ranges ( 30 V to 3 mV ).

8-95. The trigger circuit uses this signal in conjunction with a trigger reference voltage (from the front panel trigger level control) to produce a TTL output (on channel A only) for the Digital Filter A4. An out of band low level signal is injected into the main signal path from the dither circuit to exercise the analog to digital converter and improve its response. This combination of signals is applied to the antialiasing 25 kHz low pass filter. The signals are now ready for processing by the analog to digital converter.

## 8-96. Sample Hold and Analog to Digital Converter p/o A1 (B).

8-97. A sample hold and conversion operation is initiated by a pulse from the A3 Interface
and Timing board. The pulse causes a control circuit to produce two additional signals. One signal causes MOSFET switches to hold a voltage for conversion and the other signal starts a variable rate clock which sequences the successive approximation analog to digital converter. The data bits leave the converter in serial form with the most significant bit (MSB) first and are applied to the A3 Timing Board.

## 8-98. Interface and Timing A3 (C).

8-99. For further manipulation, the data sequence must be converted to another form. The data interface is composed of two shift registers with parallel input and output capabilities. The first shift register used the variable rate clock output to shift in the data from the analog to digital converter in serial MSB form. The data is then reverse parallel loaded into another shift register which then clocks the data out at a constant rate in serial LSB form. The sequencing for the sample hold and conversion and the data interface is controlled by the timing portion of the A3 board.

8-100. A 45.875 MHz XTAL oscillator is divided down to provide timing clocks for various other circuits, some of which are located on other boards. This coordination of operations includes the following circuits:
a. Sample Hold and A/D Converter A1 (B)
b. Data Interface A3 (C)
c. Digital Filter A5 (D)
d. Digital Local Oscillator A4 (E)
e. Pseudo Random Noise A4 (P)
f. CAL Source A3 (C)
g. HP-IB A2 (0)
h. Effective Trigger Rate and Phase A3 (C)
i. Impulse Source A3 (C)

8-101. The sample hold and conversion takes place at a constant rate (approximately 100 kHz ) while the trigger signal is determined by the input waveform. To obtain the proper phase components of the transformed signal, the processor needs to know the relationship between the trigger signal, effective sample rate, and the sample hold signal. These relationships are determined by the effective sample rate circuit which employs a programmable divide by N counter and a counter with an I/O buffer on the output. The divide by N counter also drives the Pseudo Random Noise clock p/o A4 (P).

8-102. The Pseudo Random Noise and IMPULSE output are both proportional to the selected SPAN setting. The PRN clock divides the output from the divide by N counter by seven which initiates the PRN circuits and provides a signal for the impulse circuit that results in a TTL output equal to the SPAN/8192.

## 8-103. Digital Filter A5 (D).

8-104. The digital filter receives the serial (LSB first) data from the data interface (located on the A3 board). Essentially, the circuit performs a mathematical low pass filter function which has a bandwidth derived from the SPAN, BANDPASS, and INPUT MODE switch selection. This control data is input from the processor through an I/O buffer and into the digital filter control circuit. This circuit also signals a firmware direct memory access (DMA) operation which loads the filter output through an I/O buffer into the time record section of
random access memory (RAM). The circuit provides a timing signal to the effective trigger delay counter on the A3 Timing board. Overload conditions are sensed and a front panel annunciator is turned on if there is a possible overload in signal data. When SET START or SET CENTER is selected, the input serial data is multiplied by both the sine and cosine digital equivalents of the center frequency, of the segment of the spectrum under analysis, translating the signal to dc. These digital mixing signals are provided by the Digital Local Oscillator.

## 8-105. Digital Local Oscillator p/o A4 (E),

8-106. The digital local oscillator (L.O.) uses control information from the processor (derived from front panel controls) to establish a mixing frequency. Basically, if a 512 point time record is needed, 512 cosine and sine amplitude words are generated so that a point by point multiplication (mixing) operation in the digital filter can take place. In the L.O., 1024 cosine words are stored in ROM and are modified to obtain intermediate values. The starting phase and incremental value are the main requirements necessary to perform the word lookup routine.

8-107. The L.O. controller coordinates the timing of various L.O. circuits such as the binary incremental phase counter. The initial phase and frequency increment are loaded into the counter which has a feedback loop that adds the previous sum to the increment. Thus, a flow of incremented digital numbers are produced which form the address for the phase and cosine tables (ROMs). The outputs from the cosine and phase ROMs are combined using a slope intercept interpolation technique to produce a sine and cosine digital frequency amplitude word for each input sample.

## 8-108. Processor A7 (F).

8-109. The processor controls most of the major circuits in the instrument and performs the necessary calculations to implement the discrete analysis techniques. Data as well as control information is transferred over the I/O BUS and the IDA BUS. The I/O Bus is a bidirectional sixteen line bus which has access controlled by the processor. The IDA (instruction, address, and data) bus links the processor to the instruction ROM A6 (G) and the data processing RAM A8 $(\mathrm{H})$. It is comprised of sixteen lines, is bi-directional, and controlled by the processor.

8-110. The processor board contains the circuits which allow for bus buffering, bus access (I/O select), start up, reset, and a XTAL timing clock. Note that the start up and reset circuit has interconnections to other boards which may inhibit the processor from operating, should they malfuncation.

## 8-111. ROM A6 (G).

8-112. The processor receives its operating instructions from the ROM board. The board contains the integrated circuits which provide approximately 40 K of ROM. A control circuit, run by the processor, provides the sequencing of address and data output.

## 8-113. RAM A8 (H).

8-114. The processor uses the dynamic RAM to store control information and data variables. The digital display driver A9 accesses the RAM through a hardware DMA func-
tion which gives it priority over the processor. By accessing a specified area of the RAM at a constant rate, the display circuits perform a refresh function while obtaining display data. Data for the display section is transferred over a sixteen wire one way bus (XIDA).

## 8-115. Display Controller p/o A9 (I).

8-116. The display controller is an algorithmic state machine which sequences the activities of the display section. It receives a clock signal from the processor board and instructions via the I/O bus through an I/O buffer.

## 8-117. Digital Display Driver p/o A9 (J).

8-118. The digital display driver uses the control signals from the display controller to obtain data from the RAM and decode it into graphics and alphanumeric digital data. An address counter supplies the RAM address through the DMA circuit and returning data is latched into a buffer. The data is decoded into addresses for the character dot matrix generator and into X and Y amplitude graphics data. The X amplitude sweep data is actually the address count to the RAM. This data is multiplexed and applied to the analog display driver.

## 8-119. Analog Display Driver p/o A10 (K).

8-120. The analog display driver uses digital to analog converters to obtain the dc signals which eventually are amplified to drive the CRT. Character data is converted into X and Y position signals and $Z$ axis blanking to provide a $5 \times 7$ character dot matirx display. The display controller causes each character to be drawn on the CRT until all alphanumeric data is displayed.

8-121. X and Y graphic data is divided as follows. The X axis data is primarily used for character generation in the alpha mode. In the graphics mode however, the $X$ axis is set by the display controller to sweep at a constant rate which depends on the number of traces being displayed. A marker comparator circuit produces a signal when the sweep position voltage is the same as the front panel MARKER POSITION control voltage. The signal causes the RAM address to be latched into an I/O buffer for processor use.

8-122. The Y axis amplitude data is converted and applied to a line drawer which supplies a dc signal to drive the $Y$ axis CRT deflection amplifier. An associated circuit senses the magnitude of the Y axis change and applies a dc signal to control the intensity ( Z axis) of the CRT so that large displacements in amplitude will retain the same brightness as the X axis is swept at a constant rate. The dc signals which are developed by the analog display driver are next applied to the XYZ amplifiers.

## 8-123. XYZ Amplifiers p/o A13 (L).

8-124. The signals to the deflection amplifiers are less than $\pm 1$ volt. The amplifiers boost this voltage to less than $\pm 100$ volts to drive the CRT deflection plates. The Z axis amplifier uses a variable intensity control from the analog display driver in the graphics mode, and a TTL blanking pulse from the display controller for character dot generation in the alpha mode. An intensity input from the front panel controls the overall intensity level. The output from the amplifier is applied to the high voltage rectifier in the high voltage section of the instrument.

## 8-125. High Voltage Section p/o A13 and A65 (M).

8-126. The high voltage section contains circuits necessary to provide all of the high voltage CRT drives (except the $X$ and $Y$ deflection drives). Extreme caution should be used when servicing or adjusting controls and components mounted on circuit boards in this area due to high voltages (up to +18 KV ) which may remain present on circuit components EVEN WHEN THE INSTRUMENT IS OFF.
$8-127$. The high voltage rectifier supplies +18 KV to the post accelerator of the CRT. Inside a metal box located underneath the CRT are a transformer which supplies high voltage to a rectifier and voltage multiplier. The transformer receives its primary input from the high voltage oscillator and additional signals form the front panel FOCUS control and the Z axis amplifier. A cable which is connected to the rear of the CRT supplies filament, cathode, control grid, and focus voltages.

8-128. Other circuits located on the A13 board supply flood gun, accelerator, orthogonality, and X align voltages.

## 8-129. Supporting Boards and Circuits.

8-130. There are several areas of the instrument which do not interact directly with the signal flow. These areas are described as follows.

## 8-131. Instrument Control.

8-132. Two sections of the instrument affect the control functions by interacting with the processor through the I/O Bus. These are the front panel controls and the HP-IB.

### 8.133. Front Panel Controls A11 and A12 (N).

8-134. The front panel controls consist mainly of switches which have digital functions (operate at TTL levels). These switch outputs are latched into an I/O buffer where they are interrogated approximately ten times a second. Indicators are driven by the processor (except overload and data loading) which latches the data in an I/O buffer.

8-135. A subassembly mounted on the front panel switch board contains the logic to decode the FREQUENCY ADJUST rotary pulse generator and the processor reset control. Note that reset logic has an input from the front panel and from the HP-IB board.

## 8-136. HP-IB A2 (0).

8-137. The HP-IB board permits interfacing the HP-IB with the processor through the I/O bus. Mounted on the board is a nano-processor which, with the help of an instruction ROM, translates the HP-IB ASCII code to binary processor coding and handles HP-IB protocol. Also contained on the board are HP-IB isolation circuits, remote control and reset circuits, and an I/O buffer. Note that the processor is run by a clock which has, as its primary input, a signal from the A3 Timing board.

### 8.138. Instrument Outputs.

8-139. Instrument outputs (except IMPULSE) are located on portions of two boards which
carry primary signal data. In many respects, they operate as independent sections and are therefore shown on separate schematics.

## 8-140. Pseudo Random Noise p/o A4 (P).

8-141. Pseudo random noise is derived from a modified dc voltage which has been converted from the output of a pseudo random binary sequence generator. The binary sequence generator obtains an input clock from the A3 Timing board and programming from the L.O. portion of the A4 board. A front panel switch selects either PERIODIC or RANDOM noise. Periodic noise is a defined pseudo random binary sequence which is programmed and initiated so that its duration and timing coincides with the SPAN and resulting bandwidth. Random noise is simply extended pseudo random noise (up to 14 minutes) and does not coincide with other measurement activities. The binary output from the generator is converted by a digital to analog converter and applied to a four quadrant multiplier. So that phase and amplitude of the PRN output match the sample frequencies for the SPAN and PASSBAND selected, a cosine word is obtained from the Digital L.O. The cosine word is converted by a digital to analog converter and applied as the other input to the multiplier. The product of the two inputs is amplified and output to a BNC connector on the front panel.

## 8-142. X-Y Recorder p/o A10 (0).

8-143. The recorder outputs consist of a digital to analog converter for each of the two axis. The two converters (DACS) transform data directly off the I/O bus buffers. The rate of data transformation is controlled by the processor and approximates a constant slew rate for the X-Y recorder. A reference voltage source supplies the recorder DACS and the display DACS (A10) with a conversion reference voltage. The PEN LIFT relay drive is derived from a latched bit on the Xaxis I/O buffer.

## 8-144. Power Supplies A14 (R), A15 (S), A16 (T), A19-A17 (U), A18 (V).

8-145. All supply voltages, except those that are used for the floating input section, are derived from switching power supplies. The power supplies switch at a 27 kHz rate which is out of the measurement band of the instrument (the power supply clock can be detected in the band analysis modes when the center or start frequency is at 25 kHz ). The $+18,+12$, +7 power supply boards are interchangeable, their function depending on the position they occupy in the power supply mother board.

8-146. The control board (A17 and A19) schematic also contains the transformer, power supply clock, rectifiers, and other chassis mounted components. It must be in place and in working order for the other switching supplies to operate.

8-147. The linear power supply A18 can operate independantly and must be operating in order to supply power to the floating input section.
$\rightleftharpoons$ service group $\approx 2-$ TIMING $=$



Figure 8-4. 3582A Block Diagram. $\Longleftarrow$ SERVICE GROUP \#10-X Y RECORDER $\Longrightarrow$

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH ASSEMBLY OR SUBASSEMBLY DESIGNATION (S) OR BOTH FOR COMPLETE DESIGNATION.
2. COMPONENT VALUES ARE SHOWN AS FOLLOWS UNLESS OTHERWISE NOTED.

RESISTANCE IN OHMS
CAPACITANCE IN MICROFARADS
INDUCTANCE IN MILLIHENRYS
3.

DENOTES EARTH GROUND
USED FOR TERMINALS WITH NO LESS THAN A NO. 18 GAUGE WIRE CONNECTED BETWEEN TERMINAL AND EARTH GROUND TERMINAL OR AC POWER RECEPTACLE.
4. DENOTES FRAME GROUND
USED FOR TERMINALS WHICH ARE PERM. NENTLY CONNECTED WITHIN APPROXIMATELY 0.1 OHM OF EARTH GROUND.
5.
 DENOTES GROUND ON PRINTED CIRCUIT ASSEMBLY. (PERMANENTLY CONNECTED TO FRAME GROUND.

10.


DENOTES FRONT PANEL MARKING.
11. $\left[\begin{array}{l}\text { - }-7 \\ 1-\infty\end{array}\right.$

DENOTES REAR PANEL MARKING.
12.
$\Longrightarrow$ DENOTES SCREWDRIVER ADJUST.
13. * aVERAGE VALUE SHOWN, OPTIMUM VALUE SE. LECTED AT FACTORY. THE VALUE OF THESE COMPONENTS MAY VARY FROM ONE INSTR MEN TO ANOTHER. THE METHOD OF SELECTING THESE COMPONENTS IS DESCRIBED IN SECTION V OF THIS MANUAL
14. $\rightarrow$ DENOTES SECOND APPEARANCE OF A CON.
15. 924 DENOTES WIRE COLOR: COLOR CODE SAME AS RESISTOR COLOR CODE. FIRST NUMBER IDES. TIFIES BASE COLOR, SECOND NUMBER IDE. TIFIES WIDER STRIP, THIRD NUMBER IDENTIFIES NARROWER STRIP. (egg. $924=$ WHITE, RED, YELLOW.)
17. ALL RELAYS ARE SHOWN DEENERGIZED.

H


DENOTES BUFFER



DENOTES INVERTER


| A | $B \quad C \quad$ |
| :--- | :--- | :--- | :--- |

LL LL
LL L L
L HL L
LH HL
$H L L L$
HL HL
H HL L
H H H H


| $A$ | $B$ | $C$ | $Q$ |
| :--- | :--- | :--- | :--- |
| $L$ | $L$ | $L$ | $H$ |
| $L$ | $L$ | $H$ | $H$ |
| $L$ | $H$ | $L$ | $H$ |
| $L$ | $H$ | $H$ | $H$ |
| $H$ | $L$ | $L$ | $H$ |
| $H$ | $L$ | $H$ | $H$ |
| $H$ | $H$ | $L$ | $H$ |
| $H$ | $H$ | $H$ | $L$ |


| $A B C D$ |
| :--- | :--- | :--- | :--- |

LL HL
LH LL
LH HL
HL L L
HL HL
H HL L
H H HL


AB $Q$
LL L
LH H
H L H
H HL

## SERVICE GROUP 1 INPUT

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## INPUT

## SERVICE GROUP 1

## 8-1-1. INTRODUCTION.

8-1-2. The Input Service Group provides information pertaining to all the circuits contained on the A1 Input boards. The three major functions are input scaling, anti-aliasing filtering, and analog to digital conversion. Input scaling and the anti-aliasing filter are found on the $A$ (A1) schematic and the analog to digital converter on the B (A1) schematic.

## 8-1-3. GENERAL INFORMATION.

8-1-4. The input boards are interchangeable, their function depending on the mother board position they occupy. Therefore, even though both boards contain trigger circuitry, only the channel A position utilizes the trigger output. A malfunction on an input board can be quickly verified by exchanging the boards between the two channel positions. Programming data is derived from the I/O Bus via the E (A4) board. Note that the majority of the circuits on the board have floating power supplies and grounds. Be aware of instrument grounding connections when making measurements. Grounds can be made common by moving the ISOL/CHAS switch to the CHAS position.

## 8-1.5. ISOLATING THE PROBLEM.

8-1-6. The Troubleshooting Quick Reference Diagrams should be used to help isolate a problem. This assumes that one has switched input boards or in some other manner insured that the problem is on the Input (A1) Assembly. If only one of the input assemblies is bad, the other channel can be used as a troubleshooting tool. That is, any point in the signal path up to and including the S/H TP can be run through the other channel and should produce a good spectrum. Use this form of troubleshooting wherever possible.

8-1-7. Another valuable troubleshooting aid is circuit cooler spray. This is especially effective for the A/D converter comparator (U109) and DAC (U111). Many times a defective component can be made to work momentarily by spraying with the cooler spray. In this way, the spray can be used for troubleshooting.

## 8-1.8. TROUBLESHOOTING THE INPUT ATTENUATOR, AMPI.IFIER AND LP FILTERS.

## 8-1.9. No Spectrum.

8-1-10. If there is no spectrum on only one channel, this is the place to start troubleshooting. Check the level at the LPF TP. With a full-scale input, the level should be about 1.5 volts rms and should look like the input. If this is OK , the problem is with the $\mathrm{A} / \mathrm{D}$ section (Schematic B). If the signal is not good, refer to the Troubleshooting Block Diagram.

## 8-1-11. Attenuator.

8-1-12. If the problem is only on some ranges, use Tables $8-1-1$ and $8-1-2$ with input pro-
gramming and relay and stage gain information. If U11 isn't programming, check the optical isolators U15 and U16 with the front panel I/O Bus Test as follows:
a. Get into the Front Panel self-test by holding RESTART while pushing and releasing RESET.
b. Select average \#256, short A7J4 and push restart. (A754 must remain shorted)(Don't short this TP until the instrument is in the self-test mode or it will initiate the primitive ROM test). This allows the instrument to go into the I/O Bus test.
c. Push RESTART until test \#10 is displayed (it's the one after 7). This gives a signal at D IN and CLK IN so that the outputs of U15 and 16 are changing. Check for high and low levels (the failure mode is that the output is stuck high). When the test is completed, unshort J4.

## 8-1-13. CAL Signal.

8-1-14. If the CAL signal isn't displayed on one channel, check the other channel. If this is OK, run the input to U14 (pin 3) into the other channel ( 3 V range). If this is OK, it's probably the isolator (U14). If the signal at U14(3) isn't good, check A3U42. If there's no CAL signal on either board and the attenuators are programming correctly, troubleshoot the CAL circuits on the A3 board. (Schematic C)

## 8-1.15. Distortion.

8-1-16. If the spectrum is excessively distorted on one channel, run the signal from the LPF TP into the input of the other channel. If this looks OK, go to the A/D section (Schematic B). If it can be determined that the distortion is not caused by the A1 board, use the front panel digital filter, ROM and RAM tests to check these components. Distortion can also be caused by the timing and local oscillator boards.


Figure 8-1-1. Schematic A Block Diagram.

## 8-1-17. Noise.

8-1-18. Excessive noise is usually caused by the A/D section. Figure 8-1-2 shows a CAL signal display with excessive noise. Note that the noise floor has risen. This particular problem was due to the comparator (U109). Again, circuit cooler spray is helpful for isolating this problem.


Normal CAL Signal


CAL Signal With Excessive Noise

Figure 8-1-2. CAL Signal Indications.


Tabla 8-1-1. Input Programming.

| Full Scala dBV | Line: <br> U11 Pin: | A 3 | B 4 | c | 0 6 | E | F 11 | 6 12 | $H$ 13 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Cal |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| + 30 |  | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |
| +20 |  | 0 | 0 | 1 | 0 | 0 | 0 | 1 |  |
| +10 |  | 0 | 0 | 0 | 0 | 1 | 0 | 0 | U |
| 0 |  | 0 | 0 | 1 | 0 | 1 | 0 | 0 | - |
| - 10 |  | 0 | 0 | 0 | 0 | 0 | 1 | 0 | - |
| -20 |  | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 8 |
| -30 |  | 1 | 0 | 1 | 0 | 0 | 1 | 0 |  |
| -40 |  | 1 | 0 | 0 | 1 | 0 | 1 | 0 |  |
| -50 |  | 0 | 1 | 0 | 1 | 0 | 1 | 0 |  |

Table 8-1-2. Input Board Attenuator Relay And Amplifier Gain.

| Sensitivity |  | K2 | K3 | K4 | K5 |  | 1st Stage Gain | $\begin{gathered} \text { 1st } \\ \text { Stage } \\ \text { Gain } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Cal |  |  |  |  |  | X | 2.364 | 2.364 |
| $30 \vee(+30)$ | $x$ |  |  | X |  |  | 2.364 | 2.364 |
| $10 \vee(+20)$ | $x$ |  |  | X |  |  | 7.476 | 2.364 |
| $3 \vee(+10)$ |  | $x$ |  |  | x |  | 2.364 | 2.364 |
| 1 V 01 |  | X |  |  | X |  | 7.476 | 2.364 |
| $\begin{aligned} & 300 \mathrm{mV} \\ & (-10) \end{aligned}$ |  |  | X |  |  |  | 2.364 | 2.364 |
| $\begin{aligned} & 100 \mathrm{mV} \\ & (-20) \end{aligned}$ |  |  | x |  |  |  | 7.476 | 2.364 |
| $30 \mathrm{mV}(-30)$ |  |  | X |  |  |  | 7.476 | 7.476 |
| $10 \mathrm{mV}(-40)$ |  |  | X |  |  |  | 23.64 | 7.476 |
| $3 \mathrm{mV}(-50)$ |  |  | X |  |  |  | 23.64 | 23.64 |

IMPUT PROGRAMNING. Input programming comes thru optical isolators U15 and U16. To check the isolators:

1. Select the front panel self-test mode by pressing RESET while holding down RESTART. When RESTART is released, F.P. self-test 0 will come up.
2. Short A7 J4 and select AVE NUMBER 256.
3. Press RESTART until test 000010 comes up.
4. There should be $0-5 \mathrm{~V}$ signals on pin 6 of both U15 and U16.

Programming can be checked using Table 8-1-1. When done with this test, unshort A7 J4.



Figure 8-1-3. Troubleshooting Quick Reference For Schematic A

| Attenuator | 30 dev | 20 dBV | 10 dBV | O dBV | - 10 dBV | $-20 \mathrm{dBv}$ | $-30 \mathrm{dBV}$ | $-40 \mathrm{dBV}$ | $-50 \mathrm{dBV}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 16 dBV | 16 dBv | 9 dBV | - 1 dBV | -11 dBV | -21 dBV | -31 dBV | -41 dBV | - 51 dBV |
| Input Leval | 63 VRMS | 6.3 VRMS | 2.8 vRMS | 0.89 VRMS | 279mVPMS | 89 mVRMS | 28 mVRMS | 9.0 mVRMS | 3 mVRMS |
| Top of R9 | 60 mV | 80 mV | 266 mV | 84 mv | 279 mV | 89 mV | 28 mV | 9.0 mV | 3 mV |
| Top of R12 | 62 mV | 62 mV | 281 mV | 89 mV | 279 mV | 89 mV | 28 mV | 9.0 mV | 3 mV |
| TP 7 | 149 mV | 468 mV | 665 mV | 662 mv | 663 mV | 668 mV | 209 mV | 211 mV | 67 mV |
| 44 (6) | 351 mv | 1.108 V | 1.576 V | 1.568 V | 1.569 mV | 1.582 V | 1.564 V | 1.574 V | 1.574 V |
| 47 (6) | 351 mV | 1.108 V | 1.576 V | 1.568 V | 1.569 mV | 1.582 V | 1.564 V | 1.574 V | 1.574 V |
| U8 161 | 351 mV | 1.10 BV | 1.576 V | 1.56 BV | 1.569 mV | 1.582 V | 1.564 V | 1.574 V | 1.574 V |
| U9 (6) | 352 mV | 1.109 V | 1.578 V | 1.569 V | 1.570 mV | 1.585 V | 1.565 V | 1.577 V | 1.577 V |
| LPF TP | 351 mv | 1.10 BV | 1.576 V | 1.568 V | 1.569 V | 1.582 V | 1.564 V | 1.574 V | 1.574 V |


| Full Scalo dBy | $\left\|\begin{array}{r} \text { Line: } \\ \text { U1I Pin: } \end{array}\right\|$ | 1 | B | c | 0 |  | E | F | 6 | H 13 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Cal |  | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | - |
| + 30 |  | 0 | 0 | 0 | 0 |  | 0 | 0 | 1 | ॥ |
| +20 |  | 0 | 0 | 1 | 0 |  | 0 | 0 | 1 | u |
| +10 |  | 0 | 0 | 0 | 0 |  | 1 | 0 | 0 | - |
| 0 |  | 0 | 0 | 1 | 0 |  | 1 | 0 | 0 | ${ }^{\prime \prime}$ |
| -10 |  | 0 | 0 | 0 | 0 |  | 0 | 1 | 0 | ¢ |
| -20 |  | 0 | 0 | 1 | 0 |  | 0 | 1 | 0 |  |
| -30 |  | 1 | 0 | 1 | 0 |  | 0 | 1 | 0 |  |
| -40 |  | 1 | 0 | 0 | 1 |  | 0 | 1 | 0 |  |
| -50 |  | 0 | 1 | 0 | 1 |  | 0 | 1 | 0 |  |


| Sensitivity | KI | $K 2$ | K3 |  | K5 | K | 1st Stage Gain | $\begin{aligned} & \text { 1st } \\ & \text { Stage } \\ & \text { Gain } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Cal |  |  |  |  |  | x | 2.364 | 2.364 |
| $30 \vee(+30)$ | x |  |  | X |  |  | 2.364 | 2.364 |
| $10 \vee(+20)$ | X |  |  | X |  |  | 7.476 | 2.364 |
| $3 \vee(+10)$ |  | X |  |  | X |  | 2.364 | 2.364 |
| $1 \mathrm{~V}(0)$ |  | X |  |  | X |  | 7.476 | 2.364 |
| $\begin{aligned} & 300 \mathrm{mv} \\ & 1-10) \end{aligned}$ |  |  | X |  |  |  | 2.364 | 2.364 |
| $\begin{aligned} & 100 \mathrm{mV} \\ & (-20) \end{aligned}$ |  |  | $x$ |  |  |  | 7.476 | 2.364 |
| $30 \mathrm{mV}(-30)$ |  |  | X |  |  |  | 7.476 | 7.476 |
| $10 \mathrm{mV}(-40)$ |  |  | X |  |  |  | 23.64 | 7.476 |
| $3 \mathrm{mV}(-50)$ |  |  | X |  |  |  | 23.64 | 23.64 |




## 8-1-19. TROUBLESHOOTING THE A-D CONVERTER.

8-1-20. A common failure with this circuit is excessive distortion. This type of problem can easily be isolated to the Al board by swapping input boards. Remember that a board must be in the inner slot (Channel A) for triggering.

## 8-1-21. Checking Power Supplies and H/C TP.

8-1-22. Refer to Figure 8-1-5 for the $\mathrm{H} / \mathrm{C}$ signal. This must be working for the $\mathrm{S} / \mathrm{H}$ to work and is used for triggering in further tests.


Figure 8-1-5. H/C TP.

## 8-1-23. Checking the S/H.

8-1-24. Check at the S/H TP and refer to Figure 8-1-6.

## WARNING

Do not accidentally short S/H TP to ground. This will destroy U104; same with U102 and its output.

CH A TRIG; HOLD OFF MAX
CH A: LPF TP; 0.1 VIDIV CH B: S/H TP' 0.2 V/DIV (BOTH ABOVE X 10 PROBE) ALTERNATE SWEEP; 50 USEC/DIV 3582: 0-25 kHZ SPAN; 300 mV RANGE INPUT: 10 kHz AT 105 mV OR -3.4 dBm , 50 OHMS.


Figure 8-1.6. 10 kHz Input At LPF and S/H TP's.

Adjustment of the trigger level and holdoff will be necessary to get exactly this picture, but this will indicate whether the $\mathrm{S} / \mathrm{H}$ is working. To check for distortion, connect the S/H TP to the other channel's input. If distortion is evident here and not at the LPF TP, the problem is more than likely in the S/H. Note that the S/H output must "look" sampled. If it looks just like the input, the op-amp or current amp (U103 or U104) is open or the sample FET, Q108 is shorted.

## 8-1-25. Troubleshooting The S/H.

8-1-26. The most common causes for problems are the FET's, Q108 and Q110 and the current amps U104 and U102. These amps are very easy to damage, so check that U103 and U101 are OK before replacing them.

## NOTE

FETS and amps in the S/H and buffer may have to be replaced more than once to eliminate distortion. The FETS have a guarding ring around the leads; leave this on during soldering and then remove it.

8-1-27. Intelligent shotgunning is the most efficient way to troubleshoot these circuits. Figure 8-1-7 below shows the S/H output with the LPF TP shorted to ground, along with the register clock.


Figure 8-1.7. S/H TP and A/D Clock With LPF TP Shorted To Ground.
8-1-28. Use a X1 probe with short ground lead to get the S/H signal to look like this. The important things is that the S/H level at the 2nd and 13th clock pulse be within 2 mV and these should be within 2 mV of the level between clock cycles. If these levels are off, suspect the FETS. Note that the S/H TP signal peak amplitude can vary from the value shown on a good unit. If the signal doesn't go all the way to zero, Q108 is probably leaky. If it goes too far below zero, suspect Q110.

## 8-1-29. Troubleshooting The A/D.

8-1-30. It's difficult to look at specific data signals in this circuit. If the problem is on the input board and the $\mathrm{S} / \mathrm{H}$ output appears correct through the other channel, it must be the A/D.

8-1-31. The first thing to check is the register clock (CLK TP), see Figure 8-1-8. The clock
rate is slower for the first 3 periods to allow more settling time for the most significant bits. If the clock runs at a constant rate, check U108C and associated circuits.


EXT TRIG. ON H/C; - SLOPE
1 USEC/DIV
0.1 V/DIV; X10 PROBE; DC CPL.

OVDC 2 CM FROM BOTTOM

Figure 8-1-8. Register Clock.

EXT TRIGGER ON H/C; - SLOPE
0.01 V/DIV; X10 PROBE; OVDC AT CENTER graticule.
1 USEC/DIV SWEEP

MOTE
SIGNAL CAN GO NEGATIVE OR POSITIVE. THE
IMPORTANT THING IS THAT IT BE ZERO AT THE START AND END OF THE SWEEP.


Figure 8-1-9. Output Of DAC With LPF TP Shorted To Ground.

8-1-32. As an overall check of the A/D, look at the DAC output (top of R122) with the LPF TP shorted to ground. This should look like Figure 8-1-9. Depending on the DC offset, this can swing either way at first; the important thing is that it starts and ends at zero.

8-1-33. If it doesn't return to zero, suspect the comparator (see next section) or SAR. If it is inconsistant, suspect the successive approximation register (SAR), U111. This register controls the logic for the A/D. If there is distortion traceable to the A/D, but Figure 8-1-6 looks OK, it's probably the DAC.

## 8-1-34. Troubleshooting The Comparator.

8-1-35. The inputs to U109 (pins 2 and 3 ) should "converge". If they do and the DAC output is not getting to zero, the problem is with the balance of the differential preamp. If the inputs aren't converging, suspect U109. Circuit cooler spray is helpful in troubleshooting this circuit.

## 8-1-36. The Light Isolators.

8-1-37. The light isolators, U105-107, can cause problems, but are easy enough to troubleshoot. The outputs should be TTL levels with failure mode a "stuck high" condition.


Figure 8-1-10. Analog To Digital Converter Block Diagram.



INTRODUCTION. This section of the A1 assembly consists of a buffer amplifier, sample and hold circuit, and analog to digital converter (A/D). A simple way to localize the problem is to pick off signals at various locations and feed them through the other channel. A signal from any point in the signal path up to and including the S/H TP can be fed into a spectrum analyzer (such as the other channel) and display a good spectrum.

The output current amplifiers of the Buffer Amplifier and the Sample and Hold are easily damaged by accidently shorting them to ground. Please use caution.

The signal at the S/H TP must "look" sampled. A defective S/H will put a signal on the S/H TP that looks very much like that at the LPF TP.

This is a difficult circuit to troubleshoot for noise and distortion problems that are not too serious. That is, operational amplifiers and other active components may appear to be good and still cause problems. It is appropriate when a problem is localized to replace tested-good circuit components when no other problem can be found.

Note that the $A / D$ Clock has uneven periods. This is to allow more settling time for the MSB's of the A/D.

A/D CONVERTER. The A/D converter is of the successive approximation type, using an IC DAC. The Successive Approximation Register (SAR) controis the logic for the A/D.

The SAR begins a cycle by setting the MSB input to the DAC. The output of the DAC is a current proportional to the difference between the input (S/H TP) and the analog equivalent of the MSB. This signal goes to the comparator and the comparator output tells the SAR whether the MSB should be set (if the input is higher than the MSB) or not set. This process is continued for the remaining 11 bits in a "successive approximation" that is quite accurate.





Table 8-1-4. Replaceable Parts.


Table 8-1-4. Replaceable Parts (Cont'd).

| Reference Designation | HP Part Number | C | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| C132 | 0160-3622 | 8 |  | CAPACITOR-FXD , IUF +80-20X 100 VDC CER | 28400 | 0160-3622 |
| C133 | 0160-3622 | 8 |  | CAPACITOR-FXD IUF $1480-20 \mathrm{X}$ 100VDC CER | 28480 | 0160-3622 |
| C134 | 0160-2264 | 2 |  | CAPACITOR-FXD 20PF +05K 500VDC CER 0+030 | 28480 | 0160-2264 |
| C135 | 0160-3286 | 0 | 1 | CAPACITOR-FXD 190PF $\$-18$ 300VDC MICA | 28480 | 0160-3286 |
| C136 | 0160-3622 | 8 |  | EAPACITOR-FXD . IUF +80-20X LOOVDC CER | 28480 | 0160-3622 |
| ${ }^{\text {C }} 131$ | 0160-2201 | 7 |  | CAPACIPDROFXO 51PF +-5\% 300VDC MICA | 28480 | 0160-2201 |
| C138 | 0160-3622 | 8 |  | CAPACITOR-FXO IUF +80-20X LOOVDE CER | 28480 | 0160-3622 |
| C139 | 0160-4389 | 6 | 2 | CAPACIPOR-FXO l00PF \$-5PF 200VDE CER | 28480 | 0960-4389 |
| C140 | C160-4389 | 6 |  | CAPACITOR-FXD 100PF $+05 P F$ 200VDC CER | 28480 | 0160-0389 |
| 6141 | 0121-0474 | 0 | 1 | CAPACITDR-V PRMR-PSTN , 3-1.5PF G00V | 28480 | 0121-0474 |
| ${ }_{6} 142$ | 018000116 | , |  | CAPACITOR - PXD 6. SUF+-10X 35VOC TA | 56289 | $1500685 \times 903582$ |
| ${ }_{6} 143$ | 0160-3622 | 8 |  |  | 28480 28480 | 0160-3622 |
| C144 $C 145$ | $0160-0945$ $0121-0046$ | 2 | 1 |  | 28480 52763 | 016000945 $3043229 / 39 P \mathrm{Pr}$ $\mathbf{N 6 S O}$ |
| C147 | 0160-3622 | , | 1 | CAPACIPOR-FXD. 1 UF +80-20X 100 VDE CER | 28480 | 0160-3622 |
| $C 148$ $C 149$ | $\begin{aligned} & 0160=2055 \\ & 0160=0576 \end{aligned}$ | $\stackrel{0}{5}$ |  | CAPACIPOR-FXD .01UF $+80-20 X 100 \mathrm{VDC} \mathrm{CER}$ CAPACITOR | 28480 28980 | $\begin{aligned} & 0160-2055 \\ & 0160=0576 \end{aligned}$ |
| C150 | 0160-0516 | 5 |  | CAPACITOREFXD :IUF +-20X 5OVDC CER | 28480 | 0160-0576 |
| CR1 | 1902-0117 | 3 | 3 | DIODE-ZNR INE25 6.2V 5X Do.1 PDE.4W | 04713 | 1N825 |
| CR2 | 1901-0518 | 8 | 4 | DIODE-SCHOTTKY | 28480 | 1901-0516 |
| CR 7 | 1901-0040 | 1 |  | DIODE-SWITCHING 30V SOMA 2NS 00.35 | 28480 | 1901-0040 |
| CR8 | 1901-0356 | 6 | 2 | DIDDE-GEN PRP 35V 50ma 00035 | 28480 | 1901-0376 |
| CRG | 1901-0376 | 6 |  | DIDDE-GEN PRP 35V SOMA O0-35 | 28480 | 1901-0376 |
| CR10 | 1901-0040 | 1 |  | DIODE SWITCHING 30V SOMA 2NS DO-35 | 28480 | 1901-0040 |
| CR11 | $1902-0049$ $1902-0049$ | 2 |  |  | 28480 28480 | 1902-0099 |
| CR101 | 1901-0518 | 8 |  | DIODE-8CHOTTKY | 28480 | 1901-0518 |
| Crioz | 1901-0518 | 8 |  | diode-sehotiky | 28480 | 1901-0518 |
| CR105 CR106 | 1902-0526 | 9 | $\frac{1}{2}$ | DIODE-CUR RGLTR 1 N5305 100V DO-7 DIODE-2NR 8.25 V 5 | 04713 28480 | 2N5305 190205130 |
| CR10) | 1902-3139 | 7 |  | DIODE=2NR 8.25V 5x DO-7 PDE. 4 w PCE4.053x | 28460 28480 | 1902-3130 |
| $\mathrm{J}_{1}$ | 1250-1512 | 5 | 1 | CDNNECTOR-RF SM-SNP M PC 75-0MM | 98291 | 51-153-0000 |
| $k$ $k$ $k$ | $0490-1168$ $0490-1168$ | 2 | 7 | RELAY-REED iA 500 MA 200VDE SVOC-COIL RELAY-REED IA 500 MA 200VDC SVOC-EOIL | 28480 28480 | $0400-1168$ $0900-1168$ |
| $k 3$ | 0490-1168 | 2 |  | RELAY-REED 14500 ma 200VDE $5 \mathrm{VDC}=$ COIL | 28480 | 0490-1168 |
| K4 | 0490-1168 | 2 |  | RELAY-REED 1A SOOMA 200VDE SVOC-COIL | 28480 | 0490-1168 |
| k 5 | 0490-1168 | 2 |  | RELAY-REED IA 500 MA 200VDC $5 \mathrm{VOC-COIL}$ | 28480 | 0490-1168 |
| $\mathrm{K}_{6}$ | 0400-1108 | 2 |  | RELAY-REED 1A 500ma zoovot 5VDE-COIL | 28480 | 0490-1168 |
| $k 7$ | 0490-1168 | 2 |  | RELAY-REED 1A SOOMA ZOOVDE 5VOC-COIL | 28480 | 0090-1168 |
| L101 | 9100-2556 | 8 |  | COIL-MLD 33UM 10x 0 =45 .1500x, 375LG-NOM | 28480 | 9100-2356 |
| 6102 | 9100-2596 | 8 |  | COIL-MLD 33UN 10X 0=45 .1560X, 375LGENOM | 28480 | 9100-2356 |
| 6103 | 9100-2556 | 8 |  | COIL-MLD 33UN 10X QEa5 .1560X,375LG-NOM | 28480 | 9100-2550 |
| 0101 0101 | $1855-0308$ 1854.0215 | 5 | 2 | TRANSISTOR-JFET OUAL N-CMAN D-MODE SI TRANSISTOR NPN 81 PDESSOMW FTE3OOMHZ | 28480 04713 | $\begin{aligned} & 1855-0308 \\ & \text { SP8 } 3611 \end{aligned}$ |
| 0102 | 1853-0089 | 5 |  | TRANSISTOR PNP 2N4911 S1 PDa 200 Mm | 07263 | 2N4917 |
| 0103 | 1854-0221 | 9 | 1 | TRANSISTOR-DUAL NPN PDE 550 MW | 28480 | 1854-0221 |
| 8104 | 1853-0089 | 5 |  | TRANSISTOR PNP 2N4917 SI PDE200mm | 07263 | 2N4917 |
| 0105 0100 | $1853-0089$ $1853-0016$ | 5 | 3 | TRANEISTOR PNP $2 N 4917$ 81 PDE200MW TRANSISTOR PNP 81 PO-92 PDE300MW | 07263 28480 | $2 N 4919$ 105300016 |
| 0107 | $1853-0016$ | 8 |  | TRANEISTOR PNP SI PO-92 PDEJ00 Mm | 28480 | 1853-0016 |
| 0108 | 1855-0269 | 9 | 2 | TRANSISTOR MOAFET N-CHAN E-MDDE SI | 18324 | 80214 |
| 0100 | 1853-0089 | 5 |  | TRANSIBPOR PNP 2N4917 SI PDE200MW | 07263 | 2N4917 |
| 0110 | 1855-0269 | 7 |  | TRANSISTOR MOAFET N-CHAN EGMODE SI | 18324 | 80214 |
| R1 | 0698-5132 | 8 | 1 | RESISTOR 900K .5x , 25w F TC=040100 | 28480 | 0698-5132 |
| R2 | 06988.5131 | 7 | 1 | RESISTOR POOK . $5 x$, 25w F TCE04-100 | 19701 28480 | MF52c1/4-7009003=0 |
| R3 | 0757-0013 | 0 | 1 | REBISTOR 111k.5x. 5 w W PCE0+050 | 28480 19901 | $075700013$ |
| Ra RS | $0698-8324$ 0698.4195 | 1 | 1 |  | 19701 24596 | MF52C1/4-72-1012-0 $C 4-1 / 8-90-10210 F$ |
| R6 | 0698-4423 | 8 | 1 | RESISTOR 1.37K ix . 125 W F TC=04-100 | 24546 | c4-1/8-10-1371-F |
| R 7 | 0698.4441 | 0 | 1 |  | 24546 | C4-1/8-10-3741*F |
| R8 | $2100-3052$ 0698.7332 | 4 | 1 |  | 02111 28480 | $43 P 500$ $0698-7332$ |
| R10 | 0698-3279 | 0 |  | RESISTOR 4,99K ix. 125 WF FCEO+0100 | 24546 | C4-1/8-70-4991 -5 |
| R11 R12 | $0898-9486$ 0698.4470 | 3 | 2 |  | 24546 24546 | $C 4-1 / 8-10-2492-F$ $C 4-1 / 8-90-691-F$ |
| R13 | 0698.4470 | 5 |  | RESISTOR 6,98k $1 \times$. 125 W F TCOO+=100 | 24546 | C4-1/8-10-6981-F |
| R14 | 0698-3279 | 0 |  | RESISTOR 4.99K 1\% . 125 W F YCaO $+=100$ | 24546 | $\mathrm{C} 4=1 / 8 \mathrm{~F}$ - 0 - 49910 F |
| R15 | 0698.4424 | 9 | 1 | RESISTOR 1.4K 1\%.125w F TCoteriot | 24546 | C4-1/8-90-1401-F |
| R19 R17 | $0683-1115$ $0683-1515$ | 8 | 1 | RESISTOR 110 RESISTOR 150 SX | 01121 | $\begin{aligned} & C B 1115 \\ & C B 1515 \end{aligned}$ |
| R1s | 0699-0190 | 0 | 2 |  | 28480 | 0699-0190 |
| R19 | 0699-0193 | 3 | 2 | RESISPOR 6, 48K, 25x . $125 \mathrm{WFF} \mathrm{TC}=04050$ | 28480 | 069900193 |
| R20 | 0699-0447 | 0 | 2 | RESISTOR 2.264K.25\%.125W F TC $=0+50$ | 28480 | 0699-0447 |

See introduction to this section for ordering information
*Indicates factory selected value

Table 8-1-4. Replaceable Parts (Cont'd).

| Reference Designation | HP Part <br> Number | C | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| R21 | 0698-3358 | 6 | 6 | RESISTOR 1K .5\% . 125 W W TC=040100 | 03888 | PME55-1/8-F0-1001-D |
| R23 | 0698-3202 | 9 | 1 | RESISTOR 1.74K $1 x$, 125 W F TCOO $+=100$ | 24546 | c4-1/8-10-1741-F |
| R24 | 0699-0190 | 0 |  | RESISTOR 1.364K , 25x , 125w F TC=00-50 | 28480 | 0699.0190 |
| R25 | 06999-0193 | 3 |  |  | 28480 28480 | $0699-0193$ |
| R26 | 0689-0194 | 4 |  |  | 28480 | $0699.0194$ |
| R27 | 0698-2258 | 3 | 1 |  | 28480 | 0698-2258 |
| ${ }^{R} 28$ | 06988-4464 | 7 | 1 |  | 24546 | Ca-1/8-T0-887Rof |
| $\mathrm{R}_{29}$ | 0757-0290 | 5 |  |  | 19701 | MFAC1/8-10-61910F |
| R330 R 31 | 0698-4014 | 3 3 | 2 | RESISTOR 787 iz. 125 W F TC=040100 RESISTOR 787 \% | 24546 24546 | $C 4-1 / 8-10-787 R-F$ $C 4-1 / 8-10-787 R-F$ |
| R31 | 0698.4014 | 3 |  | RESISTOR 787 1\%.125w F TCE040100 | 24546 | C4-1/8-10-787R.F |
| $\mathrm{R}_{32}$ | 0698-3515 | 7 | 1 | RESISTOR 5.9K $1 \times .125 \mathrm{WF}$ TCEO* 0100 | 24546 | C4-1/8-90-59010 ${ }^{\text {c }}$ |
| R33 | 0698-4468 | 1 |  |  | 24546 | c4-1/8-10-1131-F |
| R334 | 0698-4468 | 1 |  |  | 24546 | C401/8-10-1131-F |
| R36 | $0098=4465$ | - | 1 | RESISTOR 931 1 x , 125W F TCE040100 | 24546 | C401/8-T0-931R-F |
| $\mathrm{R}_{37}{ }^{2}$ | 0757-0421 | 4 | 1 |  | 03292 | C4-1/8-T0-825R-F |
| R38 | 0757-0446 | 3 | 1 | RESISTOR 15K $1 \%$, 125 W F $\mathrm{CC}=040100$ | 24546 | $C 4-1 / 8=10-1502-F$ |
| R30 | 0698-3519 | 1 |  |  | 24546 | C4-1/8-10-1242-F |
| R40 R4, | $0698=4435$ $0683-3945$ | 2 | 2 |  | 24546 01121 | $\begin{aligned} & \operatorname{c4-1/8-T0-2491-F} \\ & \operatorname{cs3045} \end{aligned}$ |
| R42 | 0683-2055 | 7 | 1 | RESISTOR 2M 5\% , 25 mFC FCE-900/ 11100 | 01121 | C82055 |
| 8.3 | 0683-1525 | 4 |  | RESISTOR 1.5K 5x . 25 WFFC TCE $=400 / 4700$ | 01121 |  |
| R44 | 0698-4470 | 5 |  | RESISTOR 6.98 K (18, 125 W F TC $=0+-100$ | 01121 | C4-1/8-TO-6981-F |
| 845 | 2100-3350 | 5 | 1 | AEStSTOR-TRMR 200 10\% C StOE=ADJ I-TRN | 28480 03292 | $2100-3350$ $\mathrm{C} 4-1 / 8-\mathrm{TO}-6981-\mathrm{F}$ |
| Ras | 0698-4470 | 5 |  | RESISTOR 6.98K.18.125W F TC=0+-100 | 03292 | C4-1/8-T0-6981-F |
| R47 | 0698-3447 | 4 | 2 | RESISTOR 422 1\% . 125 W F TCO04-100 | 24546 | Ca-1/8-T0-422R-F |
| R48 | 0008-3358 | 6 |  | RESISTOR 1K, 5\%, 125W F TCE04=100 | 03888 28480 | PME55-1/8-T0-1001-D 0698-5438 |
| R49 | 0698-5438 | 7 |  | RESISTOR 100.25\%.125W F TC=0+-50 | 28480 | $0698-5438$ |
| R50 R5i | $0008-3358$ 0698.3358 | 6 |  | RESISTOR RESISTOR K K | $\begin{aligned} & 03888 \\ & 03888 \end{aligned}$ | $\begin{aligned} & \text { PME55-1/8-T0-1001=D } \\ & \text { PME55-1/8-T0-1001=D } \end{aligned}$ |
| R51 | 0698-3358 | 6 |  | RESISTOR IK .5\% . 125 W F TCE04-100 | 03888 | PME55-1/8-T0-1001=D |
| R52 | 0083-3045 | 6 |  | QESISTOR 390k 5x , 25W FC TCE-S00/4900 | 01121 | C83945 |
| $R 53$ | 0683-2415 | 3 |  | RESISTTR 240 5X, 25W FC TCE-400/4600 | 01121 | $082415$ |
| R54 | 0757-1094 | 9 | 1 |  | 24546 | Ca-1/8-T0-1471-F |
| R101 | 21000-3095 | 5 | 1 | RESISTOR-TRMR 200 10x C SIDE-AOS $17-$ TRN | 02111 24546 | a3P201 c 4018 -10-1911-F |
| R102 | 0698-4430 | 7 |  | RESISTOR 1.91K 1\% . 125 F F TE04-100 | 24546 | C4-1/8-10-1911-F |
| R104 | 0757-0283 | ${ }^{6}$ |  | AESISTOR 2 K 1\%, 125w F TC=04.100 | 24546 | Ca-1/S-10-2001-F |
| R100 | 0757-0161 | 9 |  | RESISTOR 604 $1 \times, 125 \mathrm{~W}$ P TC=04-100 | 24546 | C4-1/8-10-604R-F |
| R107 | 0757-0280 | 3 |  | RESISTOR IK 1\%, 125 W F TC=0t-100 | 24546 | Ca-1/8-10-1001-F |
| R109 R100 | 0757-0161 $0757-0410$ | 9 | 1 |  | 24546 24546 | $C 4-1 / 8-10-604 R-F$ $C a-1 / 8-T 0=301 R-F$ |
| R110 | 0083-1005 | 5 |  | RESISTOR $105 \%$, 25 W FC TCE $=400 / 4500$ | 01121 | c81005 |
| R111 | 0683-1525 | 4 |  |  | 01121 | CB1525 |
| R112 | 0757-0283 | 5 |  | RESISTOR 2K 1x.125w F TC=0 $=100$ | 24546 | Ca-1/8-10-2001-F |
| R113 | 0083-1005 | 5 |  | RESISTOR 10 5\% , 25WFC TC=A400/4500 | 01121 24546 | CB1005 |
| R114 | 0759-0283 | 6 |  | RESISTOR 2K 1\% .125W F TCeot-100 | 24546 | Ca-1/8-10-2001-F |
| R1: R116 | 0683-3025 | 3 | 2 | RESISTOR 3K 5x, 25 W FC TCa-400/4700 | 01121 | C83025 $C 83615$ |
| R1: R1: R | $008.3-3615$ $0683-3615$ | 7 |  |  | 01121 | $C 83615$ c83615 |
| R1:17 R11 | 00833-3615 | 4 |  | RESISTOR 360 RESISTOR 3 S | 01121 | c83615 C83315 |
| Rilo | 0683-3615 | 7 |  | RESISTOR 300 5\% , 25W FC TC=0400/4600 | 01121 | CB3615 |
| R120 R121 R12 | $\begin{aligned} & 0683-4315 \\ & 0683-4315 \end{aligned}$ | ${ }_{6}^{6}$ | 1 | RESISTOR 430 RESISTOR 430 R | 01607 01121 | $\begin{array}{r} \text { CB4315 } \\ \text { ce4315 } \end{array}$ |
| R122 | 0098-3557 | 7 | 1 | RESISTOR 806 $1 \% .125 \mathrm{WF}$ TC=04-100 | 24546 | Ca-1/8-10-806R-F |
| R123 | 0698-3497 | 4 |  | RESISTOR 6.04K I\% . 125 W F TCEO4-100 | 24546 | C4-1/8-10-604R-F |
| R125 | 0698-3279 | 0 |  | RESISTOR 4.99K 1\% .125WF TC=04=100 | 24546 | Ca-1/8-10-4991-F |
| R120 | 0698-3279 | 0 |  | RESISTOR 4.99K $1 \pm .125 \mathrm{~W}$ F TC=040100 | 24546 | Ca-1/8-10-4991-F |
| R127 | 0698-3497 | 4 |  | RESISTOR 0.04 K 1 t , 125W F TC=04-100 | 24540 | C4-1/8-70-604R-F |
| R128 | 0757-0161 | - |  |  | 24546 | C4-1/0-10-604R-F |
| R131 | 0683-5125 | 8 |  |  | 01121 | $C B 5125$ |
| R133 | 0757-0437 | 2 |  | RESISTOR 4.75k $1 \times .125 \mathrm{~W}$ F TC=04-100 | 24546 | C4-1/8-70-4751-F |
| R134 | 0698.4020 | 1 |  | RESISTOR 9.53 K 1\% , 125 W F FC. $0+0100$ | 24546 | ca-1/8-70-9531-F |
| R13 R130 | $0683-1525$ $0757-0280$ | 4 |  |  | 01121 24546 | C81525 ${ }_{\text {ca-1/8-10-1001-F }}$ |
| R137 R138 1 | $\begin{aligned} & 0683-5125 \\ & 0757-0280 \end{aligned}$ | 8 3 |  | RESISTOR 5,1K 5X .25W FE TCE-400/4700 RESISTOR LK $1 \times, 125 W$ F TCE040 100 | 01121 24546 | $\begin{aligned} & \operatorname{CB5} 125 \\ & \operatorname{Co-1/8-70-1001-F} \end{aligned}$ |
| R139 | 0683-3025 | 3 |  | RESISTOR 3K 5X, 25W FC TC= $4001+700$ | 01121 | CB3025 |
| R140 | 0698.4123 | 5 |  |  | 24546 | C4-1/8-70-490R-F |
| R141 | 0698-4123 | 5 |  | RESISTOR 409 1\% . 125 W F TC $=0+0100$ | 24546 | C4-1/B-10-490R-F |
| R142 $R_{143}$ | $\begin{aligned} & 0757=0346 \\ & 0698.4435 \end{aligned}$ | 2 |  | RESISTOR $101 \% .125 \mathrm{~W}$ TCFO4-100 RESISTOR 2.49K ix. 125 W F TCEO4-100 | 24546 | $\begin{aligned} & \operatorname{Ca-1/B-TO-10RO-F} \\ & \operatorname{ca-1/8-TO-2491-F} \end{aligned}$ |
| R144 | 0698-3358 | 6 |  |  | 03888 | PMES5-1/8-10-1001-D |
| R145 R146 | 0757-0283 | 6 |  | RESISTOR 2K ix .125w F TC=040100 | 24546 | C4-1/8-10-2001-F |
| R146 | 0698.4446 | - | 1 | RESISTOR 3.4K 1x.125w F TCFO+=100 | 24546 | Ca-1/8-T0-34010F |

Table 8-1-4. Replaceable Parts (Cont'd).


## SERVICE GROUP 2 <br> TIMING

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## TIMING

## SERVICE GROUP 2

### 8.2.1. INTRODUCTION.

8-2-2. The Timing board performs two main functions. One is to interface data between the Input board and the Digital Filter board. The other is to provide clock signals to other circuits in the instrument.

## 8-2.3. GENERAL INFORMATION.

8-2-4. Although an oscilloscope and a frequency counter may be used to troubleshoot the Timing board, an easier and much quicker method involves the use of signature analysis (SA). Since the dividers operate at TTL levels and process serial data, an SA test may be used in several areas of the circuit to verify proper operation. When a trouble area is encountered, a quick check of the line in question with an oscilloscope will confirm noisy or intermittent TTL levels. Suggestion: be sure that the scope probe is properly compensated since high frequency square waves can appear to be distorted with an uncompensated probe.

## 8-2-5. Using The SA Flowcharts.

8-2-6. Because the signals on the Timing board are derived from a single source, it is easier to troubleshoot different signal paths by working back through the flowchart starting from the end resulting signal. Thus, if the calibration signal was defective, one would go to Flowchart 4 and proceed from the bottom of the diagram to the top.

## 8-2.7. TROUBLESHOOTING THE TIMING BOARD.

8-2-8. This board produces clocks for many functions on the board. The following problem groupings will help to narrow down the problem area. Before checking anything else, check that the power supplies ( +12 and +5 ) are good and that TP1 is oscillating at 45.875 MHz .

## 8-2-9. No Spectrum Or Poor Spectrum.

8-2-10. Check CH/A A/D, CH/B A/D, H/C and CLK 1 using Flowchart 1. CLK 2 is the SA clock, so that gets checked automatically. If an "end" signature is bad, work back through the chart. The signatures below the dashed line check the data interface circuits. To provide known data through the interface, the DC balance is adjusted to provide a string of all 1's or all 0's. This is accomplished by setting the INPUT SENSITIVITY to the 3 mV range, shorting the input and adjusting the BAL potentiometer either fully clockwise (CW) or counter-clockwise (CCW) as indicated on the flow chart.

## 8-2-11. PRN Not Programming Correctly.

8-2-12. Go through Flowchart 2. If the signature at $\mathrm{U} 7(15)$ is correct, the $\div \mathrm{N}$ counters are working properly. If the signature at $\mathrm{U} 7(15)$ is incorrect, SA cannot be used to troubleshoot
the counters because of the closed loop nature of the circuit. Once you've checked U29(9) for 11.5 or 9.2 MHz , look for stuck counter lines, and check the programming of $U 1$ and $U 2$ given with table at the end of this section.

## 8-2-13. Phase Incorrect.

8-2-14. This problem involves the effective sample rate trigger delay circuitry. Refer to Flowcharts 2 and 3 for troubleshooting. Also see Flowchart 5.

## 8-2-15. CAL Source And/Or HP.IB Clock Not Working.

8-2-16. Refer to Flowchart 4 for troubleshooting.

## 8-2-17. Impulse Output (Rear Panel) Not Working Or Phase In Free Run Incorrect.

8-2-18. Refer to Flowchart 5 for troubleshooting.


Figure 8-2-1. Flowchart 1: No or Poor Spectrum (Clk 1, Clk 2, H/C, A/D).


Figure 8-2-2. Flowchart 2: PRN Programming Incorrect.

Table 8-2-1. +N Counter Output SA vs. Span.

| Span | 0. Start | 200m |
| ---: | :---: | :---: |
| 25 kHz | 0003 | 000 U |
| 10 kHz | 000 U | 03 U 9 |
| 5 kHz | 03 U | P 733 |
| 2.5 kHz | P 733 | 5159 |
| 1 kHz | 6692 | 5 C 1 C |
| 500 Hz | 5 C 1 C | 7576 |
| 250 Hz | 7576 | 0 FHH |
| 100 Hz | 8844 | 1 F 8 C |
| 50 Hz | 1 F 8 C | P 5 H 2 |
| 25 Hz | P 5 H 2 | C 21 U |
| 10 Hz | AHC 3 | 52 C 9 |
| 5 Hz | 52 C 9 | 53 C |
| 2.5 Hz | 53 C |  |
| 1 Hz | 974 F |  |



Figure 8-2-3. Flowchart 3: Phase Incorrect.


Figure 8-2.4. Flowchart 4: CAL Source And/Or HP-IB Clock Not Working.


Figure 8-2-5. Flowchart 5: Impulse Not Working or Free-Run Phase Incorrect.


Program Codos (Octal) For A3U1 and U2

| Display BW (Hz) | $\begin{aligned} & \text { Basaband } \\ & \text { P. Code } \\ & (\text { P15 } \end{aligned}$ | ${ }_{(\mathrm{P} 15}^{\text {2oom }} \text { - Pol }$ |
| :---: | :---: | :---: |
| 25,000 | 177776 | ----- |
| 10,000 | 177775 | 177766 |
| 5,000 | 177766 | 177754 |
| 2,500 | 177754 | 177730 |
| 1,000 | 177716 | 177634 |
| 500 | 177634 | 177470 |
| 250 | 177470 | 177160 |
| 100 | 177014 | 176030 |
| 50 | 176030 | 174060 |
| 25 | 174060 | 170140 |
| 10 | 166170 | 154360 |
| 5 | 154360 | 120740 |
| 2.5 | 130740 | X |
| 2. | 036260 | x |





| PRN CLOCK RATES at A3U32\#11 |  |  |  |
| :---: | :---: | :---: | :---: |
| Selected Span | 0.25 kHz | 0.Start | 200M |
| 25 kHz | 1.638 mHz | 1.638 mHz | 819.2 kHz |
| 10 kHz | - - - | 655.4 kHz | 327.2 kHz |
| 5 kHz | --- | 327.7 kHz | 163.8 kHz |
| 2.5 kHz | - - - | 163.8 kHz | 81.9 kHz |
| 1.0 kHz | --- | 65.5 kHz | 32.77 kHz |
| 500 Hz | --- | 34.8 kHz | 16.38 kHz |
| 250 Hz | --- | 16.4 kHz | 8.19 kHz |
| 100 Hz | --- | 6.55 kHz | 3.27 kHz |
| 50 Hz | ---- | 3.27 kHz | 1.638 kHz |
| 25 Hz | - - - | 1.638 kHz | 818 Hz |
| 10 Hz | --- | 655 Hz | 328 Hz |
| 5 Hz | --- | 327.8 Hz | 164 Hz |
| 2.5 Hz | --- | 163.8 Hz | --- |
| 1.0 Hz | --- | 65.4 Hz | - - - |

Figure 8-2.8. PRN Clock Rates

| CLOCK RATES FOUND AT U31 \#8 |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Selacted Span | $0-25 \mathrm{kHz}$ | 0-Start | Set Start | Set Center |
| 25 kHz | 5.734 mHz | 5.734 mHz | 2.867 mHz | 2.867 mHz |
| 10 kHz | - - | 2.294 mHz | 1.146 mHz | 1.146 mHz |
| 5 kHz | - | 1.147 mHz | 573.4 kHz | 573.4 kHz |
| 2.5 kHz | - - - | 573.5 kHz | 286.7 kHz | 186.7 kHz |
| 1.0 kHz | --- | 22.93 kHz | 114.7 kHz | 114.7 kHz |
| 500 Hz | --- | 114.7 kHz | 57.34 kHz | 57.35 kHz |
| 250 Hz | - | 57.34 kHz | 28.67 kHz | 28.67 kHz |
| 100 Hz | - - | 22.94 kHz | 11.468 kHz | 11.47 kHz |
| 50 Hz | - | 11.47 kHz | 5.734 kHz | 5.73 kHz |
| 25 Hz | - - | 5.73 kHz | 2.867 kHz | 2.87 kHz |
| 10 Hz | - - - | 2.294 kHz | 1.147 kHz | 1.147 kHz |
| 5 Hz | --- | 1.147 kHz | 573.4 Hz | 573.4 Hz |
| 2.5 Hz | - | 573.4 Hz | - | - - |
| 1.0 Hz | - - - | 229.4 Hz | - - - | - - |

Figure 8-2.9. Clock Rates Found At U32 Pin 11.

Pulse rates found at the Impulse Out BNC (valid when the front panel noise source is set to periodic).

|  |  |  |  |  | Pulse Width |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 0.25 | $0 . S t a r t$ | Set Stert, Set Centar | Rep Ratefrequency |  |  |  |
| 25 kHz | $1.2 \mu \mathrm{~s}$ | $2.4 \mu \mathrm{~s}$ | $2.4 \mu \mathrm{~s}$ | 10 ms | 100 Hz |  |  |
| 10 kHz | $1.2 \mu \mathrm{~s}$ | $3 \mu \mathrm{~s}$ | $6.1 \mu \mathrm{~s}$ | 25 ms | 40 Hz |  |  |
| 5 kHz | $1.2 \mu \mathrm{~s}$ | $6 \mu \mathrm{~s}$ | $12.2 \mu \mathrm{~s}$ | 50 ms | 20 Hz |  |  |
| 2.5 kHz | $1.2 \mu \mathrm{~s}$ | $12 \mu \mathrm{~s}$ | $24.5 \mu \mathrm{~s}$ | 100 ms | 10 Hz |  |  |
| 1.0 kHz | $1.2 \mu \mathrm{~s}$ | $31 \mu \mathrm{~s}$ | $60.1 \mu \mathrm{~s}$ | 250 ms | 4 Hz |  |  |
| 500 kHz | $1.2 \mu \mathrm{~s}$ | $61 \mu \mathrm{~s}$ | $122 \mu \mathrm{~ms}$ | 500 ms | 2 Hz |  |  |
| 250 kHz | $1.2 \mu \mathrm{~s}$ | $122 \mu \mathrm{~s}$ | $245 \mu \mathrm{~s}$ | 1000 ms | 1 Hz |  |  |
| 100 kHz | $1.2 \mu \mathrm{~s}$ | $305 \mu \mathrm{~s}$ | .61 ms | 2500 ms | .4 Hz |  |  |
| 50 kHz | $1.2 \mu \mathrm{~s}$ | .61 ms | 1.22 ms | 5000 ms | .2 Hz |  |  |
| 25 kHz | $1.2 \mu \mathrm{~s}$ | 1.22 ms | 2.45 ms | 10000 ms | .1 Hz |  |  |
| 10 kHz | $1.2 \mu \mathrm{~s}$ | 3.05 ms | 6.1 ms | 25000 ms | .04 Hz |  |  |
| 5 kHz | $1.2 \mu \mathrm{~s}$ | 6.01 ms | 12.2 ms | 50000 ms | .02 Hz |  |  |
| 2.5 kHz | $1.2 \mu \mathrm{~s}$ | 12.22 ms | 12.2 ms | 100000 ms | .01 Hz |  |  |
| 1.0 kHz | $1.2 \mu \mathrm{~s}$ | 30.50 ms | 12.2 ms | 2500 sec. | .004 Hz |  |  |

Figure 8-2-10. Pulse Rates Found at Impulse Out B.N.C.

Table 8-2-2. Replaceable Parts.

| Reference Designation | HP Part <br> Number | $\begin{aligned} & \mathbf{C} \\ & \mathbf{D} \end{aligned}$ | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{4} 3$ | 03582-66503 | 1 | 1 | Pe ASSEmbly, timing | 28480 | 03582-66503 |
| $C 1$ $C 2$ | 016003847 016003455 | $\stackrel{9}{9}$ |  | CAPACITOREFXD . 01 UF 100 -0X SOVDC CER CAPACITOR-FXD 470PE *-10X IKVDC CER | 28480 28480 | $0160-3847$ 0160.3455 |
| C3 | 016003455 01600095 | 5 2 | 2 | CAPACITOR=FXD OIOPF +G5x 100VDC MICA | 28480 28480 | 01600.345 $0160-0945$ |
| ${ }^{4}$ | 0121-0142 | 9 |  | CAPACITOR-V TRMR-MICA 16-150PF 175V | 72136 | T51417-5 REV. 6 |
| C5 | 0160-2199 | 2 |  | CAPACITOR-FXD 30PF +-5x 300VDC MICA | 28480 | 0160-2190 |
| C 7 | 0160-2204 | 0 |  | CAPACITOR-FXD 100PF +-5x 300VDC MICA | 28480 | 0160-2204 |
| ${ }_{6} 8$ | 0160-2204 | 0 |  | CAPACITOREFXD 100PF +05x 300VDC MICA | 28480 | 0160-2204 |
| 610 $C_{1} 1$ | $0160-2257$ 0160.3847 | 3 | 1 |  | 28480 28480 | $0160-2257$ $0160-3847$ |
| c12 | 0160-3847 | 9 |  | CAPACITOR-FXD :OIUF +100-0X SOVDC CER | 28480 | $0160-3847$ |
| 513 | 0160-3847 | 9 |  |  | 28480 28480 | $0160=3847$ $0160-3847$ |
| ¢15 | $0160-3847$ $0160-3847$ | 9 |  |  | 28480 | 016003847 0160.3847 |
| 516 | 0160-3847 | 9 |  | CAPACITOR-FXD .01UF + $10000 \times$ SOVDC CER | 28480 | 0160-3847 |
| 617 | 0160-3847 | $\bigcirc$ |  | CAPACITOR-FXD . $014 \mathrm{SF}+100=0 \%$ SOVDC CER | 28480 | 0160-3847 |
| ${ }^{6} 18$ | 0160-3847 | 9 |  | CAPACITOR-FXD . 01 UF +10000\% SOVDC CER | 28480 | 016003847 |
| 619 | 01600-3847 | 9 |  | CAPACITOR-FXD O1UF +100-0X SOVDC CER | 28480 | 0160-3847 |
| C20 | 0180-0194 | 5 | 2 | CAPAEITOREFXD 150UF+-10X 15VDE TA | 56289 | $1500157 \times 901582$ |
| C21 | 0160-3847 | 9 |  | CAPACITOR-FXD . O1UF +100-0X 50VDE CER | 28480 28480 | 0160-3847 |
| C22 | 0160-3847 | 9 |  | CAPACITOR-FXD . $01 \mathrm{UF}+100=0 \mathrm{~S}$ SOVDC CER | 28480 | 016003847 |
| 623 | 0160-3847 | 9 |  | CAPACITOR-FXD . 01 UF $10000 \%$ SoVDC CER | 28480 20480 | 0160.3847 0160.3847 |
| 624 625 | 016003847 $0160-3847$ | 9 |  |  | 28480 28480 | 016003847 $0160-3847$ |
| 626 | 0160-2264 | 2 |  | CAPACITOR-FXD 20PF +-5x Soovoc CER $0+=30$ | 28480 | $0160-2204$ |
| C27 | 016003847 | 9 |  | CAPACITOR-FXD . 01 UF (100-0\% SOVOC CER | 28480 | 0160-3847 |
| CR1 | 1901-0347 | 1 | 2 | DIDDE-SCHOTTKY 8V | 28480 | 1901-0347 |
| CR? | 1901-0347 | 1 |  | DIODE-8CHOTTKY 8V | 28480 | 190100347 |
| $\mathrm{J}_{1}$ | 1251-5202 | 8 | 12 | CONNECTOR S-PIN M POST TYPE | 28480 | 1251-5202 |
| b1 | $9100-3345$ | 5 | 1 | COILCMLD $2 \mathrm{UH} 5 \mathrm{5x}, 1550 \mathrm{X}, 3756 \mathrm{GaNOM}$ | 28480 | 9100.3345 |
| 63 | 9100.2254 | 3 | 1 | COILemLD 390NH 10X OE35 .0950X.25LG-NOM | 28480 | $9100-2254$ |
| 01 | 1854-0215 | 1 | 8 | TRANSISTOR NPN SI PDa 350 MW FTESOOMHZ | 04713 | 8ps 3611 |
| 02 | 1854.0233 | 3 | 2 | TRANSISTOR NPN $2 N 3866$ S1 TOE39 PDEIW | 01928 | $2 N 3866$ |
| 03 | 185300203 | 5 | 3 | TRANSISTOR PNP SI TO-18 PDE360MW | 28480 | 185300203 |
| 048 | $1853-0203$ $1853-0203$ | 5 |  | TRANSISTOR PNP SI PO-18 PDE 360 MW TRANSISTOR PNP SI PO-18 PDE360MW | 28480 28480 | $1853-0203$ $1853-0203$ |
| Q6 | 1854-0019 | 3 | 1 | TRANSISTOR NPN SI TO-18 PDE360 ${ }^{\text {W }}$ | 28480 | 1854-0019 |
| R1 | 0683-7525 | b | 1 | RESISTOR 7.5K 5x .25W FC TCE-400\% ${ }^{\text {\% }} 700$ | 01121 | ce7525 |
| $\mathrm{R}_{2}$ | 0683-4725 | 2 | 6 | RESISTOR 4,7K 5x, 25W FC TCE=400/+700 | 01121 | CB4725 |
| R3 | 0683.4715 | 0 | 4 | RESISTOR 470 5x, 25W FC TCE=400/4600 | 01121 | CB4715 |
| $\mathrm{Ra}_{4}$ | O6R3-2025 | , |  |  | 01121 | CB2025 |
| Rs | 0683-1835 | $\bigcirc$ | 1 | RESISTOR 18K 5x. 25W FC TC=-400/ 8 800 | 01121 | C81835 |
| $\mathrm{R}_{6}$ |  |  | 1 |  | 01121 | $C B_{1235}$ |
| R\% <br> Ra | $0683-4715$ $0683-1025$ | 0 |  |  | 01121 01121 | C84715 $\mathrm{CB1025}$ |
| R10 | 0683-2015 | 9 | 2 | RESISTOR 200 5x . 25 W FC TCE-400/4000 | 01121 | CB2015 |
| 811 | 0683-1025 | 9 |  | RESISTOR 1 K 5 S . 25 W FC TC= $4001+600$ | 01121 | C81025 |
| R1? | 0683-1015 | 7 | 6 |  | 01121 | C81015 |
| R13 | 0683-2025 | , |  | RESISTOR 2K 5x. 25 W FC TCE-4001+700 | 01121 | C82025 |
| R14 | 0683 -8215 | 3 |  | RESISTOR B20 5x, 25W FC TCE=400/\$600 | 01121 | CB8215 |
| R15 | 0683-3315 | 4 | 2 | RESISTDR 330 5x. 25 W FC TCE-400/4600 | 01121 | C83315 |
| R10 | 0683-2015 | 9 |  | RESISTOR 200 5x, 25 WWE FCE-400/4600 | 01121 | C82015 |
| 817 | 0683-5105 | 4 | 4 | RESISTOR 51 5x . 25 W FC TCE-400/ +500 | 01121 | CB5105 |
| R1P | 0683-3915 | 0 |  | RESISTOR 390 5*. 25 W FC TCE-400/1600 | 01121 | CB3915 |
| 819 | 0683-3915 | 0 |  | RESISTOR 390 5x, 25 W FC TCE-400/4600 | 01121 | C83915 |
| R20 | 0683-2405 | 1 | 2 | RESISTOR 24 5x. 25 W FC TCE=400/ 5500 | 01121 | C82405 |
| R21 R22 | $\begin{aligned} & 0683-4705 \\ & 0683-2405 \end{aligned}$ | 8 | 2 | RESISTOR 47 5x. 25 W FC TCE-400/ $\$ 500$ RESISTOR 24 5x. 25WFC TCE=400/ $\$ 500$ | $\begin{aligned} & 01121 \\ & 01121 \end{aligned}$ | $\begin{aligned} & C B 4705 \\ & C B 2405 \end{aligned}$ |
| $U_{1}$ | 1820-1730 | 6 | 14 | IC FF PTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN74L3273N |
| 42 | 1820.1730 | 6 |  | IC FF TTL LS D-TYPE PDOSEDGE-TRIG COM | 01295 | 8N74LE273N |
| $U_{5}$ | 1820-1997 | 7 | 5 | IC FF PTL LS D=TYPE POS-EDGE-TRIG PRL-IN | 34335 | SN74LS374PC |
| $U_{6}$ | 1820-1997 | 7 |  | IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN | 34335 | SN74LA374PC |
| 47 | 1820-1430 | 3 |  | IC CNTR TTL LS AIN SYNCHRD POS-EDGE-TRIG | 01295 | sN74LBIbIN |
| UR | 1820-1430 | 3 |  | IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG | 01295 | 8n74L8161N |
| $\cup 9$ | 1820-1430 | 3 |  | IC CNTR TTL LS BIN SYNCHRO PDS-EDGE-TRIG | 01295 | 8NT4LS161N |
| 410 | 1820-1430 | 3 |  | IC CNTR TTL LS BIN SYNCHRD POS-EDGE-TRIG | 01295 | SNT4LSI61N |
| 411 | 1820-1430 | 3 |  | IC CNTR TTL LS BIN SYNCHRO POS-EOGE-TRIG | 01295 | 8N74L8161N |
| U12 | 1820-1430 | 3 |  | IC CNTR TTL LS BIN SYNCNRD POSPEDGE-TRIG | 01295 | 8NTALSIGIN |

Table 8-2-2. Replaceable Parts (Cont'd).


## SERVICE GROUP 3

## DIGITAL FILTER AND LOCAL OSCILLATOR

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# DIGITAL FILTER AND LOCAL OSCILLATOR SERVICE GROUP 3 

## 8-3.1. INTRODUCTION.

8-3-2. The Digital Filter and Digital Local Oscillator work in combination to provide low pass filtering of band translated signals. The Digital Filter operates on the data in quadrature which requires the Local Oscillator to output both SINE and COSINE values. These values are then multiplied by the input data to give both real and imaginary components. Each of the components is filtered and placed in memory through a direct memory access (DMA) firmware routine.

## 8-3-3. GENERAL INFORMATION.

8-3-4. Both the Digital Filter and the Local Oscillator must be synchronized together which requires that the Timing (A3) board be in operational order. The Digital Filter and Local Oscillator should be troubleshot using the front panel internal self tests before board level troubleshooting is initiated. Digital filter chips are identical and may be switched between sockets to confirm a malfunction. Use extreme caution in handling any of the LSI devices since damage may be caused by static discharge.

## 8-3-5. TROUBLESHOOTING THE DIGITAL FILTER.

8-3-6. In order to process data, the Digital Filter must have inputs from several other boards. This interdependency makes troubleshooting difficult since all interrelated boards and processes must also be working. This situation indicates a need to troubleshoot (at least at a fundamental level) from a system standpoint. Therefore, overall troubleshooting should begin with the Front Panel Self Tests which will aid in establishing the cause of the malfunction and may even indicate the bad component.

Digital Filter Test Table

| Test Mode (oct) | Filter Chips Tested | Corresponding Instrument Mode |
| :---: | :---: | :--- |
| 000000 | 2 |  |
| 000001 | 1 | None |
| 000002 | 3 | Chan A Baseband |
| 000003 | 1,3 | Chan B Baseband |
| 000004 | 4 | Dual Chan Baseband |
| 000005 | 1,2 | None |
| 000006 | 3,4 | Chan A Zoom |
| 000007 | $1,2,3,4$ | Chan B Zoom |
|  |  | Dual Chan Zoom |

8-3-7. If the Digital Filter will not respond to any of the Front Panel Tests, then a procedure (given below) can be used to check the output of the support circuits located on the Digital Filter D (A5) board.

## 8-3-8. The Clock Driver Circuit.

8-3-9. The clock driver circuit receives its input from the Timing board (A3-Schematic C). The circuit outputs are two 12 V (nominal) rectangular waveforms which are gated such that one must be low in order for the other to be high at any time. Check TP1 and TP2 and verify that the outputs correspond to the conditions indicated in the following illustration. Then repeat for TP13 and TP14.


Figure 8-3-1. Clock Driver Output.
8-3-10. Data Input Buffer.
8-3-11. The input data buffer may be checked by verifying that digital data is available on the output lines.
a. Connect a two-channel oscilloscope to test points TP3 and TP5. Set the trigger controls to trigger off the channel connected to TP3. TP3 is the SYNC source for the digital filters and signals the filter chips when data on the other buffer output lines is valid.
b. Use the untriggered channel to confirm that signals are present on the signals lines as indicated in Figure 8-3-2.

NOTE
To check data on TP4 and TP10, the FREQUENCY MODE switch should be set to SET START or SET CENTER.


Figure 8-3-2. Output From Data Input Buffer.

## 8-3-12. DMA Request Circuit.

8-3-13. The DMA (direct memory access) circuit provides a signal to the processor (DMAR) which allows the Digital Filter access to memory through a firmware subroutine. The filter chips send a pulse on their CDR (chip data ready) lines when the input data has been low pass filtered. The AND gates perform logic operations which allow the following combinations of CDR inputs to a one of eight multiplexer.

| Multiplexer Input | CDR Line | Function |
| :---: | :--- | :--- |
| D6 | CDR2 | Cosine (real) Test |
| D1 | CDR1 | CH A Baseband |
| D2 | CDR3 | CH B Baseband |
| D3 | CDR1 \& CDR3 | CH A \& CH B Baseband |
| D4 | CDR4 | Sine (imaginary) Test |
| D5 | CDR1 \& CDR2 | CH A Zoom (band analysis) |
| D6 | CDR3 \& CDR4 | CH B Zoom |
| D7 | CDR1, CDR2, CDR3, CDR4 | CH A \& CH B Zoom |

8-3-14. These lines may be checked by using TP3 as a trigger and then placing the nontriggered channel on the selected line. The pulse should appear relative to the SYNC B signal as follows:


Figure 8-3-3. Chip Data Ready (CDR) From Digital Filters.

8-3-15. The multiplexer (U9) is coded by the controller to select one of the eight combinations for output to a D latch (U19). These signals clock the latch, setting the output $\overline{\mathrm{Q}}$ low, to indicate data is ready for memory. The latch is reset by a combination of processor command (IS15) and controller command (LAST).

## 8-3-16. The Controller.

8-3-17. Once a DMA has been requested, it remains up to the Controller to sequence the output of the digital filter chips onto the 16 -line Data Bus. The Controller consists of a data latch, ROM and programmable counter.

8-3-18. The data latch is clocked by the Processor to retain data off the I/O Bus corresponding to the operating mode (single, dual, or combinations thereof). The output of the latch (U17) in combination with the output of a programmable counter (U11) addresses a ROM (U16) which supplies the following outputs:
a. The $Y \emptyset$ output is the load command to the programmable counter which sets the counter to zero. Thus, the two output lines from the counter can give four combinations of input address for every latch output.
b. Y2-Y5 are chip enable lines which allow each digital filter chip to output 16 bits of parallel data in sequence on the 16 bit data bus.
c. Y1 goes high when the last chip of the sequence has output data on the data bus.

8-3-19. See Table 8-3-1 which is also a flowchart that describes the states of the inputs and outputs of ROM U16.

Table 8-3-1. Truth Table For ROM U16.

|  | $\begin{aligned} & \text { D } \\ & \mathbf{C} \\ & \mathbf{2} \\ & \text { E } \end{aligned}$ | $\begin{aligned} & \mathbf{D} \\ & \mathbf{C} \\ & \mathbf{1} \\ & \mathbf{D} \end{aligned}$ | D C c c | B | A | Y7 | Y6 | $\begin{aligned} & \bar{C} \\ & \mathrm{E} \\ & 4 \\ & \mathbf{4 5} \end{aligned}$ | $\begin{gathered} \overline{\mathrm{C}} \\ \mathrm{E} \\ 3 \\ \mathrm{Y} \end{gathered}$ | $\begin{gathered} \bar{C} \\ E \\ 2 \\ \mathrm{Y} 3 \end{gathered}$ | $\begin{gathered} \overline{\mathbf{C}} \\ \mathbf{E} \\ \mathbf{1} \\ \mathbf{Y 2} \end{gathered}$ | $\begin{gathered} \mathbf{L} \\ \mathbf{A} \\ \mathbf{S} \\ \mathbf{T} \\ \mathbf{Y 1} \end{gathered}$ | $\begin{aligned} & \mathbf{L} \\ & \mathbf{O} \\ & A \\ & \mathbf{D} \\ & \mathbf{Y} \end{aligned}$ | Octal |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Filt \#2 Test | 0 | 0 | 0 | 0 | 0 |  |  | 1 | 1 | 0 | 1 | 1 | 0 | 66 |
| CH A BB* | 0 | 0 | 1 | 0 | 0 |  |  | 1 | 1 | 1 | 0 | 1 | 0 | 72 |
| CH B BB | 0 | 1 | 0 | 0 | 0 |  |  | 1 | 0 | 1 | 1 | 1 | 0 | 56 |
| CH A,B BB | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | 1 1 | 1 1 | 0 | 0 1 |  |  | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & 71 \\ & 56 \end{aligned}$ |
| Filt \#4 Test | 1 | 0 | 0 | 0 | 0 |  |  | 0 | 1 | 1 | 1 | 1 | 0 | 36 |
| CH A Z | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | 0 | 1 1 | 0 | 0 1 |  |  | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & 71 \\ & 66 \end{aligned}$ |
| CH B Z | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | 1 1 | 0 0 | 0 0 | 0 1 |  |  | $\begin{aligned} & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \end{aligned}$ | $\begin{array}{r} 55 \\ 36 \end{array}$ |
| CH A, BB, Z | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | 1 1 1 1 | 1 1 1 1 | 0 0 1 1 | 0 1 0 1 |  |  | 1 1 1 0 | $\begin{aligned} & 1 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 0 \end{aligned}$ | 71 65 55 36 |
| -BB = Baseband | ; | 200 |  |  |  |  |  |  |  |  |  |  |  |  |

## 8.3-20. The Overload Circuit.

8-3-21. The overload circuit performs two functions:
a. Immediate overloads are sensed which results in a front panel indicator signal.
b. Overload information is latched by an R-S flip-flop and saved for processor interrogation. This data is shown on the display by the printed "OVERLOAD' warning.

8-3-22. The inputs to the overload circuit consist of digital filter chip overload (OVL) and overflow (OVF) outputs, and clipping level indicators (clip A and clip B) from the input
(A1-Schematic A) board. These inputs are decoded by logic gates which drive R-S flip-flops U22 and buffer amplifiers U27.

8-3-23. The DC 2 input from the controller gates overload data from digital filter chips \#2 (A imaginary) and \#4 (B imaginary) for band analysis mode operation. Processor outputs IS13 and IC1 reset U22 and gate U22 outputs onto the I/O Bus (IOB15 and IOBø).

8-3-24. To check the operation of the overload circuit, supply an input signal to each channel. Slowly increase the amplitude until the displayed spectrum approaches the top horizontal graticule. When $100 \%$ of full scale is reached, the overload signals should appear at the outputs of the overload circuit. Check every combination of overload by changing the FREQUENCY MODE switch and INPUT MODE switch.

## 8-3-25. The Trigger Circuit.

8-3-26. The trigger circuit is composed of latches which detect the rising or falling edge of the trigger input signal from the $\operatorname{Input}(\mathrm{A} 1)$ board. Processor signals B0 and B1 set the slope and are latched in U3 by OSø. A combination of B2 and OSØ resets the slope latches U5. The trigger input is applied to U5B and inverted at U5A. Thus, whichever latch has the D input high will have the correct Q low true output when the trig signal occurs. The trigger circuit output also enables the DMA output latch.

8-3-27. To check the trigger circuit, apply an input signal to Channel A. While observing the TIME display, slowly rotate the TRIGGER LEVEL control. An output signal at TP6 should appear on both negative and positive level settings. Change the setting of the slope switch and observe the TP6 while varying the TRIGGER LEVEL.




## 8-3.28. TROUBLESHOOTING THE LOCAL OSCILLATOR.

8-3-29. A quick check of the L.O. may be accomplished by performing the following procedure:
a. Verify that the LINE switch is OFF.
b. Place the A4 board on an extender.
c. Set the LINE switch to ON, FREQUENCY MODE to SET CENTER, and FREQUENCY ADJUST for 4779 Hz .
d. Turn the DC BAL on Channel A fully clockwise and move jumper A4J2 to " T " (test).
e. Return the FREQUENCY MODE switch to $0-25 \mathrm{kHz}$ and adjust the SENSITIVITY controls for a proper display.
f. Except for spectral lines at 4779 Hz and 22 kHz , no other spectral displays above the noise floor should be seen. This indicates a properly working L.O. If the L.O. passes this test and there were no phase problems, return A4J2 to " $R$ " (run).
g. Short the input and use the TIME display to set DC BAL for 0 Vdc as indicated by the trace on the center horizontal graticule.

8-3-30. More extensive testing of the L.O. may best be performed with the use of signature analysis. An oscilloscope can be used to check absolute signal levels and noisy signal lines. However, signal data, as referenced to time, varies greatly and is repetitive only over long periods.

8-3-31. As a secondary test of the L.O., see SA Sine and Cosine Quick Check. For phase verification see SA Test g.

## 8.3-32. Signature Analysis Procedures.

8-3-33. To use the SA procedures, preset the 3582A as follows:
A4J1 to "T" (test); A4J2 and J3 to "R" (run).
FREQUENCY MODE to SET CENTER
FREQUENCY ADJUST to 101 Hz
SPAN to 25 Hz
INPUT MODE to BOTH
TRIGGER REPETITIVE to ON
TRIGGER LEVEL to FREE RUN
8-3-34. Connect the -hp- 5004A Signature Analyzer to test jack J6 as follows:

| GND | J6(1) |
| :--- | :--- |
| CLK | J6(3) |
| START | J6(4) |
| STOP | J6(5) |

The +5 signature should be 35 H .
8-3-35. Sine and Cosine Quick Check. With the 5004A connected to test jack J6, the sine and cosine outputs (serial) may be checked at the following points:

| Location | Signature |
| :--- | :---: |
| TP10 | 063 U |
| U126 (13) | 16 H 6 |

U388 for REV A, B AND C. This signature may be unstable on a working board.

8-3-36. If these signatures check correctly, the L.O. is probably functioning properly. To quickly check the phase output, proceed to SA Test g . If these signature are incorrect, continue.

## NOTE

1. For SA to work on this board, the Timing board (A3) and the DMAR signal from the Digital Filter board (A5) must be operational. These inputs may be checked by placing the SA probe on the +5 V supply and obtaining the signature 35 HI .
2. If wrong signatures are obtained, recheck the $S A$ setup procedures preceeding each test section.

8-3-37. Perform the following steps:
a. Check the following signatures (timing and control):

| U127 (2) | P7A2 |
| ---: | ---: |
| 6 | 6572 |
| 7 | 50 A 3 |
| 10 | $35 A 5$ |
| 15 | F18U |

If ok , go to b , if not check:

| U130 (11) | 85UP | U131 (14) | AP63 |
| ---: | ---: | ---: | ---: |
| 12 | U251 | 13 | H8AA |
| 13 | $3 C 14$ |  |  |
| 14 | 134 U |  |  |

If ok, check:
U128 (12) 9137
11 A146
$10 \quad 3538$
9 831P
If ok, the problem is probably with U127.
b. Move SA CLK to TP4 and check signatures on the input latches, U101 and U104. (+5 signature C21U)

| U101 (12) | C21U | U104 (12) | C21U |
| ---: | ---: | ---: | ---: |
| 9 | 0000 | 9 | 0000 |
| 15 | 0000 | 15 | 0000 |
| 6 | 0000 | 6 | 0000 |
| 16 | 0000 | 16 | 0000 |
| 5 | 0000 | 5 | 0000 |
| 19 | 0000 | 19 | 0000 |
| 2 | 0000 | 2 | 0000 |

If these check ok, the board is set to correct frequency. Proceed to Part C. If not ok, double check the test setup (set center-101 Hz, $25 \mathrm{~Hz}, \mathrm{SPAN}$, DUAL channel mode, repetitive and free run).

If the test set-up is ok, check the latches and I/O bus using front panel I/O bus test \#15 as follows:

## NOTE

Do this test only if previous signatures are incorrect.
To perform the front panel self test,

Obtain self-test mode by pressing RESET while holding in RESTART.
Select average \#256
Short A7J4 and push RESTART
Push RESTART until you get test \#15.
Set up the 5004A as follows:
CLK: OS13
START/STOP: I/O 15

+5 Signature: UFP6
Check the following signature pairs:

| U101 (3) | 01UF | U101 (2) | 026C | U104 (3) | 0001 | U104 (2) | 0295 |
| ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: |
| 4 | 07U3 | 5 | $016 F$ | 4 | 0007 | 5 | 0296 |
| 7 | 1UFP | 6 | $0 H 72$ | 7 | 001 U | 6 | $029 A$ |
| 8 | $7 U 39$ | 9 | $3 H 09$ | 8 | 007 U | 9 | 02 AA |
| 13 | UP73 | 12 | 7 HAF | 13 | 00 UP | 12 | 02 PA |
| 14 | 3U9F | 15 | 1H5C | 14 | 003 U | 15 | 028 A |
| 17 | 0UP7 | 16 | 0566 | 17 | 000 U | 16 | 0292 |
| 18 | 03U9 | 19 | 0369 | 18 | 0003 | 19 | 0294 |

Remove the short from A7J4 after this test.
c. With the 5004 A clock still on TP4, check the latches and adders by checking the signatures in the first column below. If an error is found, work across the table to check preceeding signatures.

| U111 (8) | 6819 | U108 (3) | HA06 | U102 (12) | 6819 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 7 | 98P3 | 4 | 638P | 1 | 98P3 |
| 6 | 4H5C | 6 | 356P | 2 | 4H5C |
| 5 | HPA7 | 11 | 7A9F | 3 | HPA7 |
| 4 | 85 C 1 | 13 | 16F5 | 6 | 9374 |
| 3 | 125C | 14 | 496P | U103 (12) | 85 C 1 |
| 2 | A89H | U109 (3) | A275 | 1 | 125C |
| 1 | F3UF | 4 | 0UU3 | 2 | A894 |
| U112 (8) | C24U | 6 | C35H | 3 | F3UF |
| 7 | U8PF | 11 | P3C3 | 6 | C30H |
| 6 | U63U | 13 | H8UF | U105 (5) | C24U |
| 5 | 9073 | 14 | 41FH | 3 | U8PF |
| 4 | 6481 | U110 (3) | 9205 | 14 | U63U |
| 3 | C36H | 4 | FHC4 | 12 | 9073 |
| 2 | 21FA | 6 | 872A | 9 | U684 |
|  |  |  |  | U106 (5) | 6481 |
| 1 | 3675 | 11 | H9H5 | 3 | C36H |
| 23 | 8C36 | 13 | 94U2 | 14 | 21FA |
| 22 | POUO | 14 | F7PF | 12 | 3675 |
|  |  | U114 (5) | P53F | 9 | 71FP |
| U110 (1) | C21U | 6 | 6POA | U107 (5) | P53F |
|  |  | 3 | U1UC | 3 | U1UC |
|  |  | 2 | C21U |  |  |

d. Move 5004A clock to TP-8 and check the parallel to serial converters as follows:

1. Check for 5A61 at U120 (12).
2. If bad, check back through U121-123.

| U121 (12) | C286 |
| :--- | :--- |
| U122 (12) | AH66 |
| U123 (12) | 4807 |

If these all have bad signatures, check the ROMS,
3. Move 5004A clock to TP2 and check for U55F at U116 (13).
4. If bad, check back through U117 and U118.

| U117 (12) | FA2U |
| :--- | :--- |
| U118 (12) | AU57 |

If all signatures are ok, the parallel to serial converters are working.
e. Move 5004A clock to TP-4 and check for 2637 at U115 (6). If this is ok, go to f. If bad, check the signatures below:

| U115 (5) | 8330 | U115 (13) | 9330 |
| ---: | ---: | ---: | ---: |
| 4 | 6819 | 12 | POUU |
| 3 | 1 H 52 | 11 | P141 |
| 2 | 5317 | 15 | FUP3 |
| 14 | FC98 |  |  |

If these are ok, U115 is probably bad.
f. Check the following signatures, clocking the 5004A on TP8.*

| U119 (7) | 32F2 | Sin Output* |
| :---: | ---: | :--- |
| U126 (13) | 17 HU | Cos Output |
| U125 (3) | 9961 |  |
| 4 | 6279 |  |
| 5 | 1 UU5 |  |
| 6 | 2133 |  |
| 10 | CP50 |  |
| 11 | 71 P 1 |  |
| 12 | 9639 |  |
| 13 | 65 H 5 |  |

Signature Table for D2. To be done only if all signatures in Section d, Part 2 are bad. Clock off TP-4.

| U111 (9) | 8330 |  |  |
| ---: | ---: | ---: | ---: |
| 10 | 6819 |  |  |
| 11 | 1 H52 | U113 (16) | 17AO |
| 13 | 5317 | 17 | 49P6 |
| 13 |  | 22 | POUO |
| 14 | FC98 | 23 | 8 8C36 |
| 15 | 9330 |  |  |
| 16 | POUU |  |  |
| 17 | P141 |  |  |
| U112 (9) | U7CU |  |  |
| 10 | 5COU |  |  |
| 11 | CFUP |  |  |
| 13 | F526 |  |  |
| 14 | F96A |  |  |
| 15 | HCC3 |  |  |
| 16 | $84 A 8$ |  |  |
| 17 | 1412 |  |  |
| U113 (9) | $87 A 1$ |  |  |
| 10 | F8C2 |  |  |
| 11 | UOFF |  |  |
| 13 | AC05 |  |  |
| 14 | H917 |  |  |
| 15 | 8324 |  |  |

If the $\sin$ output is ok, but U125 and U126 signatures are wrong, it's probably U125. If all the above are wrong, check U119, U124, and U126 signatures. U1 19 (2) and (3) should have already been checked in Sections $d$ and e.

| U119 (4) | 4 A 52 | U 124 (1) | 35 H 1 |
| ---: | :---: | :---: | ---: |
| 5 | F 070 | 3 | 0000 |
|  |  | 4 | 50 A 3 |
| U126 (9) | 35 H 1 |  |  |
| 8 | 6572 |  |  |

g. Trigger delay and phase. If phase is incorrect, check U135 and 134 signatures below. Clock on TP2.

| U135 (3) | H8AA | U134 (3) | 922U |
| ---: | ---: | ---: | ---: |
| 4 | 86 UP | 4 | C35U |
| 7 | 3 C 14 | 7 | 3C2U |
| 11 | 35 HI |  |  |
|  |  | 8 | U6U7 |
| 14 | 134 U | 11 | 35 HI |
| 17 | U251 | 13 | 3427 |
| 18 | AP63 | 14 | AH17 |
|  |  | 17 | AOHF |
|  |  | 18 | HPUA |



Figure 8-3-5. Schematic E Troubleshooting Quick Reference.




Table 8-3-2. Replaceable Parts.

\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Reference Designation \& HP Part Number \& C \& Oty \& Description \& Mfr Code \& Mfr Part Number <br>
\hline ${ }^{4} 4$ \& 03582-66504 \& 2 \& 1 \& pe assembly, local oseillator/prn \& 28480 \& 03582066504 <br>
\hline $\mathrm{C}_{1}$ \& 0160-3622 \& 8 \& \&  \& 28880
28480 \& 016003622
$0100-2222$ <br>
\hline C3 \& 16002222
010022
014000234
0 \& $?$ \& $\frac{1}{2}$ \&  \& 28880
72136 \&  <br>
\hline C4 \& 014000234
$0160-2585$ \& 0 \& 1 \&  \& 72136
28480 \& OM15F501F0300NVIC
$0160-2555$ <br>
\hline ${ }_{6} 6$ \& 0140-0223 \& 7 \& 1 \&  \& 72136 \& DM15P261P0300NVIC <br>
\hline c \& 0100.3538 \& 5 \& 1 \& CAPACITORaFXO 750PF +e5x 100VDC MICA \& 28480 \& 0100-3838 <br>
\hline c8 \& O160-2202
016003622 \& 8 \& 1 \&  \& 28480
28480 \& 016002202
016003622 <br>
\hline ${ }^{2} 10$ \& 01603622
016003847 \& $\stackrel{8}{9}$ \& \& CAPACITORFPXO OUUF* $+10000 \times$ SOVDC CER \& 28480
28480 \& 01003622
016003647 <br>
\hline $\mathrm{c}_{11}$ \& 0100-3847 \& - \& \& CAPACITOR-FXD .01UF +10000x 50VDC CER \& 28480 \& $0100 \cdot 1047$ <br>
\hline c
$c_{13}$
$c_{13}$ \& ( $0160-3847$ \& ? \& \&  \& 28480 \& 016003847
016003847 <br>
\hline ${ }_{1} 14$ \& $0100-3622$ \& 8 \& \&  \& 28480 \& 016003622 <br>
\hline $\mathrm{c}_{15}$ \& 0160-3622 \& - \& \& CAPACITOR-FXD . 1 UF , 80-20x loovde CER \& 26480 \& 016003622 <br>
\hline c
c19
cif \& 010003022
$0160-3622$ \& 8 \& \& CAPACITOR-FXD
CAPACITOR F \& 28880
28480 \& $0160-3622$
0160.3622 <br>
\hline ${ }^{18} 8$ \& -1600-3622 \& 8 \& \&  \& 26480 \& $0160-3622$ <br>
\hline ${ }^{c} 19$ \& $0160-3622$
$0100-3622$ \& 8 \& \&  \& 28880
28480 \& 016003622
$0160-3622$ <br>
\hline ${ }^{\text {c }} 0$ \& 7100-3622 \& 8 \& \& CAPACITOR-FXD .1UF *80-20x loovoc Cer \& 28480 \& 0160-3622 <br>
\hline $C 102$
$C 106$ \& 018000194
$0160-3847$ \& 5 \& \&  \& 50280
28480 \& $1500157 \times 001532$ $0160-3847$ <br>
\hline ${ }^{\text {c10 }} 10$ \& -10003847 \& 9 \& \&  \& 28480 \& 0160-3847 <br>
\hline c10
C 110 \& 016003847
$0160-3847$ \& $\stackrel{\square}{9}$ \& \&  \& 28480
28480 \& 016036897
$0160-3647$ <br>
\hline ${ }^{1} 112$ \& 010003847 \& 9 \& \& CAPACITOR-FPO .01UF +10000 50VDC CER \& 28480 \& 0100-3847 <br>
\hline $\mathrm{C}_{1} 15$ \& $0100-3847$ \& 9 \& \& CAPACITOR FFXD 01UF 010000x SOVOC EER \& 28480 \& 0160-3847 <br>
\hline cili \& O1603847
016003847 \& 9 \& \&  \& (28880 \& $0160-3847$
016003809 <br>
\hline $\mathrm{Clis}^{\text {c }}$ \& 016003847 \& $\bigcirc$ \& \& EAPACITOR-FXO :OIUP +100-0x Sovoc Cer \& 28480 \& 0160.3647 <br>
\hline ${ }^{\mathrm{J} 1}$ \& $1251-4822$
$1251-4822$ \& 8 \& - \& CONNECTOR
COP-PIN M POST \& 28880
28480 \& $1251-4822$
$1251-4822$

12 <br>

\hline ${ }^{3}$ \& \& 6 \& \&  \& 28480 \& | 12514822 |
| :--- |
| $1251-4822$ | <br>

\hline J 5 \& - \& \& \& CONNECTOR 3 -PIN M POST TYPE
CONNECTOR SPIN POST TYPE \& 28480
28480 \& $1251-4822$
1251.5202 <br>
\hline \& \& \& \& \& \& <br>
\hline \& 1251-5202 \& - \& \& CONNECTOR SOPIN M POST TMDE \& 28480 \& 125105202 <br>
\hline R1 \& 0698.7332
0098.3457
0 \& 4 \& 3 \&  \& 28480
28480 \& 069807332
0698.3457 <br>
\hline $R_{2}$
$R_{3}$ \& 009883457
069864525 \& $\stackrel{0}{i}$ \& $\stackrel{2}{2}$ \&  \& 28880
28546 \& $0698-3457$
$C 601 / 18=10-1873-F$ <br>
\hline R4 \& 0698-3271 \& 2 \& 2 \&  \& 24546 \& Ca-1/8-90-1153-F <br>
\hline RS \& 0098-4511 \& 5 \& 2 \& RESISTOR 86.0K 1\% .125w F TC00*-100 \& 24546 \& C 4 -1/8-10-8662-F <br>
\hline Ros \& 009804507
$0757-0463$ \& $\stackrel{9}{4}$ \& 2 \&  \& 24540
24546 \&  <br>
\hline Ra \&  \& 6 \& 2
2 \&  \& 24546
2346 \& C $401 / 85$-70-1433-F <br>
\hline R9 \& 0698.4536 \& ${ }_{4}^{6}$ \& 2 \&  \& 28480
24540 \& $0698-4536$
$C 401 / 8=70-54920 F$ <br>
\hline R10 \& 0698.4499 \& 8 \& 2 \& RESISTOR 54.09 14.125w F TC=0\$-100 \& 24540 \& C4-1/8-50-54920F <br>

\hline | $R_{11}$ |
| :--- |
| $R_{12}$ |
| 12 | \& 0698.44888

0698.4481 \& 5 \& 2 \&  \& 24540
24546 \& $C a=1 / 80-10-26720 F$
$C a=1 / 8=10-1652-F$ <br>
\hline ${ }_{\text {R }}^{13}$ \&  \& ${ }_{3}^{8}$ \& \&  \& 28546
24546
24546 \& C001/8-10-11020\% <br>
\hline R14 \& 0698.4020
0757044 \& 1 \& $\stackrel{4}{2}$ \&  \& 24546
24546 \&  <br>
\hline R16 \& \& \& 2 \& \& 24546 \& C401/8-T0-7681-F <br>
\hline R17 \& 069804472 \& 7 \& \& RESISTOR 7:60k ix :125N F YC00*-100 \& 24540 \& C4-1/8050-76810\% <br>
\hline R18 \& $0757-0441$
0698.4020 \& ${ }^{6}$ \& \&  \& 22496 \& CC-1/8-70-6251-F, <br>
\hline R19
R20 \& 0098.0020
0.908 .3264 \& 3 \& \&  \& 24546
24546 \& c $4=1 / 8=Y 0=0331-\%$
$C 8=1 / 8=10-1182-F$ <br>
\hline $\mathrm{R}_{21}$ \& 0698-4481 \& \& \& RESISTOR 10.5K ix. 125 M F TC00*-100 \& 24546 \& C4-1/8-10-1652-F <br>
\hline R22 \& 0698.44888 \& 5 \& \&  \& 24546
24546 \& C401/8070-26720\% <br>
\hline R23
R24 \& 009884499
0698.4536 \& $\stackrel{8}{4}$ \& \&  \& 24546
28480 \&  <br>
\hline R25 \& 0698-4520 \& 6 \& \& RESISTOR 143K ix : $125 \mathrm{NFHCO+-100}$ \& 24546 \& C $4=1 / 8=10-1433-F$ <br>
\hline R26
R27 \& 075700463
$0698=4507$ \& $\stackrel{4}{4}$ \& \& RESISTOR A2.5K 1 X , 125 N F TCoO+ 100 RESISTOR 76.8K ix. 125 F F TC=0+6 100 \& 24546

24546 \& $$
\begin{aligned}
& C 4=1 / 8-T 0-8252-F \\
& C 4-1 / 8-10-76620 F
\end{aligned}
$$ <br>

\hline R28 \& 0698-4511 \& 5 \& \&  \& 24546 \& C $4=1 / 8-70-8602 \mathrm{~F}$ <br>
\hline 829
830 \& 009883271
0698.4525 \& $\stackrel{2}{2}$ \& \&  \& 24546
24546 \& C401/8-70-1153-F <br>
\hline ${ }^{83}$ \& 0698.4525 \& 1 \& \& Resistor ie7k ix -125w F TC00*-100 \& 24546 \& C4-1/8-70-1873-F <br>

\hline  \& \[
$$
\begin{aligned}
& 0698=3457 \\
& 0698=7332
\end{aligned}
$$

\] \& $\stackrel{4}{4}$ \& \& | RESISTOR 316K ix, 125N F TC=0*-100 |
| :--- |
|  | \& 28480

28480
28480 \&  <br>
\hline  \& 210000552
0957 -0420 \& 3
3 \& 1 \&  \& 28480
24546 \& $2100-0552$
$C 4=1 / 8070=7510 \%$ <br>
\hline - \& 0698.4123 \& 5 \& \&  \& 24546 \& C $4=1 / 8=90=499 R-\nmid$ <br>
\hline
\end{tabular}

Table 8-3-2. Replaceable Parts (Cont'd).

| Reference Designation | HP Part Number | $\begin{aligned} & c \\ & 0 \\ & 0 \end{aligned}$ | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }_{8}^{2} 38$ | 0757-02033 |  | 5 |  | 20946 | Ca01/8-T0-2001-8 |
| 836 | - 07570289 | $\begin{aligned} & 2 \\ & 2 \end{aligned}$ | I |  | ${ }^{2}$ | Catile |
| ¢ | 07570043 0.5770270 | ${ }_{9}$ | 1 |  | 20586 <br> $\mathbf{2 5 4 6}$ |  |
|  | -0698-31548 | ¢ | 2 |  | 208546 |  |
|  |  |  |  | Retisaor |  | Catisioto |
| ${ }_{\text {R45 }}$ |  | 1 |  |  |  |  |
| R ${ }_{\text {Rab }}$ | 9757-0439 | d | 2 |  | 20546 |  |
| - | - | : |  |  |  | 边 |
| RS50 | - $\begin{aligned} & 0883-1025 \\ & 0757-0161\end{aligned}$ | ; |  |  | 01121 24546 |  |
| ${ }_{\text {Res }} \mathrm{R} 5$ | O698-3157 0757 P04az | 3 | 1 |  | 20546 | Ce401/8-T0-1902-F |
| Res | 975700492 | : |  |  |  |  |
| R35 | - 0096853572 | ${ }_{3}$ | 1 |  | 224964 |  |
| R55 | 0757,0280 | 3 |  |  | 24548 |  |
| ${ }_{\text {Ref }} 8$ |  | ? |  |  | ¢ 245446 | C4011870-7010102-7 |
| R800 | -07570019 | 3 3 | 2 |  | 27867 27167 | c5-1/4-T0-221aof |
| ${ }_{863}{ }_{8} 8$ | -9757-0280 | 1 | 1 |  | 20596 |  |
| ${ }_{\text {R68 }}$ |  | ! | 1 |  | ${ }^{201124}$ | ${ }_{\text {cidio25 }}$ |
| R101 R 102 | - 006331025 | : |  |  | - 012121 |  |
| R104 | 0663-1025 | : |  |  | 01121 | C81025 |
| ${ }^{810 \%}$ | - 066331.1025 |  |  | Remsior | -1121 | cifice |
|  | ( $\begin{gathered}0633-1025 \\ 0683-1025\end{gathered}$ | : |  | (embitor | - 01121 |  |
| ${ }^{\mathrm{R}} 110$ | 0083-1025 |  |  |  | 0121 | ${ }^{\text {cha }} 1025$ |
| R119 | ${ }^{0} 0633313915$ | : |  |  | ${ }^{012121}$ |  |
|  |  | : |  |  | 退0121 |  |
|  | $0683-1025$ $0683-3915$ <br> $0.063=1325$ <br> $0633-1025$ | : |  |  <br>  aistor 1k 5x. 25W FC TC0-400/+600 | $\begin{aligned} & 012121 \\ & 0121 \\ & 0 \\ & 0121 \\ & 0\end{aligned}$ |  |
| Rp64 | 181000279 | 5 | , | NETWORK-REs $10-\mathrm{PIN}$-sip : 1 -PiN-speg | ${ }^{11236}$ | 750-1010R4.7 |
| ${ }_{\text {RPbob }}^{\text {RPb }}$ |  | 5 |  |  | ${ }_{11236}^{1236}$ |  |
| RP6\% | ${ }^{181000270}$ | 5 |  |  | 11236 | ${ }_{\text {150-1010R4; \% }}$ |
| ${ }_{\text {Tp\% }}$ | $1251-5300$ 125159380 | 3 |  |  | 28480 | 125125380 $1251-5380$ |
| $\mathrm{u}_{1}$ |  | : | 12 |  | 01205 |  |
| U3 |  | \% |  | ic | 01295 | onvts |
| U5 |  | $\stackrel{6}{2}$ | , |  | (1295 |  |
| Y6 | ${ }^{18280-1197} \begin{aligned} & 1820 \\ & 1\end{aligned}$ | : |  |  | O1295 | 8NT42000 |
| U8 | ( | 1 | $\frac{2}{2}$ |  | (121295 | coly |
| U10 | ${ }_{1820-1470}$ | 1 |  | IC MUXR/DATA-BEL THL LS 2-To-1-LINE OUAD | 01295 | -974Latsm |
| $\mathrm{Y}_{1}$ | 1882-1197 | , |  |  | 01295 | 8NT4L800 ${ }^{\text {and }}$ |
| U13 | ${ }_{1820} 18130$ | ! |  |  | 01295 | anvitazism |
| U14 |  | : | 1 |  | -04713 | Mciadestes |
| ${ }^{4}$ |  | ! | 3 |  |  | cal 14586 |
| Wid |  | ? |  |  | ( |  |
| U19 | ${ }^{18200-02224}$ | : | 3 |  | 27044 | LH0002CM |
| 4101 0102 0 |  |  | 2 |  | 01295 |  |
| - 1102 |  | : | 2 | It | (18324 |  |
| U104 | - $\begin{aligned} & 182001730 \\ & 1820-1441\end{aligned}$ | : | 4 |  | ( 01285 | - |

Table 8-3-2. Replaceable Parts (Cont'd).


Table 8-3-2. Replaceable Parts (Cont'd)

| Reference Designation | HP Part Number | $\begin{aligned} & \mathrm{C} \\ & \mathrm{D} \end{aligned}$ | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 45 | 03582-66505 | 3 | 1 | PC ASBEMBLY, DIGITAL FILTER | 28480 | 03582-64505 |
| $\mathrm{C}_{1}$ C 2 | $0100-2208$ $0160-2208$ | 4 | 2 | CAPACITOR-FXD 330PF *O5x 300VDC MICA CAPACITOR-FXD 330PF +E5X 300VDC MICA | $\begin{aligned} & 28480 \\ & 28980 \end{aligned}$ | $0160=2208$ |
| C1 $C 3$ | 01600288 010004571 | 8 |  | CAPACITOR-FXD S 1 UF +80-20X SOVDC CER | 28480 | 0160-4571 |
| C4 | 0160-4571 | 8 |  | CAPACITOR-FXD . $14 F+80-20 X$ SOVDE CER | 28480 | 0160-4571 |
| 65 | 0160.4571 | 8 |  | CAPACITOR-FXD , 1 UF +80-20x SOVDC CER | 28480 | 0160-4571 |
| $\mathrm{C}_{6}$ | 0160-4571 | 8 |  | CAPACITOR-FXD . $14 F$-80-20X 50VOC CER | 28480 | 0160-4571 |
| ${ }^{\text {c }}$ | 0160-4571 | 8 |  | CAPACIYOR-FXD . $1 \mathrm{UF}+80-20 X$ SOVDC CER | 28480 | 0160 -4571 |
| ${ }^{6} 8$ | 0160-4571 | 8 |  | CAPACITOR-FXD .1UF +80-20X SOVDC CER | 28480 | $0160-4571$ |
| ${ }_{c}{ }^{\text {c }}$ | 01600-4571 | 8 |  | CAPACIPOR-FXD. $14 F$ +80-20x SOVOC CER | 28480 | 0160 -4571 |
| ${ }^{6} 10$ | 016004571 | 8 |  | CAPACITORAFXD . 1 UF -80-20x 50VDC CER | 28480 | 0160 -4571 |
| ${ }_{6}{ }_{11}$ | 0160-4571 | 8 |  | CAPACITOR-FXD . 1 UF +80-20X SOVDC CER | 28480 | $0160-4571$ |
| ${ }^{6} 12$ | 0160-4571 | 8 |  | CAPACIPOR-FXO .1UF +80-20X SOVDC CER | 28480 | 0160-4571 |
| C13 C14 | 010004571 $0160-4571$ | 8 |  | CAPACIPDR-FXD 1 l CAPACITOR | 28480 28480 | 0160.4571 01600.4571 |
| C15 | 0160.4571 | 8 |  | CAPACITOR-FXD IUF 80020 S SOVOC CER | 28480 | 0160-4571 |
| ${ }_{C} 16$ | 0160-4571 | 8 |  | CAPACITDR-FXD . 1 UF -80-20X SOVOC CER | 28480 | 0160-4571 |
| ${ }_{6} 17$ | 0160-4571 | 8 |  | CAPACIPOR-FXD , 1 4 F +80-20X SOVOC CER | 28480 | 016004571 |
| $C 18$ $C 19$ | $0160-4571$ $0160-4571$ | 8 |  | CAPACITOR-FXD I I FF | 28480 | 0160.4571 |
| C19 C20 | $0160-4571$ $0160-4571$ | 8 |  |  | 28480 28480 | $0160-4571$ $0160-4571$ |
| C21 | 0160-4571 | 8 |  | CAPACIPDR-FXD 1 IUF $80-20 x$ 50VDC CER | 28480 | 0160-4571 |
| C22 | 0180-0229 | 7 |  | CAPACITOR $\triangle$ PD 3 3UF $+=10 \mathrm{X}$ 10VDC TA | 56289 | $1500336 \times 901082$ |
| ${ }^{2} 23$ | 018000116 | 1 |  | CAPACITORAFXD 6. BUFt-10X 3SVOC TA | 50289 | $1500885 \times 03582$ |
| ${ }^{6} 24$ | 0180-0229 | 7 |  | CAPACITOR-FXD 33UF+-10X 10 VOC TA | 56289 | $1500336 \times 901082$ |
| C25 | 0160-4571 | 8 |  | CAPACITOROFXD GIUF +80-20x SOVOC CER | 28480 | 0160-4571 |
| c26 | 0180-0116 | 1 |  | CAPACITOROFXD 6, 8UFP-10\% 35VOC TA | 56289 | $1500685 \times 903582$ |
| C27 | 0180-0116 | 1 |  | CAPACITOR-FXD 6.8UF\$-10x 35VDC TA | 56289 | $1500685 \times 903582$ |
| C28 | 0160-4571 | 8 |  | CAPACITOR-FXO. 1 UF -80-20X SOVDC CER | 28480 | 0160-4571 |
| 629 | 0160-4571 | 8 |  | CAPACITOR-FXD : 1 UF \$80-20X SOVDC CER | 28480 | 0160-4571 |
| C30 | 0160-4571 | 8 |  | CAPACITOR-FXD IIUF $800-20 x 50 \mathrm{VDC} \mathrm{CER}$ | 28480 | 0160 -4571 |
| ${ }^{C} 31$ | 0160-0571 | 8 |  | CAPACITORAFXD .1UF -80-20X SOVDC CER | 28480 | 0160.4571 |
| C32 | 0160-4571 | 8 |  | CAPACITOR-FXD . $14 F$ \$80-20X SOVDC CER | 28480 | 0160.4571 |
| C33 | 0160-4571 | 8 |  | CAPACITOROFXD 1 UF 80-20X 50VOC CER | 28480 | 0160.4571 |
| C34 | 0160-4571 | 8 |  | CAPACITOR-FXD .1UF +80-20x 50VDC CER | 28480 | 0160-4571 |
| CR1 | 1902-3030 | 7 |  | OICOE-2NR 3.OIV 5X 00-7 PDE.aW TCE=.067x | 28480 | 1902-3030 |
| R1 | 0683-1025 | 9 | 53 | RESISTOR 1K 5X . 25 W FC TCE $5000 / 4000$ | 01121 | CB1025 |
| $\mathrm{R}_{2}$ | 0683-1025 | $\stackrel{0}{9}$ |  | RESISTOR 1K 5x. 25 W FC TCEa400/4000 | 01121 | CB1025 |
| R3 | 0683-1005 | 5 |  | RESISTOR 10 5x. 25W FC TCE=400/\$500 | 01121 | C81005 |
| R4 | 0683-1005 | 5 |  |  | 01121 | C81005 |
| R5 | 0683-1025 | 9 |  | RESISTOR iK 5x , 25W FC TCE=400/4600 | 01121 | CB1025 |
| R6 R 7 | $0683-1025$ $0683-2715$ | 6 |  |  | 01121 01121 |  |
| R9 | $0683-2715$ $0683-2715$ | 6 |  | RESISTOR 210 5x, 25 W FC PC=-400/*600 RESISTOR 270 SX | 01121 01121 | C82715 c82715 |
| Ro | -683-2415 | 3 | 3 | RESISYOR 240 SX . 25 w FC YCE-400/+600 | 01121 | c82415 |
| R10 | 0683-2415 | 3 |  | RESISTOR 240 5x, 25 W FE TCE-400/4600 | 01121 | ce24is |
| R14 <br> $R_{15}$ <br> 15 | 0683-5625 | 3 | 3 | RESISTOR 5.6K 5X . 25 W FC TCE-400/4700 | 01121 |  |
| R15 R17 | $0683-1225$ $0683-1035$ | 1 | 1 |  | 01121 | C81225 681035 |
| R18 | $0683-1135$ $0683-1035$ | 1 |  | RESISTOR 10K 5x, 25 W WC YCE=400/\$700 | 01121 | c81035 c81035 |
| R19 | 0683-1025 | ${ }^{\circ}$ |  | RESISTOR iK 5x. 25 W FE TCE-400/+600 | 01121 | csi025 |
| $\mathrm{R}_{20}$ | 0683 -1025 | 9 |  | RESISTOR 1K 5x, 25w FE TCE-400/4600 | 01121 | CB1025 |
| R21 R22 | $0683-1005$ $0683-1005$ | 5 |  |  | 01121 01121 | cel 1005 celo |
| RP11 | 181000030 $1810-0030$ | 6 | 3 |  | 28480 28480 | $1810-0030$ $1810-0030$ |
| RPI? | 181000030 | 6 |  |  | 28480 28480 | 181000030 18100030 |
| RP13 | 181000030 | 6 |  | NETWORK-RES S-PIN-SIP .125-PIN-SPCG | 28480 | 1810-0030 |
| 41 | $1520-2103$ | , | $?$ |  |  |  |
| 42 | 1820-0681 | 4 | 3 | IC GATE TTL S NAND QUAD E-INP | 01295 | 8N74800N |
| 43 | 1820-1112 | 8 |  | IC PF PTG L8 O-TYPE POSEEOGE-TRIG | 01295 | 6N746374N |
| 44 45 | $1820-1197$ 1820.1112 | 9 | 18 | IC GATE TTL LS NAND QUAD 2-INP IC FFTTL LS O-FYPE POSOEDGETTRIG | 01295 01295 | $8 N 746800 \mathrm{~N}$ 8N746874N |
| US | 1820-1112 | 8 |  | IC FF TTL LS DeTYPE POS-EDGE-TRIG | 01295 | 8N746874N |
| $U_{6}$ | 1820-2061 | 8 | 4 |  | 28480 | 1820-2061 |
| 47 | 182002061 | 8 |  |  | 28480 | 1820-2061 |
| 48 | 1820-1201 | 6 |  | If GATE TTL LS AND QUAO 2-INP | 01295 | 8N74L808N |
| 49 | 1820-1217 | 4 | 1 | If MUXRIDATAESEL TTL LS Sotool-line | 01295 | 8 NTHLSISIN |
| $\mathrm{U}_{10}$ | 1820-1199 | 1 |  | IC INY TTL LS HEX I-INP | 01295 | 8N74L804N |
| 411 412 | $\begin{aligned} & 1820-1432 \\ & 1820-1197 \end{aligned}$ | 5 | 3 | IE CNTR TYL Ls BIN SYNCHRO POS-EDCE-TRIG | 01295 01295 | $8 N 74 L 8163 N$ $8 N 74800 \mathrm{~N}$ |
| 413 | 1820-1197 | 9 |  | IC gate til ls nand ouad ioinf | 01295 | SN74L800N |
| 414 | 1820-2061 | 8 |  |  | 28480 | 1820-2001 |
| U15 | 1820-2061 | 8 |  |  | 28480 | 1820-2061 |

Table 8-3-2. Replaceable Parts (Cont'd).


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## PROCESSOR

## SERVICE GROUP 4

### 8.4.1. INTRODUCTION.

8-4-2. The Processor Service Group consists of the Processor, Random Access Memory (RAM) and Read Only Memory (ROM) Assemblies. Processor instructions are contained in the ROM while data storage is in the RAM. Since this group is so essential to instrument operation, faults can cause a wide variety of problems. On the other hand, several internal self tests are provided to speed troubleshooting.

## 8-4-3. BUS STRUCTURE.

8-4-4. It is useful to think of processor functions in two groups; I/O Bus and IDA Bus. The I/O Bus communicates data and processor instructions to all peripheral assemblies, except the ROM and RAM. These would include operations such as reading the front panel switch registers or passing data from the digital filters to the RAM. The IDA Bus (instruction, data and address) communicates instructions and addresses to and from the ROM and data and addresses to and from the RAM. Notice that the Troubleshooting Diagrams are divided along these lines.

## 8-4-5. INTERNAL TESTS.

8-4-6. There are several internal tests that can be used to check circuitry in this group and they can again be divided along the lines given above. For the I/O Bus section, an I/O Bus Test is provided. This test can selectively enable peripheral bus buffers and also puts readable signatures on the I/O Bus lines. For the IDA Bus portion, a basic Processor Test Loop is provided. This exercises the memory control circuits and puts readable signatures on the IDA Bus. In addition to the basic test loop, there are "primitive" ROM and RAM tests which can do overall tests on the memory assemblies in addition to providing readable signatures.

## 8-4.7. TROUBLESHOOTING STRATEGY.

8-4-8. As previously stated, a malfunction in this group can cause a wide variety of problems. However, it is useful to divide these into two general groups:
a. Instrument not responding to front panel or "hung-up".
b. All other problems with a running instrument.

8-4-9. A non-responding mode is caused usually by a peripheral line being in the wrong state and holding up program execution. Once stopped in program execution, the processor will not "get around to" reading the front panel and will thus not respond to changes in front panel settings.

## NOTE

When a diagnostic message appears on the screen, the instrument will not respond to changes in front panel settings until the diagnostic is cleared. For example, pressing COHERENCE will cause the message "USE BOTH MODE RMS AVERAGE FOR COHERENCE" unless alredy in that mode. The instrument will not respond unless BOTH mode RMS AVERAGE is selected or COHERENCE is released.

8-4-10. The following procedure provides a quick check as to whether the processor is running:
a. Release the Amplitude and Phase Display pushbuttons and the REPETITIVE pushbutton.
b. Moving the INPUT MODE slide switch from A or B to BOTH should cause the display section LED to move from SINGLE CHAN to BOTH CHAN.
c. If the LED moves, the processor is running.

## NOTE

## It should be emphasized that a bad processor is not usually the cause of non-response.

8-4-11. To isolate the cause of non-response, follow the procedure below for each of the A2,3,4 and 5 assemblies. Power should be turned off before a board is removed or replaced.
a. Turn the instrument off and remove a board (A2,3,4 or 5).
b. Turn the instrument on and check for a running processor using the procedure in Paragraph 8-4-10.
c. If the processor is now running, the board pulled is the cause. Check the associated control lines to the processor.
d. If the processor is not running, repeat the procedure for the next board.

8-4-12. If this strategy does not result in a running processor, the problem is probably with the processor or one of the memory boards. Refer to information in Using The Internal Tests to help find the problem.

8-4-13. Other problems with the instrument can be found using the internal test information below and specific troubleshooting information given in the rest of this group.

## 8.4-14. USING THE INTERNAL TESTS.

8-4-15. As stated earlier, the internal tests consist of an I/O Bus test and basic processor, RAM and ROM tests. Information on the I/O Bus test is given in the I/O Bus Section Troubleshooting Diagram. The other tests are described in the following sections.

8-4-16. The Basic Processor Test Loop tests the memory control circuits and passing this test indicates that this section of the processor is at least basically working. If the problem is a non-responding instrument, all the circuit boards except A7, 9 and 10 can be pulled out of the card nest to more or less "start from scratch"' in troubleshooting. If the processor passes this test, the ROM (A6) board can be added and its basic test run. The process can then be repeated with the RAM board. If the instrument passes the basic processor test loop, it's a good idea to check the IDA Bus signatures before continuing. These signatures are given on the next page and the IDA Bus Section Troubleshooting Diagram. Follow this procedure to enter the basic processor test loop:
a. Move jumper A7 J2 to the 'test'' position.
b. Set up the 5004 Signature Analyzer as follows:

| GND: | J1(1) |  |
| :--- | :--- | :--- |
| CLK: | J1(3) | - |
| START: | J1(4) | - |
| STOP: | J1(5) |  |

c. With the probe to +5 and the probe reset button pressed and released, the signature should be 9PA2. Note, it may be necessary to press RESET. If this is correct, the IDA Bus signatures below can be checked.
d. If the +5 signature is incorrect, troubleshooting information is given on the IDA Bus Section Troubleshooting Diagram. Access to these signatures is from the top, backside of the A7 assembly.


Table 8-4.1. IDA Bus Signatures.

| IDA Bus Line |  | Xa7a |  |  |
| :---: | :---: | :---: | :---: | :---: |
| 0 | (A20) | $14 \mathrm{F3}$ | 1 | F666 |
| 1 | (A19) | 1882 | 2 | $7 \mathrm{CA8}$ |
| 2 | (A18) | POA8 | 3 | 8P75 |
| 3 | (A17) | 882A | 4 | 775H |
| 4 | (A16) | 775 H | 5 | 8824 |
| 5 | (A15) | 8 P 75 | 6 | POA8 |
| 6 | (A14) | $7 \mathrm{CA8}$ | 7 | 1882 |
| 7 | (A13) | F666 | 8 | 14 F 3 |
| 8 | (A5) | 3343 | A | 9PA2 |
| 9 | (A6) | 9745 | B | P156 |
| 10 | (A) ) | 9160 | C | AA5F |
| 11 | (A8) | 5586 | D | A4 12 |
| 12 | (A9) | A412 | F | 5586 |
| 13 | (A10) | AA5F | H | 9160 |
| 14 | (A11) | P156 | $J$ | 97 A 5 |
| 15 | (A12) | 9PA2 | L | 3343 |

BACK SIDE OF A7 (NOT SHOWN)

8-4-17. If satisfactory results are obtained from the processor test loop checks, turn off the instrument and install the ROM (A6) board. To enter the primitive ROM test:
a. Move jumper A7 J2 to "run'" and turn the instrument on.
b. Short A7 J4 and press RESET (front panel). A754 must remain shorted.
c. Set up the 5004 A as in the previous section.
d. The +5 signature should be OH 62 . Note that this signature will take about 10 seconds
to come up. If this is incorrect, check the IDA Bus signatures in Table 8-4-1 (J2 to test and J4 unshorted) and continue with ROM troubleshooting procedures given later in this section.
e. If the signature is correct, continue with the primitive RAM test.

8-4-18. The primitive RAM test does not completely check the RAM, but provides stable signatures for component level troubleshooting given later in this section. At this point, having passed the basic processor and ROM tests, the front panel self-tests should run; and included in these is a very complete RAM test. Details are given later in this section. To check the +5 signature here, install the RAM board and remove the jumper from A7 J4. For the same 5004 A setup as above, the +5 signature should be 89 FP , which takes about ten seconds to come up. Note that the tests must be done in the order given. That is, with jumper J2 to run, shorting J4 enters the ROM test mode. Unshorting J4, after pressing RESET, enters the RAM test mode.

## 8-4-19. PROCESSOR TROUBLESHOOTING.

8-4-20. Processor troubleshooting information is given on the following two Troubleshooting Diagrams. In general, it is difficult to say that one particular section of the assembly is causing a particular problem. In these cases, it is most appropriate to do all the tests given on the diagrams. An exception would be if the problem is with a specific peripheral. In this instance, the I/O select line associated with the peripheral can be checked using the I/O Bus test. This information is given on the I/O Bus Section diagram.

## general troubleshooting.

a. Check The Power Supplies. First check the power supply LED's for a "green" condition, then make sure the foliowing voltages are getting to the board.

1.     + 12: should be 12.01-12.37 VDC at top of A7 C18.
2.     - 5: should be -5.5 to -4.5 VDC at right side of A 7 C 22 . If not present, check or -18 VDC on the can of U24.
3. +7 : should be $+7(+0.15,-0.07)$ at the top of C21.
4.     + 5: should be $+5(+0.1,-0.05)$ at the top of C14.
b. Clock. Check that $\emptyset_{1}$ (TP1) and $\emptyset_{2}$ (TP2) clocks have high and low levels $>11 \mathrm{~V}$ and $<1 \mathrm{~V}$ and cross at less than 1 V .

## INTRODUCTIOM.

This section of the Processor Assembly handles communications with the ROM (A6) and RAM (A8) memory assemblies. Instructions, data and memory addresses are sent over the "IDA" Bus.

A memory cycle begins with STM (TP3) going low. The RAM/ROM Select circuit determines whether the communication will be with the ROM, RAM or an internal register. An internal register operation is indicated by a high Register Access Line (RAL). The output of the select circuit will be a Start ROM or Start RAM (STROM or STRAM).

A STROM or STRAM will start the Memory Control circuit through its count, as long as Memory Busy $\overline{M E B}$ is high. This line hoids off the memory cycle if the RAM assembly is in the middle of a refresh cycle. The purpose of the control circuit is to allow time for data to become valid on the memory board and to pull MBE Iow (Memory Buffer Enable). This enables memory data onto the IDA Bus.
thoubleshooting.
The basic processor test loop is used for troubleshooting this portion of the assembly. To enter this test:

a. Move jumper J2 to the test position.
b. Set up the 5004A Signature Analyzer as follows:

| GND: | $J 1(1)$ |
| :--- | :--- |
| CLK: | $J 1(3) \_$ |
| START: | $J 1(4) \_$ |
| STOP: | $J 1(5) \_$ |

## nOTE

Pin 1 is on the left when facing the board.
c. The +5 signature should be 9PA2. If this is correct, the memory control circuit is basically working. If the signature is incorrect, use the waveforms given to troubleshoot the RAM/ROM Select, Memory Control Circuits, processor clocks and initialization circuits.
d. Check the IDA bus signatures as given.

MOTE
+5 signature must be correct.

| IDA Bus Signatures. |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| IDA Bus Line | XA7A |  |  |  |
| 0 | (A20) | 14F3 | 1 | F666 |
| 1 | A19) | 1882 | 2 | 7CA8 |
| 2 | (A18) | POA8 | 3 | 8P75 |
| 3 | (A17) | 882A | 4 | 775H |
| 4 | (A16) | 775H | 5 | 882A |
| 5 | (A15) | 8P75 | 6 | POA8 |
| 6 | (A14) | 7CA8 | 7 | 1882 |
| 7 | (A13) | F666 | 8 | 14F3 |
| 8 | (A5 ) | 3343 | A | 9PA2 |
| 9 | (A6 ) | $97 A 5$ | B | P156 |
| 10 | (A7 ) | 9160 | C | AA5F |
| 11 | (A8 ) | 5586 | D | A412 |
| 12 | (A9 ) | A412 | F | 5586 |
| 13 | (A10) | AA5F | H | 9160 |
| 14 | (A11) | P156 | J | $97 A 5$ |
| 15 | (A12) | 9PA2 | L | 3343 |




## IMTRODUCTION.

This portion of the processor assembly handles I/O communications with all the other boards in the instrument, except the ROM and RAM, which work over the IDA Bus.

The other assemblies are connected to the I/O Bus through tri-state buffers that are enabled by the OS and IS lines 0-15. The I/O Bus test can be used to selectively enable these lines and also to put readable signatures on the I/O Bus lines. There are additional control lines (e.g. (RH) which provide asynchronous timing for the instrument.

## I/O BUS TEST.

This test is very powerful for troubleshooting this part of the processor assembly. It can selectively enable the I/O Bus control lines OS 0-15 and IS 0-15. While this test is running, the I/O Bus lines, and IC1 and IC2 will have stable signatures for troubleshooting. To get into this test mode:

1. Enter the front panel self-test mode by pressing RESET while holding in average RESTART. When RESTART is released, the front panel switch test (Test 0 ) will come up.
2. Short A7 J4. This must be done only after step 1. Unless the instrument is in the front panel self-test mode, shorting J 4 will initiate the primitive ROM self-test. Pressing RESET during the bus test will stop the test and steps one and two must be repeated.
3. Select average number 256 and press RESTART. This should get you the l/O Bus test. Pressing RESTART will allow you to select the desired test. Note that the I/O enable lines are decimal numbers while the test numbers are octal. Thus, $0-7$ will correspond, while I/O enable lines numbered 8 and higher will use the test number 2 higher. That is, to enable OS13, test 15 should be selected.

NOTE
1/O Test 14 enables the $1 / O$ lines to the display section and the display will be unstable.


## TROUBLESHOOTING

fthe problem is a non-running processor, check the I/O control lines first. These are checked with the instrument in normal operating mode and $0-25 \mathrm{kHz}$. For specific problems wit peripherals, check the appropriate I/O Bus Select Line using the I/O Bus Test. For general prolems, also check the I/O Bus signatures using the I/O Bus Test.

## I/O CONTROL LINES. (Use logic probe and 0.25 kHz frequency span.)

IPH Interrupt Priority High. Should go low once per time record in response to DMAR (DMA Request). U13(6)
$\overline{\text { PL }} \quad$ Interrupt Priority Low. Will pulse low once per time record and put out a tring of pulses when the RPG (ADJUST) is turned in SET START or SET string of pulses wh
CENTER. U13(3).

FLG Flag line from HP-IB. Should pulse low during manual operation and stay high during the "blinking light test" (see HP-IB Service Section). U22(17).
STS Status line from HP-IB. Should stay high during manual operation and pulse low during the blinking light test. U22(9).
$\overline{\mathrm{C}} 1$ Control Line 1. To Digital Filter, HP-IB Interface and Local Oscillator Assemblies. Check with I/O Bus signatures. U22(15).
$\overline{\text { C2 }}$ Control Line 2. To Digital Filter and HP-IB Interface Assemblies. Check with I/O Bus signatures. U22(13).
$\overline{\mathrm{RL}} \quad$ Interrupt Request Low. From RPG (ADJUST). Should pulse low when the RPG is turned in SET START or SET CENTER modes. U22(3).
$\overline{\text { IRH }} \quad$ Interrupt Request High. From Digital Filters. Should pulse low once per time record. U22(5).

DMAR Direct Memory Access Request. Tells processor that digital filter data is ready and needs DMA channel to RAM. Should go low once per time record. U22(7).

## NOTE

A time record is one measurement cycle; the data loading light will flash once per time record for spans greater than 500 Hz .

## I/O BUS SIGNATURES.

1. Enter the front panel self-test mode. (Press RESET while holding in RESTART)
2. Short jumper A7 J4 and select I/O Bus Test \#000005. (Jumper remains shorted thru test.)
3. Set up the 5004A Signature Analyzer as follows: (Refer to component locator.)
GND
START/STOP
+5 signature
$\overline{\mathrm{JOSB}} \mathrm{J} 20(18)$
C1(TP7) -
7FC2
4. If RESET is pushed in this test mode, the test will stop and steps 1 and 2 will have to be repeated. Note that J4 must be unshorted for step 1.
5. Check the following signatures:

| 110 | Location | Signature |
| :---: | :---: | :---: |
| $\overline{\text { IC1 }}$ | U22(15) | 8552 |
| 0 | RP1 (8) | A511 |
| 1 | (7) | 999H |
| 2 | (6) | 96CP or 5455 |
| 3 | (5) | 3PP7 |
| 4 | (4) | 9P15 |
| 5 | (3) | U629 |
| 6 | (2) | 855F |
| 7 | (1) | 8AA5 |
| 8 | RP2(8) | C1PP |
| 9 | (7) | 4H6H |
| 10 | (6) | $42 \mathrm{U7}$ |
| 11 | (5) | F111 |
| 12 | (4) | P1P8 |
| 13 | (3) | 69H6 |
| 14 | (2) | FCH9 |
| 15 | (1) | 21C1 |



## 5. Check the following signatures

| $1 / 0$ | Location | Signature |
| :---: | :---: | :---: |
| $\overline{\text { IC1 }}$ | U22(15) | 8552 |
| 0 | RP1 (8) | A511 |
| 1. | (7) | 999H |
| 2 | (6) | 96CP or 5455 |
| 3 | (5) | 3PP7 |
| 4 | (4) | 9P15 |
| 5 | (3) | U629 |
| 6 | (2) | 855F |
| 7 | (1) | 8AA5 |
| 8 | RP2(8) | C1PP |
| 9 | (7) | $4 \mathrm{H6H}$ |
| 10 | (6) | $42 \mathrm{U7}$ |
| 11 | (5) | F111 |
| 12 | (4) | P1P8 |
| 13 | (3) | 69H6 |
| 14 | (2) | FCH9 |
| 15 | (1) | 21C1 |



| $1 \mid 0$ Bus Seleet Lines |  |  |  |
| :---: | :---: | :---: | :---: |
| Line | Location | 1/0 Bus Test \# | Description |
| $\overline{050}$ | U20(1) | 00 | Trigger Control. Clocks programming data into A5 trigger circuit (U3) once per time record. |
| $\overline{053}$ | (4) | 03 | Front Panel LED's. |
| OS6 | (7) | 06 | HP-IB. Enables data onto A2 D/I bus from I/O bus. |
| ठS8 | (9) | 10 | Input Programming. Latches Attenuator/Gain and PRN data into A4 U129. |
| $\overline{089}$ | (10) | 11 | X-Y Recorder Data Latch. |
| $\overline{0811}$ | (13) | 13 | Cal Signal/PRN Programming. Latches data on A3. Should pulse low when sensitivity is changed. |
| $\overline{\text { OS12 }}$ | (14) | 14 | Graphics Sweep Control. Latches data into A9U9 for \# of lines of graphics to display. |
| $\overline{\mathrm{OS} 13}$ | (15) | 15 | Local Oscillator Frequency control. Latches data into A4 U101 and U104. |
| $\overline{\text { OS14 }}$ | (16) | 16 | Digital Filter Programming. Latches data into A5 U26 and U28. |
| $\overline{0 S 15}$ | (17) | 17 | Enables DMAR. |
| IS0 | U19(1) | 00 | Front Panel Switch Register $\emptyset$. Enables data onto I/O bus from A11 U1 and U2. (Corresponds to condition code $\varnothing$ in self-test.) |
| $\overline{\text { S1 }}$ | (2) | 01 | FP Switch Register 1; A11 U7 and U8. |
| $\overline{\text { 152 }}$ | (3) | 02 | FP Switch Register 2; A11 U3 and U4. |
| $\overline{\text { S3 }}$ | (4) | 03 | FP Switch Register 3; A11 U9 and U10. |
| $\overline{154}$ | (5) | 04 | FP Switch Register 4; A11 U5 and U6. |
| $\overline{\text { S5 }}$ | (6) | 05 | RPG Interrupt. Should pulse low when RPG is turned in SET START or CENTER. |
| IS6 | (7) | 06 | HP-IB. Latches data from D/I to I/O bus. |
| $\overline{158}$ | (9) | 10 | L.O. Phase. Enables phase data onto I/O bus from A4 U134 and U135. |
| $\overline{\text { IS11 }}$ | (13) | 13 | Phase Count. Enables phase count data from A3 U5 and U6 onto I/O bus. |
| $\overline{\text { S12 }}$ | (14) | 14 | Marker Register. Enables additional count from A9 U8. |
| $\overline{1513}$ | (15) | 15 | Overload. Enables OVLD data from A5 (not for OVLD lites). |
| $\overline{1515}$ | (17) | 17 | Enables digital filter data onto I/O bus. |



CONNECTOR A (IDA SIGNATURES)




## 8-4-21. TROUBLESHOOTING THE ROM ASSEMBLY.

## 8-4-22. Introduction.

8-4-23. This assembly provides programming for the A7 processor. The proper address comes over the IDA Bus from the processor and the correct program code is returned. Note that, unlike the RAM, the ROM is completely static; changing the input address changes the output.

8-4-24. Selection of the proper ROM chip is accomplished by the higher order IDA address bits 11-14. Bits $12-14$ go through a 3 to 8 decoder (U25) that selects two pairs of IC's. Note that one pair provides a high order byte and a low order byte to make up the sixteen bit instruction word. Bit 11 selects which pair and also whether U1 and U2 are enabled.

## 8-4-25. Troubleshooting.

8-4-26. Signature analysis works quite well for troubleshooting this assembly, although a bus conflict problem requires use of an ocilloscope. The first thing to do is to try the front panel self-test. For some ROM failures, the test will point out the bad chip. For other problems, the self-test won't run. In this case, the processor test loop and the primitive ROM test will indicate problems on the board.

8-4-27. The procedure for using signature analysis consists of:
a. Checking address and chip select signatures.
b. Checking overall data output. This will usually indicate at least one bad line. Finding the cause of trouble for that line will probably also fix other bad lines, so go to the next step as soon as a bad line is found.
c. By starting and stopping the signature analyzer at various chip enables, it is possible to isolate signatures to a group of $4 ; 2$ high byte and 2 low byte. It is further possible to isolate signatures to one of the pairs thus enabling one to deduce which is the bad chip.

8-4-28. As an example of step $c$, one set of ROM signatures might be for chips U3, 4, 11 and 12. That is, the SA measurement cycle lasts through contributions from all four chips. This signature set also would include signatures for only U3 and 4. Thus, if the signatures for all four are incorrect but the signatures for U3 and 4 are correct, U11 or 12 must be bad.

8-4-29. A bus conflict can be a little trickier to find. This happens when the chip enable function is bad and the chip is talking to the bus constantly. This will make data on the bus always incorrect except when the bad chip is addressed. This is the key to troubleshooting this type of problem. Note that if the bad chip is one that can't have its signature isolated, signature analysis cannot find the problem. Looking at the bad line, there will be three visible levels when there is conflict: 1) when two chips are "fighting each other", 2) when they are both low and 3) when they are both high. When the bad chip only is addressed, the line will look OK.

## 8-4-30. Front Panel Self-Test.

8-4-31. To initiate the ROM self-test mode:
a. Enter the front panel self-test mode by pressing RESET while holding in average RESTART and then releasing RESTART. This should get the front panel switch test (\#0). If it doesn't, proceed with the troubleshooting given at the beginning of the service group.
b. Select average number 32 and press RESTART. This should get the ROM test, number 3.
c. The test will display "RU' for about 5 seconds and then display either OK or ER. For ER, condition codes 0-9 (see Section VIII for details) will display an error code.


High Byte Error (If Set To 1)

| ROM Address In <br> Condition Code | High Byte ROM <br> Ref. Desgn | Low Byte ROM <br> Ref. Desgn |
| :---: | :---: | :---: |
| 0000 | U2 | U1 |
| 0040 | U28 | U27 |
| 0100 | U4 | U3 |
| 0140 | U12 | U11 |
| 0200 | U6 | U5 |
| 0240 | U14 | U13 |
| 0300 | U8 | U7 |
| 0340 | U16 | U15 |
| 0400 | U10 | U9 |
| 0440 | U18 | U17 |

## 8-4-32. Signature Analysis Procedures.

8-4-33. To use the signature analysis chart effectively, perform Part 1 first. This will establish whether the addressing for the ROMs is correct. If the addressing circuits are working, go to Part 2 to check the overall data outputs at the buffer ICs. Proceed vertically down the chart until an incorrect signature is obtained which indicates a defective data line. Then proceed to the right horizontally and check the signature output from each ROM for that particular data line. Don't forget that each ROM and ROM pair require a different SA setup. Place the ROM board on extenders for troubleshooting and continue with Part 1.

## NOTE

ROMS were changed at roughly serial number 1809A01006 resulting in a new signature set which is given in this section. Some earlier instruments have been retrofitted to these new ROMS by replacing U1, U2, U3 and U4 with -hp- part number 1818-0957, 1818-0958, 1818-0959 and 1818-0961 respectively. Instruments with the ROM retrofit will also use the signatures given in this section. To identify which unit you have, access any front panel self test. The ROM datecode given in the upper right hand corner of the displays will be 017536 on old units, 020151 on new units.


Data for U5，6，and U13，14

## 郎a for 07,8 ，and U15．16

 Date code 020151
## ata for U9，10，and U17，18

 Date code 020151U9，10，\＆17， 18 U9 and 10 only

| Clk： | J2（3） | 工 | Clk： | J2（3） |
| :---: | :---: | :---: | :---: | :---: |
| Stop： | TP6 | $\checkmark$ | Stop： | TP2 |
| Start： | TP6 | L | Start： | TP6 |

Part 3：Data Test For Patch ROMS U1， 2 Datecode： 020151
Place A7 J2 to Tes
Setup：CIk：J2（3）ک
Stop：TP3 」
Start：TP3 L
+5 Signature $\quad \underline{105 U}$
note
U28 and 29 are not installed for this software．

## M．S．Byte <br> $\underset{\text { UG }}{\text { M．S．Byte }}$

| 7 | $74 U C$ | 7 | 7PP8 |
| :--- | :--- | :--- | :--- |
| 6 | F9FH | 6 | P656 |
| 5 | F39H | 5 | UAU6 |
| 4 | P68F | 4 | $10 F 6$ |
| 3 | $520 H$ | 3 | $5 F P H$ |
| 2 | A23U | 2 | APO1 |
| 1 | $973 F$ | 1 | P5F7 |
| 0 | $5 H 98$ | 0 | $42 F A$ |

L．S．Byte
U5 $\& 13$
L．S．Byte
U5

M．S．Byte
U8 \＆U16 $\quad$ M．S．Byte

| 943H | 7 | 7125 |
| :---: | :---: | :---: |
| HOH9 | 6 | FU53 |
| CUH5 | 5 | $374 U$ |
| HAF7 | 4 | $9 H 7 C$ |
| UCC1 | 3 | $36 H P$ |
| 2743 | 2 | A534 |
| 7681 | 1 | $868 U$ |
| 8PO1 | 0 | $68 H 2$ |

$\begin{array}{ll}\text { L．S．Byte } \\ 07 \& 15 & \text { L．S．Byte } \\ 07\end{array}$

| U709 | 7 | OUU8 |
| :--- | :--- | :--- |
| 5319 | 6 | 5UAC |
| OP4F | 5 | PH51 |
| 3700 | 4 | HH85 |
| H5U7 | 3 | $9 H 17$ |
| U82C | 2 | F516 |
| 3756 | 1 | H901 |
| PC92 | 0 | H76H |

## M．S．Byte M．S．Byte

| 7 | 331 H | 7 | $5 P P 3$ |
| :--- | :--- | :--- | :--- |
| 6 | 8766 | 6 | 462 U |
| 5 | 1684 | 5 | $7 \mathrm{CU7}$ |
| 4 | CC2O | 4 | P633 |
| 3 | PCO2 | 3 | 1 C7H |
| 2 | FAHA | 2 | 7 CO6 |
| 1 | 41 UA | 1 | FA12 |
| 0 | $88 H 7$ | 0 | F39C |

$\begin{array}{cc}\text { L．S．Byte } & \text { L．S．Byte } \\ \text { U9 \＆U17 } & \mathbf{U 9}\end{array}$

M．S．Byte
2

349
7H9C
504U
572H
8064
60A3
C78U
P769

L．S．Byte
U1
7F42

P296

049 U

AFH1

85 FO

90CB

30 C 6




Figure 8-4-4. A6 Read Only Memory.

## 8-4-34. TROUBLESHOOTING THE RAM ASSEMBLY.

8-4-35. Introduction.

8-4-36. RAM chips U1-U16 are dynamic and must be refreshed by the display circuits. The refresh address comes over the RAD Bus, while data readout of the RAM is sent to the display section over the XIDA Bus.

8-4-37. During normal operation, the processor usually reads and writes into RAM often enough to keep the chips refreshed. Thus, the board may appear to be working with a malfunctioning refresh circuit. The result of this condition would be a non-working display in normal operation, although the internal self-test would pass (switch on the A9 board).

## 8-4-38. Troubleshooting.

8-4-39. The troubleshooting procedure for this board is the same as for the ROM board:
a. Try the front panel self-test. This can identify the bad component, if the test will run. Remember that this is a 12 -minute test.
b. Go through the basic tests (processor test loop, primitive ROM and RAM tests). Details are given earlier in this section.
c. Isolate the problem to a component using signature analysis.

## 8-4-40. Front Panel Self-Test.

8-4-41. To get into the RAM self-test mode, do the following:
a. Initiate the front panel self-test mode by pressing RESET momentarily while holding in average RESTART. When RESTART is released, front panel self-test ( 0 ) should come up. If it does not, go to the basic tests at the beginning of the service group.
b. Select average number 64 and press RESTART. This should select RAM test, number 4. Note that this is a twelve-minute test that can only be terminated by pressing RESET, which will cause the instrument to leave the self-test mode.
c. The display will do some rather odd things during the test; this is normal.
d. At the end of the test, either OK or ER will be displayed. When ER is displayed, condition code 9 will display the accumulated error. Since each chip is responsible for one bit, it is easy to isolate the bad chip. For example, if condition code 9 reads 000010 , this would imply that the chip responsible for the 4th bit is bad. That is, the first three bits make up the least significant digit, the next three bits, the second digit, etc. As another example, condition code 000040 would imply that the chip for the 6th bit is bad.

Table 8-4-3 Error Codes for RAM Tests.

| Error Code |  | Bad Ram Chip |
| :---: | :---: | :---: |
| 000 | 001 | U1 |
| 000 | 002 | U2 |
| 000 | 004 | U3 |
| 000 | 010 | U4 |
| 000 | 020 | U5 |
| 000 | 040 | U6 |
| 000 | 100 | U7 |
| 000 | 200 | U8 |
| 000 | 400 | U9 |
| 001 | 000 | U10 |
| 002 | 000 | U11 |
| 004 | 000 | U12 |
| 010 | 000 | U13 |
| 020 | 000 | U14 |
| 040 | 000 | U15 |
| 100 | 000 | U16 |

## 8-4-42. Signature Analysis.

## 8-4-43. Address Lines.

Setup: 3582A: Short A7J4 and press RESET.
Unshort J4. This is the primitive RAM test.


For the address line signatures:

1. Each test point will have two valid signatures.
2. The read and write signatures will be the same and both should be checked.

| Address Line | IC \& Pin No. | Signatures <br> Read/Write |
| :---: | ---: | ---: |
| 11 | $\mathrm{U} 22(4)$ | U81P/U03F |
| 10 | $(12)$ | C811/5F08 |
| 9 | $(7)$ | $3771 / 9 \mathrm{CC} 8$ |
| 8 | $(9)$ | $\mathrm{HU} 4 \mathrm{U} / \mathrm{CP9P}$ |
| 7 | $\mathrm{U} 23(4)$ | $6064 / 3032$ |
| 6 | $(12)$ | $\mathrm{U} 253 / \mathrm{U} 929$ |
| 5 | $(7)$ | C177/62PU |
| 4 | $(9)$ | OF51/18A2 |
| 3 | $\mathrm{U} 24(4)$ | 66CA/335H |
| 2 | $(12)$ | $40 \mathrm{H} 1 / 2068$ |
| 1 | $(7)$ | A872/50P5 |
| 0 | $(9)$ | $\mathrm{UF} 4 \mathrm{C} / \mathrm{U} 897$ |

8-4-44. Data Line. (Same setup as Part A)
NOTE
Start/Stop trigger slopes change for read or write. For the IC's listed:

Start $\quad \longleftarrow$ Read | Write |
| :--- |
| Stop |
| Read | Write

The Write Signature is on Pin 6, Read on Pin 7.

| IC \# | Signature <br> Read/Write | IC \# | Signature <br> Read/Write | IC \# | Signature <br> Read/Write |
| :---: | ---: | :---: | :---: | :---: | :---: |
| 1 | U897/7P25 | 6 | 58CC/C5AA | 11 | AP04/58H5 |
| 2 | AFAU/5439 | 7 | UHU4/7F94 | 12 | UFF3/UFOU |
| 3 | $1034 / 24 C 5$ | 8 | $9819 / 34 P U$ | 13 | UF4C/UF4A |
| 4 | $99 A P / 3780$ | 9 | HC92/PUA7 | 14 | H657/A872 |
| 5 | $088 F / 8628$ | 10 | FHHF/9U65 | 15 | $2068 / 925 A$ |
|  |  |  |  | 16 | ICFO/335H |

8-4-45. Refresh.

| Setup: | Start/Stop | - TP5 | - |
| :--- | :--- | :--- | :--- |
| Clock | - TP4 | - |  |
|  | +5 Signature | -4596 |  |

## Address Signatures

|  |  |  |
| :---: | ---: | ---: |
| Address Line | IC \& Pin No. | Signature |
| AAD 11 | U22 (4) | 0000 |
| AAD 10 | $(12)$ | 4596 |
| AAD 9 | $(7)$ | 4596 |
| RAD/AAD 8 | $(9)$ | UPA2 |
| RAD/AAD 7 | U23 (4) | HFP7 |
| RAD/AAD 6 | $(12)$ | $41 F 7$ |
| RAD/AAD 5 | $(7)$ | FA11 |
| RAD/AAD 4 | $(9)$ | 8 C36 |
| RAD/AAD 3 | U24 (4) | CHU8 |
| RAD/AAD 2 | $(12)$ | $627 P$ |
| RAD/AAD 1 | $(7)$ | PC84 |
| RAD/AAD 0 | $(9)$ | $3 F 8 H$ |
| Write enable right (WER) | U1-8(12) | 4596 |
| Write enable left (WEL) | U9-16(12) | 4596 |

## NOTES

1. Verify chip enable signal (CE, U1-16(17). (Trigger on LFETCH XA8B(L).)
2. Address signatures do not depend on display mode.

8-4-46. Output Signatures (XIDA Bus).
Select display front panel self-test Number 1 (Ave \#8).

| XIDA Line | Connector Pin | Signature |
| :---: | :---: | :---: |
| 0 | XA8B(19) | 0950 |
| 1 | $(18)$ | F1H9 |
| 2 | $(17)$ | 3 H81 |
| 3 | $(16)$ | H2CO |
| 4 | $(15)$ | 981 A |
| 5 | $(14)$ | HUCP |
| 6 | $(13)$ | OA24 |
| 7 | $(12)$ | A3H2 |
| 8 | (S) | 6HHF |
| 9 | (R) | 22 P9 |

For lines 10-15, signatures depend on self-test number as shown.

| Test \# |  | 0 | 1 | 2* | 3 | 4 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| X1DA 10 | XA8B(Q) | AUPU | 68UF | H2UC | P6HA | P6HA |
| 11 | (P) | 6A36 | U85F | F815 | 2303 | U85F |
| 12 | (O) | H752 | 1041 | 2008 | 9P67 | 1041 |
| 13 | (N) | 6AOP | P428 | H461 | 3U77 | U864 |
| 14 | (M) | 0000 | 0000 | 66AP | 0000 | 0000 |
| 15 | (L) | 901F | UPA2 | UPA2 | 0000 | 0000 |

*For Test \#2, marker must be at left edge of screen (position 000000).


RAM BLOCK DIAGRAM








## 8-4-34. TROUBLESHOOTING THE 03582-66528 RAM ASSEMBLY

## 8-4-35. Introduction.

8-4-36. This procedure should be used for troubleshooting only the 03582-66528 RAM board; see the backdating section for the 03582-66508 RAM board. The 66528 board is a direct replacement for the 66508 board. The newer 66528 board uses four $2 \mathrm{~K} \times 8$ bit static RAMs instead of sixteen $4 \mathrm{~K} \times 1$ bit dynamic RAMs. The new board will still be referred to as the A8 assembly.

8-4-37. Although the RAMs do not need to be refreshed, the RAD (Refresh Address) Bus is used by the display (A9) to address the RAMs. Data is read out of the RAM and sent to the display section over the XIDA bus. The processor (A7) also uses the RAM through the IDA bus.

## 8-4-38. Troubleshooting.

8-4-39. The troubleshooting procedure for this board is the same as for the ROM board:
a. Try the front panel self-test. This can identify the bad component, if the test will run. Remember that this is a 12 minute test.
b. Go through the basic tests (processor test loop, primitive ROM and RAM tests) in sec 8-4-14.
c. Isolate the problem to a component using signature analysis.

## 8-4-40. Front Panel Self-Test.

8-4-41. To get into the RAM self-test mode, do the following:
a. Initiate the front panel self-test mode by pressing RESET momentarily while holding in average RESTART. When RESTART is released, front panel self-test ( 0 ) should come up. If it does not, go to the basic tests at the beginning of the service group.
b. Select average number 64 and press RESTART. This should select RAM test, number 4. Note that this is a 12 minute test that can only be terminated by pressing RESET, which will cause the instrument to leave the self-test mode.
c. The display will do some rather odd things during the test; this is normal.
d. At the end of the test, either OK or ER will be displayed. When ER is displayed, condition code 9 will display the accumulated error. Due to the memory structure, it is not possible to isolate an error to one chip. Rather, each error code indicates bad data from either of two chips.

TABLE 8-4-3 Error Codes for RAM Test

| Error code | Bad RAM chip(s) |
| :---: | :---: |
| 000001 | U7 or U8 |
| 000002 | U7 or U8 |
| 000004 | U7 or U8 |
| 000010 | U7 or U8 |
| 000020 | U7 or U8 |
| 000040 | U7 or U8 |
| 000100 | U7 or U8 |
| 000200 | U7 or U8 |
| 000400 | U9 or U10 |
| 001000 | U9 or U10 |
| 002000 | U9 or U10 |
| 004000 | U9 or U10 |
| 010000 | U9 or U10 |
| 020000 | U9 or U10 |
| 040000 | U9 or U10 |
| 100000 | U9 or U10 |

## 8-4-42. Signature Analysis.

8-4-43. Address Lines. This checks the RAM address lines from the A7 board, and A8 U1 through U6. The A9 board should be removed from the card cage. Only the A6, A7 and A8 boards are needed for this test.

3582A: Short A7J4 and press RESET
Unshort J4. This is the primitive RAM test.
Setup: 5004A:
Gnd: A8TP1
Clock: A8TP2
$\begin{array}{llll}\text { Start: } & \text { A8TP3 } \\ \text { Stop: } & \text { A8TP3 } & \text { (for read) } & \square\end{array}$

Note: Signatures should be checked in both the read and write setup. Each pin will alternate between two signatures during both the read and the write tests. The +5 signature should alternate between 04 HH and 826 P . The signature at A8TP4 should be the same, if not there is a problem with A8U18 curcuits.

Signatures

| Address Line | IC \& Pin No. | Read | 1 | Write |
| :---: | :---: | :---: | :---: | :---: |
| 11 | U6 ( 4) | U81P | 1 | U03F |
| 10 | (12) | C811 | 1 | 5F08 |
| 9 | ( 7) | 3771 | 1 | $9 \mathrm{CC8}$ |
| 8 | (9) | HU4U | 1 | CP9P |
| 7 | U2 (4) | 6064 | 1 | 3032 |
| 6 | (12) | U253 | 1 | U929 |
| 5 | ( 7) | C177 | 1 | 62PU |
| 4 | (9) | OF51 | 1 | 18A2 |
| 3 | U4 (4) | 66CA | , | 335H |
| 2 | (12) | 40 H 1 | , | 2068 |
| 1 | (7) | A872 | 1 | 50P5 |
| 0 | (9) | UF4C | 1 | U897 |

8-4-44. Data Lines During Write. This checks the data lines while data is input into RAM.
Setup: Same as 8-4-43 for write.

| IC \& Pin No. | Signatures Read/Write |
| :---: | :---: |
| U14 (17) | 335H / ICFO |
| (15) | 925A / 2068 |
| (13) | A872 / H657 |
| (11) | UF4A / UF4C |
| (9) | UFOU / UFF3 |
| ( 7) | 58H5 / APO4 |
| ( 5) | 9U65 / FHHF |
| ( 3 ) | PUA7 / HC92 |
| U11 (17) | 34PU / 9819 |
| (15) | 7F94 / UHU4 |
| (13) | C5AA / 58CC |
| (11) | 8628 / 088F |
| (9) | 3780 / 99AP |
| ( 7) | 24C5 / 1034 |
| ( 5) | 5439 / AFAU |
| ( 3) | 7P25 / U897 |

8-4-45. Data Lines During Read. This checks the data lines while data is read out of RAM.
Setup: Same as 8-4-43 for read.

| IC \& Pin No. | Signatures Read/Write |
| :---: | :---: |
| U14 (17) | $99 \mathrm{AP} / 3780$ |
| (15) | 24C5 / 1034 |
| (13) | AFAU / 5439 |
| (11) | 7P25 / U897 |
| ( 9) | 7P61 / U81P |
| ( 7) | 5F08 / 2F6A |
| ( 5) | 4 UC 2 / 9CC8 |
| ( 3) | HU4U / 6HF9 |
| U11 (17) | 1A77 / 3032 |
| (15) | UPUA / U929 |
| (13) | C177 / HAH5 |
| (11) | OF51 / 0446 |
| ( 9) | $335 \mathrm{H} / 1 \mathrm{CFO}$ |
| (7) | 2068 / 925A |
| ( 5) | H657 / A872 |
| (3) | UF4C / UF4A |

## 8-4-46. RAD and XIDA bus tests.

This checks the circuits used by the A9 board to read display date from RAM. A9 and A10 boards should be inserted into the card nest now. Push RESET to stop the primitive RAM test. A9S1 should be in RUN.

Setup: 5004A:

| Gnd: | A8TP1 |
| :--- | :--- |
| Start: | A8TP5 |
| Stop: | A8TP5 |
| Clock: | A8TP4 |

The + signature should be 4596

Initiate the front panel self test mode by pressing RESET while holding RESTART. Select average number 8 and press RESTART. Continue to press RESTART to change TEST\# as needed. For test \#2, marker must be at the left edge of the screen (position 000000). These signatures are only valid for software date code 020151 (upper right corner of display).

| IC \& Pin No. | Test \# |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | 0 | 1 | 2 | 3 | 4 |
| A8U15 (17) | 901 F | UPA2 | UPA2 | 0000 | 0000 |
| (15) | 0000 |  |  |  |  |
| (13) | 386 H |  |  |  |  |
| (11) | U7F5 |  |  |  |  |
| (9) | AU2P |  |  |  |  |
| ( 7) | A8FC |  |  |  |  |
| ( 5) | 22P9 |  |  |  |  |
| (3) | 6HHF |  |  |  |  |
| U12 (17) | A3H2 |  |  |  |  |
| (15) | OA24 |  |  |  |  |
| (13) | HUCP |  |  |  |  |
| (11) | 981A |  |  |  |  |
| (9) | H2CO |  |  |  |  |
| (7) | 3H81 |  |  |  |  |
| ( 5) | F1H9 |  |  |  |  |
| ( 3) | 0950 |  |  |  |  |

Software date code 002262 signatures are the same except for the following:

| IC \& Pin No. | Test \# 0 |
| ---: | ---: |
| A8U15 (13) | U834 |
| (11) | 92UA |
| (9) | 1 F01 |
| (7) | FH12 |



Table 8-4.3. Replaceable Parts.

| Reference Designation | HP Part Number | c | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 46 | 03582-66500 | 18 |  | dc Assembly, rom | 28480 | 03562-66506 |
| $c_{1}$ $c_{2}$ | 018000228 $0160-4571$ 0 0 |  |  |  <br>  <br>  |  | ${ }_{\substack{1500228 \times 9001582 \\ 01604571}}$ |
| c1 $\mathrm{c}_{2}$ $\mathrm{C}_{3}$ cta |  |  |  |  | (e) |
| ${ }_{\text {cis }}$ | ( 0160.4571 |  |  |  |  |
| ${ }_{6}{ }_{6}$ | 018000300 |  |  |  | 58880 | ${ }^{1500475 \times 001042}$ |
| ${ }_{\text {ch }}$ | 0118003509 018000309 |  |  | cisisicis | ${ }^{150} 5$ |
| ${ }_{\substack{\text { cid } \\ \text { cio }}}$ | 0112000309 $0180-309$ |  |  | ¢ 560288 |  |
| $\mathrm{c}_{11}$ | 018000300 |  |  |  | 56280 | 1500475x01012 |
| ${ }_{\substack{c \\ c_{13} \\ c_{13} \\ \hline 15}}$ |  |  |  | combe | +1500459001012 |
|  |  |  |  | cisters | $150045 \times 001012$ $150045 \times 0010{ }^{\text {a }}$ |
| $\mathrm{J}_{2}$ | 1251.5202 | 8 | 1 |  | CONNECTOR Sapin m post trpe | 28480 | 1251-5202 |
| $\mathrm{R}_{1}$ | ${ }^{0663} 55125$ | 8 | 10 |  | RESISTOR 5.1K SX, 25W FC TCT-4000/+700 <br>  | 01121 | ${ }^{\text {c } 85125}$ |
| R2 ${ }_{\text {R2 }}$ |  | $8_{8}^{8}$ |  | 0121 0 0 0121 |  |  |
| $\mathrm{Ul}_{1}$ : |  | 2 | 1 |  | 03794 | AM9218CDC Masked |
| ${ }_{\text {U2 }}$ | 181880958 $1818-0959$ | 3 | 1 |  | 03394 03794 037 |  |
| Us: |  | 退 | 1 |  | ( $\begin{aligned} & 03794 \\ & 34355\end{aligned}$ |  |
| $\mathrm{Ub}_{4}$ | ${ }^{1818} 818.518$ | 2 | ! |  | 34335 3435 | AMozi ecoc Masked |
| UR |  | 5 | , |  | ${ }^{3} 343355$ |  |
| 49 |  | $\bigcirc$ | 1 |  | cock | 181805507 1818.0568 |
| $\mathrm{Ul}_{11}$ | (1818-0523 | $\stackrel{8}{8}$ | 1 |  |  |  |
| ${ }^{4} 12$ |  |  | 1 |  | 34335 <br> 34335 | AM92icieoc masko |
| ¢ |  | $\frac{1}{2}$ | 1 |  | 34335 <br> 34335 |  |
| U16 |  | 2 |  | IC NMOS 16384-8it rom 350-ns 3 -S |  | Amp 210 CDC MASKED |
| ${ }^{418}$ | ${ }^{181880} 8570$ | 5 | 1 |  | ciserso | ${ }^{1818080570}$ |
| ${ }_{4}^{419}$ |  | 7 |  |  | ${ }^{277014}$ |  |
| $4_{22}$ | 9280-1445 | $\bigcirc$ |  | IC LCH TYL LS 4-8IT | 01295 | 3N74.3375N |
| ¢422 <br> 423 <br> 23 | (1820-1445 | : |  |  | - 01205 | an74asys |
| ( | 18820.1445 $1820-1216$ | 3 |  |  | ( 012085 | an7utisisn |
| U26 |  | - |  | ic wate til lis and duad zeinp miscellanedus parts | 01295 | 3n74Loosn |
|  |  | 3 |  |  | 28480 28480 | 200000748 200000754 |
|  |  |  |  | :SOFTWARE <br> NOTE: IF YOU HAVE TO REPLACE A ROM MUST BE REPLACED. ALL 4 OLD ROMS MUST BE REPLACED. |  |  |

Table 8-4-3. Replaceable Parts (Cont'd).

| Reference Designation | HP Part <br> Number | $\begin{aligned} & \mathbf{C} \\ & \mathbf{D} \end{aligned}$ | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 47 | 03582-66507 | 5 | 1 | PC ASSEMSLY, PROCESSOR | 28480 | 03582-66509 |
| $C_{1}$ | 014000200 | 0 | 2 | CAPACITOR-FXO 390PF +-5\% 300VOC MICA | 12136 | OML SF301J0300WVICR |
| $\mathrm{C}_{2}$ | 014000200 | 0 |  | CAPACITDR-FXD 390PF +-5x 300VDC MICA CAPACITOREFXD $130 P F$-55\% 300 VDC MICA | 72136 72136 | OM15F301J0300WVICR OMISFI31J0300WVICR |
| ${ }_{6}{ }_{4}$ | $0140-0195$ $0140-0198$ | 2 | 3 |  | 72136 72136 | DMISFIBIJ0300WVICR OMISF201J0300WVICR |
| C4 $C 5$ | $0140-0198$ $0180-0228$ | 6 | 1 |  | 72136 56289 | OMISF201J0300WVICR $1500226 \times 901582$ |
| co | 0180-0228 | 6 |  | CAPACITOR-FXD 22UF4-10x 15VOC TA | 56289 | $1500226 \times 901582$ |
| 57 | 018000228 | 6 |  | CAPACITOR-FXD 22UF+-10\% 15 VDCC TA | 56289 | $1500226 \times 901582$ |
| ${ }_{8} 8$ | 0180-0228 | 6 |  | CAPACITOR-FXO 22UF+-10x 15VOC TA | 56289 | $1500226 \times 901582$ |
| ${ }^{6}$ | 0180-1816 | 6 |  | CAPACITOR-FXD 2.2UF*-10x 35VDC TA | 56289 | $1500225 \times 903582$ |
| C10 | 0180-0197 | 8 |  | CAPACITOR-FXD 2.2UF*-10X 20VDC TA | 56289 | $1500225 \times 902042$ |
| 011 | 0160-4571 | 8 |  | CAPACITOREFXD , IUF +80-20\% 50VDC CER | 28480 | 0160-4571 |
| 612 | 0160-4571 | 8 |  | CAPACITOREFXD -1UF +80-20X 50VDC CER | 28480 | 0160-4571 |
| $C 13$ $C 14$ | 0160-4571 | \% |  |  | 28480 | 016004571 |
| C14 | $0160-4571$ $0160-4571$ | 8 |  |  | 28480 28480 | $\begin{aligned} & 0160-4571 \\ & 0160=4571 \end{aligned}$ |
| ${ }_{6} 16$ | 016004571 | 8 |  | CAPACITOR-FXO .1UF +80-20x SOVOC CER | 28480 | 016004571 |
| $C 17$ $C 18$ | 016004571 | , |  | CAPACITOR-FXD IUF +80-20\% SOVDC CER | 28480 | 0160-4571 |
| 188 $C 19$ | $0160-4571$ $0160-4571$ | 8 |  |  | 28480 28480 | $0160=4571$ $0160=4571$ |
| C20 | 0160-4571 | 8 |  | CAPACITORAFXO IUF +80-20\% SOVDC CER | 28480 | 016004571 |
| $\mathrm{C}_{21}$ | 0160-4571 | 8 |  | CAPACITOR-FXD .1UF +80-20\% SOVDC CER | 28480 | 0160-4571 |
| ${ }^{2} 22$ | 0160-4571 | 8 |  | CAPACITOR-FXD GIUF +80-20x SOVDC CER | 28480 | 016004571 |
| C23 | 016004571 | 8 |  | CAPACITOR-FXD IUF +80-20X SOVOC CER | 28480 | 0160-4571 |
| C24 | 0160-4571 | 8 |  | CAPACITDROFXO .1UF +80-20x 50VDC CER | 28480 | 016004571 |
| CR1 | 1901-0033 | 2 | 2 | DIODE-GEN PRP 180V 200MA D0.7 | 28480 | 1901-0033 |
| ${ }^{\mathrm{J}} 1$ | 1251-5202 | 8 |  | CONNECTOR SOPIN M POST TYPE | 28480 | 1251-5202 |
| J2 | $1200=0458$ $1251-5380$ | 9 |  | SOCKET-XSTR 3-CONT TO-5 DIP=SLDR CONNECTOR $2-P$ IN $M$ POST TYPE | 28480 28480 | $1200-0458$ 125105380 |
| J4 | 125105880 1251.5380 | 3 |  | CONNECTOR $2-P I N M$ POST TYPE | 28480 2840 | 1251-5380 |
| L 1 | 9100.1651 | 2 | 1 | COILemLD 750UH 5x 0=60 .190x.44LGmNOM | 28480 | 9100-1651 |
| 01 | 1854.0071 | 7 | 19 | TRANSISTOR NPN SI PDE 300 MW FTE200mhz | 28480 | 1854-0071 |
| $\mathrm{R}_{1}$ | 0683-1025 | , |  | RESISTOR 1K 5x . 25 W FC TC= $=400 / 4600$ | 01121 | C81025 |
| R2 | 0683-1025 | 9 |  | RESISTOR IK 5x. 25w FC TCE=400/*600 | 01121 | CB1025 |
| R 3 | 0683-1025 | $\stackrel{\square}{?}$ |  |  | 01121 | CB1025 |
| R4 $R 5$ | $0683-1025$ $0683-3615$ | 7 | 5 |  | 01121 01121 | C81025 c83615 |
| R6 | 0683-3615 | 7 |  | RESISTOR 360 5\% . 25 W FE TC=0400/ 4600 | 01121 | c83615 |
| R7 | 0683-1025 | 9 |  | RESISTOR IK 5x, 25W FC TC= $400 /$ (600 | 01121 | CB1025 |
| R8 | 0683-1025 | 9 |  | RESISTOR IK 54. 25 W FC TCE-400/4600 | 01121 | CB1025 |
| RQ | 0683-1025 | 9 |  | RESISTOR IK 5x. 25 W FC TC= $400 /$ ( 600 | 01121 | CB1025 |
| R10 | 0683-2005 | 7 | 2 | REAISTOR 20 5x, 25W FC TCe $400 / 4500$ | 01121 | CB2005 |
| R111 | 0683-2005 | 7 |  |  | 01121 | C82005 |
| R112 R13 13 | 0683-1025 | 9 |  |  | 01121 01121 01121 | CB1025 CB1025 |
| R13 R14 | 068311025 $0683-1335$ | 4 |  | RESISTOR 13K $5 \times$. 25 W FC TCE-400/4800 | 01121 | çi33s |
| R15 | 0683-1335 | 4 |  | RESISTOR 13K 5X, 25W FE TCR-400/4800 | 01121 | CB1335 |
| R19 R17 | $0683-5135$ $0683-1025$ | 0 |  |  | 01121 01121 | C85135 C81025 |
| R17 | $0683-1025$ $0683-1025$ | 9 |  |  | 01121 01121 01121 | C81025 c81025 |
| R19 | 0683-1025 | 9 |  | REEISTOR 1K 54, 25 W FCC TE $5=400 / 4600$ | 01121 | csiozs |
| R20 | 0683-2225 | 3 |  | RESISTOR 2.2K 5x . 25 W FC TC-40400/4700 | 01121 | C82225 |
| R21 | 0683-6815 | 5 | 1 | RESISTOR 680 5\%, 25 W FE TCR0400/4600 | 01121 | ${ }^{C} 86815$ |
| R22 R23 $R 2$ | $0683-1025$ $0683-5105$ | 9 |  |  | 01121 01121 01121 | c81025 c85105 |
| R23 $R 24$ $R 2$ | 068355105 068355105 | 4 |  | (emer | 01121 | C85105 c85105 |
| $R 25$ | 0683-5105 | 4 |  |  | 01121 | cesios |
| R26 | 0683-1025 | $\bigcirc$ |  |  | 01121 | C81025 |
| RP1 RP2 | $1810=0076$ $1810=0076$ | 0 | 3 |  | 28480 28480 | $\begin{aligned} & 1810=0076 \\ & 1810=0076 \end{aligned}$ |
| RP3 | 101000121 | 6 | 2 | NETMORK-REB O-PIN-SIP. 15-PIN-SPEG | 28480 | 1010.0121 |
| RPa | 181000121 | 6 |  | NETWORK-RES OAPIN-SIP : $15 \times P$ IN-SPCG | 28480 | 101000121 |
| RP5 | 1810-0076 | 0 |  | NETMORK-RES O-PIN-SIP .15-PIN-SPEG | 28480 | 1810-0076 |
|  | $\begin{aligned} & 09825-67909 \\ & 09825-67908 \\ & 1820-1288 \\ & 1820-0683 \\ & 1820-0681 \end{aligned}$ | 7 8 9 6 | 1 1 2 | PROCESSOR HYBRID (NOT INCLUDED W/PC ABEY PROCESSOR GASKET (NOT INCLUDED W/PC ASBY IC DRVR TTL/MOS CLOEK DRVR I-INP IC INV TTL S HEX IOINP <br> IC GATE TTL 8 NAND QUAD $2-I N P$ | $\begin{aligned} & 28480 \\ & 28480 \\ & 04713 \\ & 01295 \\ & 01295 \end{aligned}$ | $\begin{aligned} & 09825-67909 \\ & 09825-67908 \\ & \text { MMHOO26C6 } \\ & 8 N 74804 N \\ & 8 N 74800 N \end{aligned}$ |

See introduction to this section for ordering information *Indicates factory selected value

Table 8-4.3. Replaceable Parts (Cont'd).

| Reference Designation | HP Part Number | c | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 速 | 3 |  <br> ic gate th to nor guacozinp <br>  | $\begin{aligned} & 01205 \\ & 01205 \\ & 0.1205 \\ & 0.1205 \\ & 0.1205 \\ & 01295 \end{aligned}$ |  |
|  |  | ? |  |  <br>  <br> IC GATE TH La NoR GUNO 2-INP <br> HEx $1-\mathrm{IN}$ | $\begin{aligned} & 01295 \\ & 0.1205 \\ & 0.1295 \\ & 0.1295 \\ & 0.1295 \\ & 01299 \end{aligned}$ |  |
|  |  |  | ${ }^{2}$ | IC DEDR TTL $4=T O-16-L I N E$ $4=I N P$ IC DCDR TTL 4-TO-16-LINE 4 -INP IC BFR TTL LS NON-INV OCTL IC BFR TTL LS NON-INV HEX IC $V$ RGLTR TO-39 INV HEX I-INP IC FF TTL LE JOK NEG-EDGE-TRIG CRYBTAL, 13.000 MHz MISCELLANEOUS PARTA |  | 8N74154N 8 N 14154 N SN74LS307N 8N74L8112N 0410-1126 |
|  | 036000679 00400078 <br> 404000755 | $\begin{aligned} & 3 \\ & \frac{3}{3} \\ & 2 \end{aligned}$ | - | terminal-stud apcl-stof preas-mtg EXTRACTOR-PC BOARO BLK POLYC EXTACTOR | $\begin{aligned} & 28480 \\ & \begin{array}{l} 2880 \\ 28880 \\ 28480 \end{array} \end{aligned}$ | $\begin{aligned} & 030000679 \\ & 404000748 \\ & 4040=0755 \end{aligned}$ |
|  |  |  |  | $:=$ THE AT ASSEMBLY, $03582-66507$ DOES $\frac{\text { NOT }}{}$ INCLUDE A PROCESSOR OR PROCESSOR GASKET. ORDER P/N'S: <br> 09825-67907 PROCESSOR HYBRID-NEW 5001-1861 PROCESSOR HYBRID-EXCHANGE W/EXCHANGE ASSEMBLY) <br> A NEW PROCESSOR GASKET MUST BE USED WHEN REPLACING THE PROCESSOR. THIS GASKET FRAGILE AND BENDING CAN QUICKLY RUIN THE EXCHANGE PROCESSOR ASSEMBLY INCLUDES THE GASKET. <br> THE A7 ASSEMBLY, 03582-66507 DOES NOT INCLUDE A PROCESSOR OR PROCESSOR GASKET. ORDER P/N'S: <br> 09825-67907 PROCESSOR HYBRID-NEW 03582-69507 PROCESSOR HYBRID-EXCH (INCLUDED W/EXCHANGE ASSEMBLY) <br> A NEW PROCESSOR GASKET MUST BE USED WHEN REPLACING THE PROCESSOR. THIS QUICKLY RUIN IT. THE EXCHANGE PRO- |  |  |

Table 8-4-3. Replaceable Parts (Cont'd).

| Reference Designation | HP Part Number | C | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| As | 03582-66508 | 6 | 1 | pe assembly, ram | 28480 | 03582.66508 |
| $c_{1}$ | 0180-1846 | 6 | 7 | CAPACITOR-FXO 2.2UF*-10X 35VDC IA | 56289 | $1500225 \times 003582$ |
| $C^{2}$ | 0180.0210 | 6 | 13 | CAPACIPOR-FXO 3.3UF+-20X 15 VOC TA | 56280 | $1500335 \times 001542$ |
| $C 3$ $C 4$ $C 4$ | $0180-0210$ 0160.4571 | 6 |  |  | 36289 28480 | $1500335 \times 001542$ $0160-4571$ |
| C5 | 016004571 $0160-4571$ | 8 |  | CAPACITOR-FYO . IUF \$80-20\% 50VOC CER | 28480 | $0100.437 i$ |
| $C_{6}$ | 0160-4571 | 8 |  | CAPACITOR-FXO .1UF*80-20X SOVOC CER | 28480 | 0160.0571 |
| C 7 | 0160.4571 | \% |  | CAPAEITOR-FXD, IUF $+80-20 X$ SOVOC CER | 28480 | 0160.4571 |
| $\mathrm{C}^{\text {A }}$ | 0160.4571 | 8 |  | CAPACITOR-FXD , 1UF +80-20\% SOVDC CER | 28480 | 016004571 |
| ${ }_{6} 9$ | 0160.4571 | 8 |  | CAPACITOR-FXD , 1UF \$80-20X SOVOC CER | 28480 | $0160-4571$ |
| $6_{10}$ | 0160-4571 | 8 |  | CAPACITOR-FXD :IUF + B0-20x SOVOC CER | 28480 | 0160.4571 |
| ${ }_{6}{ }_{11} 1$ | $0160-4571$ $0180-0210$ | 8 |  | CAPACITOR-FXD ${ }^{1}$ UFP \$80-20X SOVDC EER | 28480 56289 | $0160-4571$ 1500335001542 |
| 612 $C 13$ | $0180-0210$ $0180-0210$ | 6 |  | CAPACITOR-FXD 3,3 SF*-20X 15 VDC TA | 56289 56289 | $1500335 \times 001542$ $1500335 \times 001542$ |
| 614 | 0180.0210 | - |  | CAPACITOR - PXD 3.3UF+-20X 15 VDC TA | 56289 | $1500335 \times 001542$ |
| ${ }_{6} 15$ | 0180.0210 | 6 |  | CAPACITOR ${ }^{\text {FXD 3,3UF*-2OX 15VOC TA }}$ | 56289 | $1500335 \times 001542$ |
| 516 | 0180.0210 | - |  | CAPACITOR-FXD 3,3UF--20X 15VDC IA | 56289 | $1500335 \times 001542$ |
| ${ }_{6} 17$ | 0130-0210 | 6 |  | CAPACITOR-FXD 3.3UF*-20\% $15 V$ OC PA | 56289 | $15003335 \times 001542$ |
| ${ }_{5} 18$ | $0180-0210$ | 6 |  | CAPACITOR*FXD 3.3UF*-20\% 15 SVC IA | 56289 | $1500335 \times 001542$ |
| ${ }_{6} 19$ | 0180-0210 | 6 |  | CAPACITOR-FXD 3,3UF*e20x 15 YOCL IA | 56289 | $1500335 \times 001542$ |
| 120 $C 20$ | $0160-4571$ $0180-0210$ | 6 |  |  | 28480 56289 | $\begin{aligned} & 0160=4371 \\ & 1500335 \times 001542 \end{aligned}$ |
| $C_{21} 1$ | 0160-4571 | 8 |  | CAPAEITOR-FXD .1UF *80-20X SOVDC CER | 28460 | 0160 -4571 |
| C22 | 0160 -4571 | 8 |  | CAPMCITOR-FXD , IUF +80-20X SOVDC CER | 28480 | 0160.4571 |
| ${ }^{\text {c } 23}$ | 0160-4571 | 8 |  | CAPACITOR-FXD .1UF +80-20X SOVOC CER | 28480 | 0160-4571 |
| ${ }_{6}{ }^{24}$ | 0160.4571 | 8 |  | CAPACITOR-FXD .1UF $\$ 80-20 \mathrm{X}$ SOVDC CER | 28480 | $0160-6571$ |
| C35 | 0160-4571 | 8 |  | CAPACITOR-FXD .1UF +80-20\% 50VDC CER | 28480 | 0160.4571 |
| C26 | 01600.0571 | 8 |  | CAPACITOROFXD .1UF +80-20\% SOVOC CER | 28480 | 010004571 |
| C29 | 0160.4571 | 8 |  | CAPACITOR-FXD : $14 F+80-20 \pm 50 V D C$ CER | 28480 | 016004571 |
| C28 | 0180.0228 | 6 |  | CAPACITOREFXD 22UF*-10\% 15VOC TA | 56289 | $1500226 \times 901582$ |
| C29 | 0180-0228 | 6 |  | CAPACITOR-FXD 22UF*-10X 15 VDC IA | 56289 | $1500226 \times 901582$ |
| C30 | 0180-0228 | - |  | CAPACITORAFXD 22UF*-10X 15VDC TA | 56289 | $1500226 \times 901582$ |
| $C_{31}$ | 0180-0220 | 6 |  | CAPACITOR-FXD 22UF\%-10X 15 VOC TA | 50289 | $1500226 \times 901582$ |
| ${ }_{6} 32$ | 0160 -4571 | 8 |  | CAPACITOR-FXD .1UF 8 80-20X SOVDC CER | 28460 | 0160-4571 |
| ${ }_{6} 33$ | 0160.4571 | 8 |  | CAPACITOR-FXD .1UF \$80-20X SOVDC CER | 28480 | 0160 -4571 |
| $C 34$ $C 35$ | $0160-4571$ | 8 |  | CAPACITORAFXD, 1 UF ABO-20X 5OVOC CER | 28480 | $0160-4571$ |
| C35 | 0160-4571 | 8 |  | CAPACITOR-FXD . 1 UF +80-20\% 50VDC CER | 28480 | 0160-4571 |
| C36 | 0160.4571 | 8 |  | CAPACITOR-FXD . 1 UF $+80-20 \mathrm{~S}$ SOVOC CER | 28480 | 0160-4571 |
| C37 | 0100.4571 | 8 |  | CAPACITOR-FXD .1UF +80-20X SOVDC CER | 28480 | 016004571 |
| ${ }^{6} 38$ | 0167.4571 | 8 |  | CAPACITOROFXD .1UF +80-20x SOVOC CER | 28480 | $0160-4571$ |
| ${ }^{6} 30$ | 0160.4571 | 8 |  | CAPACIT TOR-FXD. 14 L +80-20X SOVOC CER | 28480 | 016004571 |
| c40 | 0160-4571 | 8 |  | CAPACITOR-FXO .1UF +80-20\% SOVOC CER | 28480 | 0160.4571 |
| Cal | 0160-4571 | 8 |  | CAPACITOROFXD.1UF.80-20\% SOVDC CER | 28480 | 0160-4571 |
| CR1 CR2 | $\begin{aligned} & 1901=0050 \\ & 1901=0050 \end{aligned}$ | 3 | 10 | DIODE-SWITCHING SOV 200MA 2NE OO-35 DIDOE-SWITCHING BOV 200 MA 2NS DO-35 | 28480 28480 | $\begin{aligned} & 1901=0050 \\ & 1901=0050 \end{aligned}$ |
| $\mathrm{J}_{1}$ | 1200-0485 | 2 | 1 | SKT-ICIIA PIN, PC MTGI RT AGLI CONT | 28480 | 120000485 |
| 01 | 1853-0405 | - | 1 | TRANSISTOR PNP 2N4200 SI TO-18 PDS300mm | 28480 | 1853-0405 |
| $\mathrm{R}_{1}$ | 0083-1025 | - |  |  | 01121 | ceste25 |
| R2 | 0683-3905 | 8 | 2 |  | 01121 | ce3905 |
| $\mathrm{R}_{3}$ | 0683-3905 | 。 |  |  | 01121 | C83905 |
| Ro | 0683-5125 | - |  | RESISTOR 5.1K 5\% .25W FC TC*-400/\$700 | 01121 | cesizs |
| 01 | 1818-0508 | 9 | 16 | IC NMOS 4 K RAM DYN 270-NS 3 -S | 03406 | MM5 280N-5 |
| 42 | 1818-0508 | 9 |  | IC NMOS 4 K RAM DYN 270 -NS 3 -S | 03406 | MMS $280 \mathrm{~N}-5$ |
| 43 | 1818.0508 | 9 |  | IC NMOS 4 K RAM DYN 270 -NS $3-5$ | 03406 | MMS $280 \mathrm{~N}-5$ |
| U4 | 1818-0508 | 9 |  | IC NMOS 4K RAM DYN 270 -NS $3-5$ | 03406 | MMS $280 \mathrm{~N}-5$ |
| US | 1818-0508 | 9 |  | IC NMOS 4K RAM DYN 270-NS 3-5 | 03406 | MMS $280 \mathrm{~N}-5$ |
| U6 | 1818-0508 | 9 |  | 1C NMOS 4 K RAM DYN 270 -NS 3 -S | 03406 | MM5 280N-5 |
| 47 | 1818.0508 | 9 |  | 1 C NMOS 4K RAM DYN 270 -NS 3 -S | 03406 | MM5 $280 \mathrm{~N}-5$ |
| U8 | 1818.0508 | 9 |  | IC NMOS 4 K RAM DYN 270-NS 3 -S | 03406 | MM5 $288 \mathrm{~N}-5$ |
| U9, U10 | $1818-0508$ $1818-0508$ | 9 |  | IC NMOS 4K RAM DYN 270-NS 3-S | . 03406 | MMS $2880 \mathrm{~N}-5$ |
| $\mathrm{U}_{10}$ | 1818-0508 | 9 |  | IC NMOS 4 K RAM DYN $270-\mathrm{NS} 3-5$ | 03406 | MM5 280N-5 |
| 011 | 1818.0508 | , |  | IC NMOS 4 K RAM DYN 270 -NS 3 -S | 03406 | MM5 280N-5 |
| 412 | 1818.0508 | 9 |  | IC NMOS 4 K RAM DYN 270 -NS 3 -S | 03406 | MMS 280N-5 |
| U13 | 1818-0508 | 9 |  | IC NMOS 4 K RAM OYN 270-NS 3 -S | 03406 | MM 5 280N-5 |
| U14 | 1818-0508 | 9 |  | IC NMOS 4 K RAM DYN $270-\mathrm{NS}$ 3-5 | 03406 | MMS 280N-5 |
| U15 | 1818-0508 | 9 |  | IC NMOS 4K RAM DYn $270-\mathrm{NS}$ 3-S | 03406 | MMS 280N-5 |
| $U 10$ U17 | $\begin{aligned} & 1818-0508 \\ & 1820-1872 \end{aligned}$ | 9 | 4 | IC NMOS 4K RAM DYN 270-NS 3-S IE BPR PTL LS INV OCTL 2-INP | 03406 27014 | MM5280N-5 |
| U18 | 1820-1872 | 7 |  | IC EFR TTL LS INY OCTL 2-INP | 27014 | DMEILSoSN |
| 419 | 1820-1445 | 0 | 7 | IC LCH TTL LS AOBIT | 01295 | an7aLs375N |
| U20 | 1820-1445 | 0 |  | IC LCH TTL LS AmEIT | 01295 | SN74L8375N |

Table 8-4-3. Replaceable Parts (Cont'd).


## SERVICE GROUP 5

THE DISPLAY SECTION

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## THE DISPLAY SECTION SERVICE GROUP 5

## 8-5.1. GENERAL DESCRIPTION.

8-5-2 The Display Section performs the function of retrieving output data from the processor RAM and converting it to analog signals which control the display CRT. The output data contains alphanumeric information and graphics information. Reading the data from the RAM causes the entire RAM to be refreshed during each 1/10th display cycle.

8-5-3. The Display Section is controlled by an algorithmic state machine (ASM) which also provides instructions for interfacing with the main processor. The processor supplies information concerning the number of traces to be displayed and receives information pertaining to the marker X axis position.

8-5-4. The Display Section can be divided into four main areas contained on three boards:

1. The ASM Controller (A9 Board).
2. The Digital Display Driver (A9 Board).
3. The Analog Display Driver (A10 Board).
4. The High Voltage Amplifiers (A13 Board).

## 8-5.5. THE ASM CONTROLLER I(A9).

8-5-6. The ASM (Algorithmic State Machine) uses a ROM centered design (refer to Schematic I). The ROM (U18) has an output which is a function of the present state address and the qualifier input. A latch (U19) is inserted into the address feedback loop and is clocked to provide state interval timing. Parts of the present state address are used for qualifier selector (U20) instructions, decoder output enable (U30) instructions, and are decoded by ROM instruction decoders (U21 and U22) to provide instructions to operate other devices in the display section. Some of the instructions from the decoder are latched (U23) or modified by logic (U24,U25,U26) which changes their timing relative to the state clock.

### 8.5.7. THE DIGITAL DISPLAY DRIVER J(A9).

8-5-8. The ASM Controller establishes the sequence of operations for the Digital Display Driver. Most of the operations fall under two main groups: 1) alphanumeric operations and 2) graphics operations. Both operations require that the main processor RAM be interrogated for the desired display data. Data in the RAM is accessed by the use of addresses supplied by an address counter (U3,U4,U5) which uses the (L) FETCH command from the Display Controller as a clock input. The address counter selects 512 RAM addresses in sequential order. The (L) FETCH command to the RAM allows the display section to have direct memory access and priority over the main processor when executing RAM functions. Data from the RAM is latched by U1 and U2 (see Schematic J).

## 8-5-9. Alphanumeric Dperations.

8-5-10. There are four lines of alphanumeric characters displayed by the CRT with 32 characters in each line. The display data at each RAM address contains both alphanumeric and graphics information. Only one portion is used at a time and it takes 4 addresses to establish one character (the fourth address is not used). This information is latched into the Presettable ROM Address Counter (U12,U11,J10) by the Display Controller instructions (L) LOAD 1, (L) LOAD 2, and (L) LOAD 3. This data presets the counter which is incremented by the Display Controller instruction (L) INCR. The combined output from the counters determines the address to character ROM U16 whose output is latched by U17. Each output word from the ROM contains the X, Y dot matrix coordinates for a single dot. Each dot in a character is written on the display as the Presettable ROM Address Counter is incremented. When the last dot of the character is written, the (L) EOC line is activated which signals the Display Controller that the last dot of the character has been reached.

8-5-11. The $X, Y$ coordinates of each character are determined by parts of the output of the Address Counter. The X axis position of each character (bus lines C 3 through C 7 ) is coupled to the Analog Display Driver through a multiplexer (U13,U14,U15) which is controlled by the instruction (L) GSEL from the Display Controller. The Y axis position of each character (bus lines C8 and C9) are connected to the Analog Display Driver through the mother board via XA9A. The last character in a line is indicated by the output from U6 ((L) POINT).

## 8-5-12. Graphics Operation.

8-5-13. The Digital Display Driver provides the Analog Display Driver with Y axis amplitude data and ramp generator instructions ( X axis). The bits from the RAM Latch (U1,U2) comprise the Y axis graphics amplitude data and are coupled to the Analog Display Driver by the Multiplexer (U13,U14,U15) when the (L) GSEL line is activated by the Display Controller. The ramp generator control instructions (RAMP 1, RAMP 2, RAMP 4) and the number of records to be written on the display (BIT 1, BIT 2) are determined by the processor and are sent over the I/O Bus and latched by U9. The ramp generator signals are gated by AND gates (U29) which in turn are controlled by a secondary display controller instruction (RAMP).

8-5-14. The marker amplitude and frequency may be displayed if the processor has the $X$ axis marker address position data. When the graphics trace is at the same $\mathbf{X}$ axis position as the marker (potentiometer on the front panel), the display controller activates the (L) MAL instruction to latch the address counter data into U7. When the processor requires the information, it sends an enable instruction to U8 (tri-state buffer) which places the data on the output of U7 and on the processor I/O Bus.

8-5-15. The BLANK and MARK outputs from U1 signal the display controller to modify the graphics presentation. BLANK causes the display intensity to turn off so that the line segment connecting the point where BLANK is given and the following point will not be displayed. MARK causes the intensity to increase the Line Drawer on the Analog Display Driver to hesitate so that the marker is presented as a brighter point on the graphics display.

## 8-5-16. The Test Switch.

8-5-17. The Test Switch is used to establish a test pattern on the CRT display. When the switch is in the TEST position, the outputs from latches U1,U2, and U9 are set low. This
isolates the Processor RAM and the Processor I/O Bus from the Display Section. The Display Controller continues to run using zeros for RAM output data causing the character " $A$ " to be displayed on all four alphanumeric lines. The section of the Test Switch connected to pin 14 of U13 causes an address counter bit to be switched into the $Y$ axis amplitude data input resulting in a periodic square wave presentation on the CRT display. Note that the display cycle takes place at a rate of about 60 times a second which makes the display appear to be continuous.

### 8.5.18. THE ANALOG DISPLAY DRIVER K(A10).

8-5-19. The Analog Display Driver receives digital data from the Digital Display Driver. The data is converted to voltage levels by DAC's (digital-to-analog converters) whose outputs are used for several purposes:
a. To provide an input signal to the Line Drawer.
b. To provide a sweep control signal to the Ramp Generator.
c. To provide alphanumeric character control signals to summing amplifiers.

8-5-20. The outputs from the Line Drawer, Ramp Generator, and the summing amplifiers are multiplexed (U17) so that either alphanumeric or graphics control signals are available to the X and Y high voltage grid control amplifiers. The output from the Z Axis Intensity Correction Amplifier (Graphics) or the Z Axis Intensity (Alpha) circuit are multiplexed (U15) for input to the Z Axis high voltage grid control amplifier.

8-5-21. The operations performed by the Analog Display Driver can be divided into two areas:
a. Alphanumeric operations.
b. Graphic operations.

## 8-5-22. Alphanumeric Operations.

8-5-23. The Display Controller sets the Analog Display Driver for alphanumeric operations by setting the (L) ASEL line LOW and setting the RAMP line LOW. The (L) ASEL signal causes the Graphics-Alpha MUX to switch the alphanumeric signals to the $X$ and $Y$ axis outputs. The absence of the RAMP signal (LOW) causes the Z Axis MUX to place a fixed alphanumeric intensity level from the $\mathbf{Z}$ Axis Intensity Alpha circuit on the $\mathbf{Z}$ Axis output. This also occurs during marker intensification.

8-5-24. To display alphanumeric characters requires that the character position be defined as well as the position of each dot in the character matrix.

8-5-25. The X Axis character position is defined by the output from DAC U1. U2 is used as a voltage converter with capacitors $\mathrm{C} 116, \mathrm{C} 118$ and C 1 providing compensation for the step transition outputs from U1. The output from U2 is scaled by the resistor divider network formed by R60 and R61. The X character dot coordinate is converted by the X Axis Matrix DAC. The output is scaled by the resistor divider network formed by R54 and R62. The position and dot matrix coordinates are summed by the X Summing Amplifier U14. The output from U14 is the X Alpha input to the Graphics-Alpha MUX.

8-5-26. The Y Axis character position is defined by the output from the Y Axis Alpha DAC U11. The Y Axis character dot coordinate is defined by the output from the Y Axis Matrix

DAC U10. This output is scaled by the resistor network comprised of R39 and R46 and summed with the output from U11. The sum is amplified by the Y Summing Amplifier U12 which has an output to the Graphics-Alpha MUX.

## 8-5-27. Graphics Operations.

8-5-28. The Display Controller sets the Analog Display Driver for graphics operations by setting the (L) GSEL line LOW and the RAMP line HIGH.

## 8-5-29. THE LINE DRAWER K(A10).

8-5-30. The Line Drawer produces an output which is a linearly changing voltage representing the $Y$ Axis component of a line segment connecting two successive graphic points. A secondary output to the $Z$ Axis Intensity Correction circuit represents the rate of change in the $Y$ Axis deflection. The input to the Line Drawer is formed by DC step voltages which come from the Y Axis Graphics - X Axis Alpha DAC.

## 8-5-31. Circuit Description.

8-5-32. In the Sample Hold Circuit, Q3 operates like a switch and is controlled by the SAMPLE signal through Q5 and Q4. The summation junction takes the difference between the last point from the integrator and the present point from the output of U 2 . This is the length of the line to be drawn. This voltage is sampled and causes the Integrator to ramp from the previous point to the next point in a specified amount of time. Note that the integration time is the same for all pairs of points compared. The Line Drawer is sent the same word twice in a row to generate the marker.

## 8-5.33. The Ramp Generator.

8-5-34. The Ramp Generator provides an output for sweeping the $X$ Axis in the graphics mode of operation. The sweep rate is directly proportional to an input which represents the number of graphics records to be displayed. The sweep time is determined by the Display Controller through the (L) RTRC line. To generate the marker, the Ramp Generator is momentarilly stopped.

## 8-5-35. Circuit Description.

8-5-36. The impedance converter (Q6) provides a low current source load impedance to the DAC. Q7A and Q7B forms a current mirror circuit. The current out of the collector of Q7B equals the collector current of Q6 (for large transistor betas). The current from Q7B causes the capacitor $\mathbf{C} 20$ to charge producing a ramp voltage.

8-5-37. A retrace ((L) RTRC) signal sets the Retrace Logic R-S flip-flop U21 causing Q8 to turn on the Darlington Pair Q9 and Q10 which discharge capacitor C20. When the voltage across C20 becomes negative, comparator U23 resets the Retrace Logic R-S flip-flop U21 turning off the Retrace Current Source.

8-5-38. In the graphics mode of operation, the $X$ axis is swept by the Ramp Generator which has a sweep rate controlled by the output from the Graphics Sweep Rate DAC U7. The sweep is terminated by the Display Controller command (L) RTRC.

8-5-39. The output from the Ramp Generator is also used as an input to the Marker Comparator U23. The position is determined by comparing the $X$ Axis position voltage from the Ramp Generator and the voltage from the Marker Position potentiometer on the front panel. The output from the comparator (COMP) is used to trigger the Marker Comparator Latch (see Schematic I board A9).

8-5-40. The output from U2 defines the Y Axis graphics amplitude in the graphics mode of operation. The DC levels from the DAC U1 form step voltage changes that would represent a series of points on the CRT if they were displayed directly. The step DC levels from U2 form the input to the Line Drawer which has an output representing a line connecting the DC levels (points) as the X Axis is swept. This output from the Line Drawer is the Y Graphics input to the Graphics Alpha MUX. Another output from the Line Drawer is the input to the Z Axis Intensity Correction circuit.

8-5-41. The Z Axis Intensity Correction circuit enables the graphics display to have consistent intensity throughout the length of the graphics trace. The circuit uses an output from the Line Drawer, which represents a positive or negative difference between Y Axis points and converts this difference to an absolute value (always positive). For a simplified representation of the circuit, see Figure 8-5-1.


Figure 8-5.1. Intensity Correction Simplification.

## 8-5.42. TROUBLESHOOTING THE DISPLAY CONTROL SECTION.

8-5-43. The Display Control Section consists of the Digital Controller (Schematic I), Digital Display Driver (Schematic J) and Analog Display Driver (Schematic K). These circuits plus the XYZ Amplifier can be quickly checked using the test switch on the Digital Controller/Display Driver Assembly (A9). All that this test requires from the rest of the instrument is the power supplies (including high voltage) and the processor clock. Moving the switch to test should produce a test pattern.

8-5-44. The display test pattern consists of all A's for the alpha and a square wave for the graphics. If this pattern is correct, the display section is at least basically working. A problem with the character ROM could exist and not be apparent from the test but, in general, the test is complete. Problems with the display not in this section can usually be traced to the Processor Service Group (4), especially the RAM assembly. If the test pattern is incorrect, refer to the Troubleshooting Quick Reference to localize the problem to a schematic.

### 8.5.45. Marker Problems.

8-5-46. The marker position potentiometer controls the voltage on one side of a comparator (A10 U23); the other side has the sweep ramp for an input. When the voltages are equal, the COMP line to the controller (A9) goes high. This causes the address (in RAM) of that display point to be latched into A9 U7 and sent over the I/O Bus to the processor. The processor then sets bit 14 of the display word at that address true to intensify the dot.

8-5-47. If an HP-IB controller is available, a simple check can be made to determine where the problem is. If the marker works when programmed over the HP-IB, then the processor and the RAM are OK and the problem is with the A9 or A10 circuitry. If the marker does not work over the Bus, the problem is probably with the processor or RAM circuits.

## 8-5-48. Troubleshooting The Display Controller (I).

8-5-49. Signature Analysis is quite effective in troubleshooting this section. For the ASM, two signature analysis routines are provided. SA test \#1 effectively removes the qualifier select from the circuit. In this way, only U18 and U19 are being tested. SA test \#2 is essentially normal operation. The troubleshooting procedure would then be to check U18 and U19 with test \#1 and proceed to test \#2 if this failed to find the bad component.

Table 8-5-1. Display Controller Signature Analysis.
Introduction - troubleshooting the digital section of display (ag).
The major difficulty associated with troubleshooting this board is the closed-loop nature of the ASM. To this end, there are two SA routines provided. SA Test \#1 effectively isolates the control ROM from the qualifier inputs. This can be used for troubleshooting the ASM. For problems that aren't associated with the ASM (see procedure below), SA Test \#2, which is essentially normal operation, is used.

TROUBLESHOOTING PROCEDIJRE -(Important: For REV B and earilier A9, refer to Backdating.)

1. Check the outputs of the State Latch U19 using Test \#2.
2. Check the outputs of the State Latch U19 using Test \#1.
3. If both are correct, check other signatures using Test \#2.
4. If 1 is incorrect, check other signatures using Test \#1.In this case, the qualifiers are incorrect and must be isolated from the ASM for troubleshooting.

NOTE
a. If 2 is incorrect, check especially U18 and U19.
b. If 2 is correct, U18 and U19 are probably OK.

## SA TEST \#1.

Setup:

1. Move A9 S1 to the "TEST" position.
2. Move A 9 J 1 to the " $T$ " position.
3. Connect the 5004A as follows:

| GND | $\mathrm{J} 5(1)$ | or |
| :--- | :--- | :--- |
| GND TP |  |  |
| CLK | $\mathrm{J}(3)$ | - |
| or TP1 |  |  |
| START/STOP | $\mathrm{J5}(4)$ | $\boxed{ }$ or TP3 |

4. Momentarily short A9 J2. This should give a rather strange display - NOT THE TEST PATTERN.
5. The +5 signature should be HFUG. If this is incorrect, troubleshoot the clock from the processor U19(11) and the address counter (Schematic J) U3,4 and 5.
6. If an incorrect signature is encountered, RECHECK THE SETUP. It may be necessry to repeat Step 4.

Signatures For SA Test \#1

| IC | U1 | U2 | U3 | U4 | U5 | U6 | U7 | U9 | U10 | U11 | U13 | IC |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Pin 1 |  |  | 7 A 23 |  |  |  | HFU6 |  |  |  | U567 | 1 Pin |
| 2 | 0000 | 0000 |  |  |  |  | 3 C 86 |  |  | 0000 | 0000 | 2 |
| 3 |  |  |  |  |  |  | P770 |  |  |  | H2FA | 3 |
| 4 |  |  |  |  |  |  | 562C |  |  |  | UPF9 | 4 |
| 5 | 0000 | 0000 | OC12 |  |  |  | 6 HAH |  | 0000 | 0000 | 0000 | 5 |
| 6 | 0000 | 0000 |  |  |  |  | OAU5 |  |  |  | A16F | 6 |
| 7 |  |  | HFU6 |  |  |  | 6FPC |  |  |  | 468P | 7 |
| 8 |  |  |  |  |  | 7153 | A16F |  |  |  |  | 8 |
| 9 | 0000 | 0000 |  |  |  |  | H345 |  |  | 0000 | C493 | 9 |
| 10 |  |  |  | 449A | HFU5 |  | 0000 |  |  |  | 0474 | 10 |
| 11 |  |  | HFU6 | 8516 | A16F |  | U567 |  |  |  | 0000 | 31 |
| 12 | 0000 | 0000 |  | 37P8 | 6FPC |  | 3H31 |  |  | 0000 | PC1P | 12 |
| 13 |  |  | U567 | 0474 | 562C |  | H2FA |  |  |  | $37 \mathrm{P8}$ | 13 |
| 14 |  |  | U567 | H2FA | P770 |  | 0474 |  |  |  | $37 \mathrm{P8}$ | 14 |
| 15 | 0000 | 0000 |  | 68FO | 449A |  | 87P6 |  |  |  |  | 15 |
| 16 | 0000 | 0000 |  |  |  |  | A195 |  |  |  |  | 16 |
| 19 | 0000 | 0000 |  |  |  |  | 97FA |  |  |  |  | 19 |

Table 8-5.1. Display Controller Signature Analysis (Cont'd).


## SA TEST \#2.

Setup:

1. Move A9 S1 to the "TEST" position.
2. Move A9 J1 to run (R).
3. Connect the 5004A as follows: (Only REV D and later A9 fitted with J5.)
GND
CLK
START/STOP
J4(1) or GND TP
J4(3) or TP 1
J4(4) or TP 4
4. The +5 signature should be FHFF. IMPORTANT: For instruments with serial number prefix 1747 A , remove the A10 assembly or set the marker to the left edge of the display. Move the test switch to RUN to set the marker.

Signatures For SA Test \#2

| IC | U3 | 14 | U5 | U7 | U9 | U16 | U17 | U18 | U19 | U20 | U21 | U22 | U23 | IC |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Pin 1 |  |  |  |  | 0 |  |  |  |  | 0 | F3FA | PA45 |  | 1 Pin |
| 2 | P129 |  |  | 0 | 0 |  | 6HOP |  | 41C4 | 0 | 6F16 | F32C |  | 2 |
| 3 |  |  |  |  |  |  |  |  |  | 0 | 4U07 | 488P |  | 3 |
| 4 |  |  |  |  |  |  |  |  |  | 27 A 3 | P546 | PA45 | 00AA | 4 |
| 5 | 9482 |  |  | 0 | 0 |  | C6UP |  | 2F63 | 9482 | 034C | U0C8 |  | 5 |
| 6 |  |  |  | 0 |  |  | CA95 |  | 8059 | 4AH9 | C9U7 | 204P |  | 6 |
| 7 |  |  |  |  | 0 |  |  |  |  | 9PP3 | 783F | PA45 | H66A | 7 |
| 8 |  |  |  |  |  |  |  |  |  | 0 |  |  |  | 8 |
| 9 |  |  |  | 0 |  | 55FP | 233C | 7453 | F848 | 0 | 5H3U | U0C8 | PC11 | 9 |
| 10 |  | 68UC | FHFF |  |  | 138F |  | OP92 | 0 | 1243 |  |  |  | 10 |
| 11 |  | 27 A 3 | H60C |  |  | UUAP | 82FC | 56P6 | 0 |  |  |  |  | 11 |
| 12 |  | 5HFP | 3861 | 0 |  |  | HU48 |  | PAH1 |  |  |  |  | 12 |
| 13 |  | 30FA | 40AH |  |  | 7H9A |  | F704 |  |  |  |  | 26 HH | 13 |
| 14 |  | 7629 | H291 |  |  | 2PFA |  | 8307 | C8PO |  |  |  |  | 14 |
| 15 |  | P129 | 68UC | 0 |  | A98U | U5F4 | C8PO |  |  | OFA8 | OFA8 |  | 15 |
| 16 |  |  |  | 0 |  | 3H3P | C6F8 | PFP8 | HH59 |  |  |  |  | 16 |
| 17 |  |  |  |  |  |  |  | 301A |  |  |  |  |  | 17 |
| 19 |  |  |  | 0 |  |  |  |  | 980H |  |  |  |  | 19 |
| 21 |  |  |  |  |  |  |  |  |  | H664 |  |  |  | 21 |
| 22 |  |  |  |  |  |  |  |  |  | 6HOP |  |  |  | 22 |
| 23 |  |  |  |  |  |  |  | P44H |  | 6HOP |  |  |  | 23 |

Table 8-5-2. Display Control.

## Inputs To Data Selector.

1. Bit 1
2. Bit 2
indicate the number of records to be displayed on CRT.
3. Bit 7
4. Bit 8
5. Blank
6. CNU
7. (L) COMP
8. (L) EOC
9. MARK
10. (L) POINT
indicate Address Counter position in memory.
blank trace between two consecutive outputs of RAM graphics data.
comparator not used.
comparator output.
end of character, indicates the last dot in a character matrix.
mark an intensified dot on the graphics display.
last point for a record or alphanumeric character line.

## Display Controller Dutputs (Primary).

1. (L) A MODE
2. (L) FETCH
3. (L) G MODE
amplitude mode.
fetch RAM data, increment Address Counter.
graphics mode.
increment Presettable ROM Address Counter, latch character ROM output.
4. (L) LOAD 1
5. (L) LOAD 2
6. (L) LOAD 3
7. (L) MAL
8. (L) RTRC
9. (L) S COMP
loads RAM output data into Presettable ROM Address Counter, three RAM words required (four words per character).
10. (L) START
11. (L) STOP
12. (L) STROBE
marker address load (latch U7).
ramp retrace, occurs at the end of a displayed record.
set comparator latch.
used to initiate and terminate the display of a record or records.
strobes one-shot multivibrator $\mathbf{U} 25$ used to control $\mathbf{Z}$ axis in alphanumeric mode.
13. (L) Z OFF
14. (L) Z ON
set and clear R-S flip-flop U23, used in graphics.
mode to control $Z$ axis.

## Display Controller Outputs (Secandary).

1. (L) ASEL
2. (L) G SEL
3. RAMP
4. SAMPLE
5. ZTTL
alphanumerics select.
graphics select.
gates RAMP Generator control signals, also controls analog multiplexer on analog driver board.
activates sample/hold circuit in line drawer, signal derived from
(L) Load 1.
activates $Z$ axis grid drive, controls intensity.

## Instructions From Processor.

1. RAMP 1 write one record on display.
2. RAMP 2 write two records on display.
3. RAMP 4 write four records on display.




Figure 8-5-3. Troubleshooting Quick Reference For Schematics I, J, and K.








Output of U2 A
External trigger; A10 TP $0.1 \mathrm{v} / \mathrm{div} ; \times 10$ probe Ovdc 2 cm from bottom $2 \mathrm{~ms} / \mathrm{div}$ sweep (connect to bottom of R2)
$X$-Axis Alpha U17110 $0.2 \mathrm{v} / \mathrm{div} ; \times 10$ probe Ovde 2 cm from bottom $2 \mathrm{~ms} / \mathrm{div}$ sweep (connect to bottom of R2)


X-axis graphics-U17(7)
$0.02 \mathrm{v} / \mathrm{div} ; \times 10$ probe
Ovdc 2 cm from bottom $2 \mathrm{~ms} / \mathrm{div}$ sweep External trigger from trigger TP on A10; + slope


A10 Signal Points




Table 8-5.3. Replaceable Parts.


Table 8-5-3. Replaceable Parts (Cont'd).

| Reference Designation | HP Part Number | $\begin{aligned} & \text { C } \\ & \text { D } \end{aligned}$ | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 410 | 03582-66510 | 0 | 1 | PC ASSEMALY, ANALOG DISPLAY DRIVER | 28480 | 03582-66580 |
| $\mathrm{Cl}_{5}$ | 0160-3622 | 8 |  |  | 28480 28480 | $0160-3622$ |
| $C 3$ $C 4$ | $0160-3622$ $0160-3622$ | 8 |  |  | 28480 28480 | $\begin{aligned} & 0160=3622 \\ & 0160=3622 \end{aligned}$ |
| 66 | $0160-3622$ | 8 |  | CAPACIPOR-FXD .1UF +80-20X 100VDC CER | 28480 | 0160-3622 |
| C7 | 0160-3622 | 6 |  | CAPACIPOR FPD .1UF +80-20X loovde Cer | 28480 | 0160-3622 |
| C88 | $0160-3622$ $0180-0100$ | 6 3 |  |  | 28480 56289 | $\begin{aligned} & 0160-3622 \\ & 1500475 \times 903582 \end{aligned}$ |
| 60 610 | $0180-0100$ $0160-4438$ | 3 | 17 |  | 56289 28480 | $\begin{aligned} & 1500475 \times 903582 \\ & 0160-4438 \end{aligned}$ |
| C11 | 0160.3622 | 8 |  | CAPACITOROFXD. $1 \mathrm{CF}+80-20 \times$ l 100 VDC CER | 28480 | 0160-3622 |
| ${ }_{6} 12$ | 0160-3622 | 6 |  | CAPACITOR FFXO IUF +80-20x 100VOC CER | 28480 | 0160-3622 |
| ${ }_{1} 13$ | 0160-2204 | 2 | - | CAPACIPORAFXO 20PF +-5x S00VOC CER 0*-30 | 28480 | 0160-2264 |
| ${ }_{C} 14$ | 0160-3622 | 8 |  |  | 28480 | 016003622 |
| ${ }_{6} 16$ | 0160-4682 | 2 | 1 | CAPACITORAFXD 1000 PF + $-2.5 \times 160 \mathrm{VDC} \mathrm{POLYP}$ | 28480 | 0160-4682 |
| $C 17$ $C 18$ | $0160-3622$ $0160-3622$ | \% 8 |  | CAPACIPOR-FXD G CAPACITOR | 28480 28480 | $0160-3622$ $0160-3622$ |
| c19 | 0160-2264 | 2 |  | CAPACIPOR-FXD 20pF \$05\% Soovoc CER 0*-30 | 28480 | 0160-2264 |
| c20 | 0160.3787 | 6 | 1 | CAPACIPOR-FXO IUF +-10x 50VOC MEPOPOLYC | 28480 | 0160-3787 |
| $C_{21}$ | 0180-0100 | 3 | 1 | CAPACITOR FFXD 4, 7 UFs $=10 \times 35 \mathrm{VDC} \mathrm{TA}$ | 56289 | 1500475x903582 |
| C22 | 0160-3622 | 8 |  |  | 28480 | 0160-3622 |
| C23 | 0100-3622 | B |  | CAPACITOR-FXO .IUF +80-20X 100 VDC CER | 28480 | 0160-3622 |
| $\mathrm{C}_{24}$ | 0160-3622 | 8 |  | CAPACITOR-FXD -1UF *80-20X 100 VOC CER | 28480 | 0160-3622 |
| C25 | 0160-3622 | 8 |  | CAPACITPRRFPD 14 C (80-20X 100VDC CER | 28480 | 0160-3622 |
| 627 029 | 0180-0100 | 3 |  |  | 56289 28480 | $1500475 \times 903582$ $0160-2264$ |
| C28 c 29 | $0160-2264$ $0160-3622$ | 2 <br> 8 |  |  | 28480 28480 | $\begin{aligned} & 0160-2264 \\ & 0160-3622 \end{aligned}$ |
| C30 | 0160-2264 | 2 |  | CAPACITDR-FXD 20PF \$-5x 500VDC CER 0 + - 30 | 28480 | 0160-2264 |
| C31 | 0160-3622 | 8 |  | CAPACITOR-FYD - IUF +80-20x 100 VOC CER | 28480 | 0100-3622 |
| ${ }_{6} 634$ | 0160-3622 | 8 |  | CAPACITOR-FXD IUF +80-20X 100 VDC CER | 28480 | 0160-3622 |
| ${ }_{6} 635$ | 0160-2264 | 2 |  | CAPACIPOR-FXD 20PF + $5 \times 5$ 500VDC CER O*-30 | 28480 | 0160-2264 |
| c36 | 0160.3622 | 8 |  | CAPACITOR-FXD IUF +80020 x 100VDC CER | 28480 | 0160-3622 |
| C38 | 0160-3622 | 8 |  | CAPACITPR-FXD $14 F+80-20 x$ 100VOC CER | 28480 | 0160-3628 |
| 639 | 0180-0100 | 3 3 |  | CAPACIPOREFXD 4, 7UF+E10X 35VDC PA | 56289 | $1500455 \times 903582$ |
| cao | 0180-0100 | 3 |  | CAPACITOR-FXD $4,7 \mathrm{CF}+10 \mathrm{X}$ 35VDC TA CAPACITOR-FXD | 56289 56289 | $1500475 \times 903582$ 1500475903582 |
| C41 cat | 018000100 0160.3622 | 3 8 8 |  |  | 56289 28480 | $1500475 \times 903582$ $0160-3622$ |
| 643 | 0160-3622 | 8 |  | CAPACITOR-FXD IUF +80-20x 100VOC CER | 28480 | 0160-3622 |
| ${ }^{4} 45$ | 018000100 | 3 |  | CAPACITOR-FXD $4,74 F+=10 \mathrm{X}$ 35VDC TA | 56289 | $1500475 \times 903582$ |
| ${ }^{4} 46$ | 0140-0191 | 8 | 2 |  | 72136 | DM15E560.50300WVICR DMISES60.J0300WVIER |
| C47 CAS | $0140-0191$ $0160-2199$ | 6 2 |  | CAPACITOR-FXD SGPF +55 300 VOC MICA CAPACITOR | 72136 28480 | DMISES60.50300WVIER $0160-2100$ |
| C100 | 0180.0100 | 3 |  | CAPACITOR=FXD 4.7UF+-10x 35vDC fa | 56289 | $1500475 \times 903582$ |
| ${ }^{\text {c }} 101$ | 0180-0100 | 3 |  | CAPACIPOR-FXD G, 7 UFPE10X 35VDC YA | 56289 | 1500475903582 |
| ${ }^{\text {c }} 102$ | 0160-3622 | 8 |  | CAPACITOR-FXO. IUF $+80=20 \mathrm{X}$ IOOVDC CER | 28480 | 0160-3622 |
| $\mathrm{ClO}^{1}$ | 0160-3622 | 8 |  |  | 28480 | 0160-3622 |
| C104 | 0160-3622 | 8 |  | CAPACITOR-FXD.IUF +80-20x loovDC CER | 28480 | 0100-3622 |
| ${ }^{\text {c }} 105$ | 0180-0100 |  |  | CAPACITOREFXD 4.7UF*-10X 35VDC PA | 56289 |  |
| C106 | 0160-2264 | 2 8 8 |  | CAPACITOR-FXD 20PF \$-5x 500VDC CER O+=30 | 28480 28480 | $0160-2264$ |
| $C 107$ $C 108$ | 0160.3622 0180.0100 | 8 3 |  |  | 28480 56289 | $0160-3622$ $1500475 \times 93582$ |
| C109 | 0160-3622 | 8 |  | CAPACITOROFXD IUF $+80-20 x$ IOOVOC CER | 28480 | 0160-3622 |
| $\begin{aligned} & C_{1} 110 \\ & C_{1} \end{aligned}$ | $0160-3622$ $0160-3622$ | 8 |  |  | 28480 28480 | $\begin{aligned} & 0160=3622 \\ & 0160=3622 \end{aligned}$ |
| C112 | 0160.3622 $0180-0100$ | 3 |  |  | 28480 56289 | $0160-3622$ $1500475 \times 903582$ |
| C113 | 0160.3622 | 8 |  | CAPACIPOR-FXD IUF $+80-20 \mathrm{X}$ 100VDC CER | 28480 | 0160-3622 |
| C114 | 0160-3622 | 8 |  | CAPAEITOR-FXD .IUF +80-20x 100VDC CER | 28480 | 0160-3622 |
| $\begin{array}{lll}C_{1} & 15 \\ C_{1} & 16\end{array}$ | $0160-3622$ $0160-2264$ | 8 2 |  |  | 28480 28480 | $0160-3622$ $0160-2264$ |
| C119 | 0160-3622 | 8 |  | CAPACIPOR-FXD 1 IUF +80-20x 100 VOC CER | 28480 | $0160-3622$ |
| 6119 | 0180.0100 | 3 |  | CAPACITOR-FXD 4.7UF*-10X 35VDC IA | 56889 | $1500475 \times 903582$ |
| C120 | 0180-0100 | 3 |  | CAPACIPOREFXD 4.7UF*-10x 35VDC TA | 56289 | 15004759003582 |
| C122 C123 | $0160-3022$ $0160-3622$ | 8 |  |  CAPACITOROFXD . 1 UF +80-20X IOOVDC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0160-3622 \\ & 0160-3622 \end{aligned}$ |
| C124 | 0160-3622 | 8 |  | CAPACIPOR-FXD : $1 \mathrm{UF}+80020 \mathrm{X}$ 100VDC CER | 28480 | $0160-1622$ |
| C125 | $0180-0100$ | 3 |  | CAPACIYOR-FXD 4,7UF+010X 35VDC TA | 56289 | $1500475 \times 903582$ |
| C126 | 0180-0100 | 3 |  | CAPACIPOR-FXD 4.7UF+010x 35VDC TA | 56289 | $1500475 \times 903582$ |
| $\begin{aligned} & C 127 \\ & C 128 \\ & C 129 \\ & C 130 \\ & C 140 \end{aligned}$ | $\begin{aligned} & 0160=3622 \\ & 0160-3622 \\ & 0180=0100 \\ & 0160=3622 \\ & 0160-3622 \end{aligned}$ | 8 8 3 8 8 |  | CAPACIYOR-FXO IIUF *80-20X 100VOC CER CAPACITOR-FXD AUF +80-20X IOOVOC CER CAPACIYOR-FXO 4.7UF+-10X $35 V O C$ TA CAPACITOR-FXD .IUF +80-20X 100 VOC CER CAPACIYOR-FXD , IUF $\$ 80-20 \mathrm{x}$ loovoc CER | $\begin{aligned} & 28480 \\ & 28480 \\ & 56289 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0160-3622 \\ & 0160=3622 \\ & 1500475 \times 903582 \\ & 0160=3622 \\ & 0160=3622 \end{aligned}$ |

Table 8-5.3. Replaceable Parts (Cont'd).

| Reference <br> Designation | HP Part Number | $\begin{aligned} & \mathrm{C} \\ & \mathrm{D} \end{aligned}$ | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| C141 | 0160-3622 | 8 |  | CAPACIPORAFXD . 1 UF * 80-20X 100 VDC CER | 28480 | 016003622 |
| C201 | 0160-3622 | 8 |  | CAPACITOR-FXD -1UF +80-20X 100 VDC CER | 28480 | 0160-3622 |
| C203 | 0160-3622 | A |  | CAPACITOR-FXD -1UF*80-20X 100VDC CER | 28480 | 0160-3622 |
| C205 | 0160-3622 | 8 |  | CAPACITOR-FXD - 14 F +80-20X 100 VDC CER | 28480 | 0160-3622 |
| C210 | 0180.1746 | 5 |  | CAPACITORAFXD ISUF*-10X 2OVDC TA | 56289 | $1500156 \times 902082$ |
| C211 | 0180-1746 | 5 |  | CAPACITORAFXO 15UF*-IOX 2OVDC TA | 56289 | 1500156x902082 |
| CR1 | 1902-3030 | 7 | 3 | OLODE-2NR 3.01V 5x DO.7 PDa, Aw TC*-.067x | 28480 | 1902-3030 |
| CP? | 1901-0535 | 9 | 4 | OIODE-SCHOTTKY | 28480 | 1901-0535 |
| CR3 | 1901-0535 | 9 |  | OIODE-SCMOTTKY | 28480 | 1901-0535 |
| CR201 | 1902-0777 | 3 |  | OIODE-2NP 1 N825 6.2 V 5x OO-7 POE, 4W | 04713 28480 | 1N825 |
| Cr202 | 1901-0050 | 3 |  | OIODESWITCHING 8OV 200MA 2 NS DO-35 | 28480 | 1901-0050 |
| CR203 | 1901-0050 | 3 |  | OIOOE-SWITCHING SOV 200MA 2NS O0.35 | 28480 | 1901-0050 |
| CR204 | $1901-0050$ | 3 |  | OIODE-SWITCHING SOV 200MA 2 NS OO-35 | 28480 | 1901-0050 |
| CR205 | 1901-0050 | 3 |  | OIOOE-SWITCHING BOV 200MA 2NS DO-35 | 28480 | 1901-0050 |
| CR200 CP207 | $1901-0050$ $1901-0050$ | 3 3 |  |  | 28480 28480 | $1901-0050$ $1901-0050$ |
| CR208 | 1901.0050 | 3 |  | OIODE-SWITCHING 8OV 200ma 2NS O0-35 | 28480 | 190100050 |
| Cr209 | 1901-0050 | 3 |  | OIODE-SWITCHING 80V 200ma 2 NS 00.35 | 28480 | 1901-0050 |
| CP210 | 1901-0535 | 9 |  | OIDOE-SCHOTPKY | 28480 | 1901-0535 |
| CR211 | 1901-0535 | 9 |  | DIOOE-SCHOTTKY | 28480 | 1901-0535 |
| 4 | $9100-2550$ | 0 | 6 | COIL.MLD 33UH 10x 0E45 . 1560 C . 375 LGONDM | 28480 | 910002556 |
| 42 | 9100-2556 | 8 |  | COIL=MLD 33UH 10X OE45 . 1560 X . 375 LGONDM | 28480 | 910002556 |
| L3 | 9100-2556 | 8 |  | COIL-MLO 33UH 10 X OE45 , 1560X,375L6-NOM | 28980 | 9100-2556 |
| 01 | $1854-0475$ $1853-0083$ | 5 0 | 2 | TRANSISTOR=OUAL NPN PDE 750 mm | 28480 28980 | 1854.0475 $1853-0083$ |
| 02 03 | $1853-0083$ $1855-0272$ | 9 | 2 | TRANBISTOR-DUAL PNP PDE600MW TRANSISTOR MOSFET N-CHAN TO-72 SI | 28980 04713 | 185300083 MFE3004 |
| 63 64 | $1855-0272$ 1854.0215 | 2 1 1 | 1 |  | 04713 | MFES 3611 |
| 65 | 18530089 | 5 | 6 | TRANSISTOR PNP 2N4917 SI PDEZ20mw | 07263 | 2N4917 |
| $00_{0}$ | 1854.0023 | 9 | 1 | TRANSISTOR NPN SI TO-18 POE36OMW | 28480 | $1854-0023$ |
| 67 | $1853-0083$ $1853-0089$ | 9 5 |  | TRANSISTOR-DUAL PNP PDE 600 MH TRANBISTOR PNP 2N4917 SI PDE200MN | 28480 07263 | $\begin{aligned} & 1853-0003 \\ & 2 N 4917 \end{aligned}$ |
| 68 69 | $1853-0089$ $1854-0071$ | 5 7 |  | TRANEISTOR PNP 2N4917 SI PDE 200 MW | 07263 28480 | 1854-0071 |
| 610 | 1854.0233 | 3 |  | TRANSISTOR NPN 2NSB6E SI TO-39 PDEIW | 01928 | 2N3866 |
| 6201 | 1854-0071 | 7 |  | TRANSISTOR NPN SI PDE 300 MW FTE200MHZ | 28480 | 1854.0071 |
| 6202 | $1853-0016$ | 8 |  | TRANSISTOR PNP SI TO-92 PDE 300 MW | 28480 28480 | $1853-0016$ 185400071 |
| 6203 0204 | 1854.0071 $1854-0071$ | 7 |  |  | 28480 28480 | 185400071 $1854-0071$ |
| 6204 6205 | 185400071 $1854-0071$ | 7 |  |  | 28480 28480 | 18540091 18540071 |
| $\mathrm{F}_{1}$ | 0698.4435 | 2 | 5 | RESISTOR 2.49K 1x .125w F TEEO+0100 | 24546 | c4-1/8-70-2491-F |
| $\mathrm{R}_{2}$ | 0757-0273 | - | 7 |  | 24546 | ca-1/8-70-3011-F |
| R3 | 0757.0280 | 3 | 24 |  | 24546 | C4-1/8-T0-1001-F |
| R4 | 0757-0273 | 4 |  | RESISTOR 3.01K ix . 125 W W TEE0+-100 | 24546 | C4-1/8-10-3011-F |
| R5 | 0698-3279 | 0 | 30 | RESISTOR 4.99K 1x. 125 NF TCEO*-100 | 24546 | C4-1/8-10-4991-F |
| R6 | 0698.3279 | 0 |  |  | 24546 | C4-1/8-90-4991-F |
| R 9 | 0683-0515 | 0 | 2 | RESIETOR 5.1 5x. 25w FC TCE-400/+500 | 01121 | C85165 |
| R88 | $0083-0515$ $0757-0273$ | 0 |  | RESISTOR 5.1 5x, 25 W FC TCE-400/ 400 | 01121 24546 |  |
| R9 ${ }^{\text {R10 }}$ | -0757-0273 | 4 |  |  | 24546 01121 |  |
| R10 \%\% | 06a3-1525 | - |  |  | 0112. | caises |
| $\mathrm{R}_{11}$ | 0098.3279 | 1 |  | RESISTOR 4.99K 1\%, 125N F PCEO+-100 | 24546 | C4-1/8-90-4991-F |
| R112 R13 | $0683-2025$ $0757-0273$ | 1 |  |  | 01121 24540 | CB2025 $C 4=1 / 8-T 0.3011-F$ |
| R13 R14 | $0757-0273$ 2100.3100 | 2 |  |  | 24546 02111 | C4-1/8-T0.3011-F $43 P 202$ |
| $\mathrm{R}_{15}$ | 0757-0436 | 1 | 1 | RESISTOR 4, 32K 1x , 125 F TCEO+-100 | 24546 | C4-1/8-10-4321-F |
| R10 | 0698-3279 | - |  | RESISTOR 4.99K 1\% . 125 W F TCEO+0.100 | 24546 | $C 4-1 / 8-10-49910 F$ |
| R17 R18 | 0698.3558 $0757-0280$ | 8 | 5 |  | 24546 24540 | $C A-1 / 8-10-40210 F$ $C 4.1 / 8-90-1001-F$ |
| R19 | $2100-3109$ | 2 |  | RESISTOP-PRMR 2K 10X C SIDE=ADJ 17-TRN | 02111 | 43P202 |
| R20 | 0698-4470 | 5 |  | RESISTOR 6.98K 1x, 125W F PEOt-100 | 24546 | C4-1/8-10-6981*F |
| ${ }_{2} 21$ | 0698.4467 | 0 | 1 | RESISTOR $1,05 K$ IX, 125 W TCEO+-100 | 24546 24546 |  |
| R22 R23 2 | $0757-0280$ $0683-1035$ | 3 1 |  |  | 24546 01121 | $\begin{aligned} & C A-1 / 8-10-1001-F \\ & \text { CB1035 } \end{aligned}$ |
| R23 R24 R | $0683-1035$ $0757-0447$ | 1 | 4 |  | 01121 24546 | CB1035 CA-1/8-T0-1622-F |
| R25 | 0757-0447 | 4 |  | RESISTOR 16.2k ix . 125 W F TC=0+0100 | 24546 | C0-1/8-10-1622-F |
| R26 <br> $R 27$ <br> 27 | $0683-8205$ 0698.4307 | $\frac{1}{7}$ | $\frac{1}{2}$ |  RESISTOR 14.3K ix, 125W F TC=0+0100 | 01121 24546 | $\begin{aligned} & C B 8205 \\ & C 4-1 / 8-T 0-1432-F \end{aligned}$ |
| R28 | 0083-2025 | 1 |  | RESISTOR 2K 5x, 25 W FC TCE-4001/700 | 01121 | C82025 |
| R29 | 0757-0273 | 4 |  | RESISTOR 3.01K ix, 125W FCEOt-100 | 24546 | C4-1/8-T0-3011-F |
| R32 | 0698-4123 | 5 | 9 | RESISTOR 409 ix . 125 W F TCOO4-100 | 24546 | C4-1/8-10-499R-F |
| R33 R 35 | 0698.4123 0698.3279 | 5 |  |  | 24546 24546 | $\begin{aligned} & C 4-1 / 8-T 0=499 R-F \\ & C 4=1 / 8-T 0-4991 \circ F \end{aligned}$ |
| R30 | 0698-3223 | 4 | 3 | RESISTOR 1.24k ix, 125w TCEO+0100 | 24546 | C4-1/8-10-1241-F |
| R37 | 0757-0280 | 3 |  | RESISTOR ik ix . 12 SW F PCOOt-100 | 24546 | ca-1/8-10-10010F |
| R38 | 0757-0284 | 7 |  | RESISTOR 150 1\%.125w F TC=040100 | 24546 | C4-1/8-10-151-F |
| :\%R10 STAR VALUES | $\begin{aligned} & 0683-7515 \\ & 0683-1525 \\ & 0757-0159 \end{aligned}$ | 4 4 5 |  | RESISTOR $7505 \% .25 W$ FC TC $=-400 /+600$ RESISTOR 1.5K 5\% . 25 W FC TC $=-400 /+700$ RESISTOR $1 K 1 \%$. 5 W F , TC $=0+-100$ | 01607 01607 28480 | $\begin{aligned} & \text { CB7515 } \\ & \text { CB1525 } \\ & 0757-0159 \end{aligned}$ |

Table 8-5-3. Replaceable Parts (Cont'd).

| Reference Designation | HP Part Number | $\begin{aligned} & \mathbf{C} \\ & \mathbf{D} \end{aligned}$ | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $R 39$ | 0698.4439 | - | 2 | RESIBTOR 3.24K 12 . 125W F TCOOP=100 | 24546 | C4-1/8-10-32410F |
| R40 | 0757-0349 | , | 1 | HESISTOR 22.6K 1x 125W TC=04-100 | 24546 | C4-1/8-10-22620F |
|  | 2100.3354 |  | 2 | RESISTOR-TRMR SOK IOL C AIDE-ADS I-TAN | 28480 | $2100-3354$ |
| R42 | $2100-3273$ | 1 |  | REGIETOR-TRMR 2K $10 x \mathrm{C}$ SIDE-AOJ I-TRN | 28480 24546 | $2100 \cdot 3273$ |
| R43 | 0698.3558 | \% |  | RESIBTOR 4,02K 1\% , 125W F TC=04-100 | 24546 | $C 4-1 / 8-T 0=4021-F$ |
| Ray | 0698.3223 | 4 |  | REPISTOR $1,24 \mathrm{~K}$ 1\% 125 FW F TCOO4-100 | 24546 | C4-1/8-70-1241-F |
| Ras | 0757-0280 | 3 |  | REGIBTOR 1K 1\%. 125 W W TC-10+0100 | 24546 | C4-1/8-T0-10010F |
| R46 | 0698-3548 | 6 | 1 |  | 24546 | C4-1/8-70-732R-F |
| RS3 RSa | $2100-3357$ $0757-0469$ | 0 | 1 |  | 28480 24546 | $\begin{aligned} & 2100-3357 \\ & 64-1 / 8=70-1503-1 \end{aligned}$ |
|  | 0757-0469 | 0 |  | REdstor isok ix , 125N F TCEOPİ0 |  |  |
| R56 | 0698-3279 | 0 |  |  | 24546 | $C a-1 / 8-T 0-4+1-1$ |
| R59 | 0698.3223 | 4 |  | REAIATOR 1.2ak ix 125W F TC=0\%-100 | 24546 | $c 4-1 / 8-10+1241-p$ |
| R58 R60 | $0757-0280$ 0698.4435 | 2 |  |  | 24546 24546 |  |
| R61 | 0698-4456 | 7 | 1 |  | 24546 | C4-1/8ヶT0-549Raf |
| R62 R63 | $0698-3558$ $0757-0284$ | 8 |  |  | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & c 4-1 / 8-T 0=4021 \operatorname{c} \\ & c a-1 / 8-T 0=151-F \end{aligned}$ |
| R64 | 0698.4123 | 5 |  | REBIATOR 499 ix il 125 W F TCE040100 | 24546 | C 4 -1/8-10-499ROF |
| R66 | 0608.4430 | 7 | 2 |  | 24506 | C4.1/8-T0-1911-F |
| R67 | 0683-2025 | 1 |  | RESISTOR 2K 5x .25w Fe TC=-400/4700 | 01121 | C82025 |
| R68 | 0698-3558 | 8 |  | RESISTOR 4.02K 18.125 W F TC=0+-100 | 24546 | C4-1/8-T0-4021-F |
| R69 | 0698-4307 | 7 |  | RESISTOR 14.3K 1\% . 125 W F TC=0+100 | 24546 | C4-1/8-TO-1432-F |
| R70 R71 | $0698-4123$ 2100.335 |  |  | RESISTOR 499 1\% 125 WF TC=0+-100 | 03292 28480 | $\begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-499 \mathrm{R}-\mathrm{F} \\ & 2100-3354 \end{aligned}$ |
| R71 R72 | 2100.3354 0757.0447 | 9 |  | REEIGTOR TRMR SOK RESISTOR 16.2 K I | 28480 24546 | 2100-33S4 $C 4-1 / 8-10-1622-F$ |
| R73 | 0757-0447 | 4 |  |  | 24546 | c 4 -1/8-10-1622 - |
| R7a | 0757-0284 | 7 |  | RESIATOR 150 1\% . 125 w F TCOO4-100 | $24506$ |  |
| R100 R101 | 0683-1005 | 5 |  |  | 01121 01121 | C81005 <br> CB1005 |
| R101 R102 R10 | $0683-1005$ $0757-0280$ | 5 |  |  | 01121 24546 | CB1005 C4-1/8-50-1001 F\% |
| R104 | 0698.4435 | 2 |  | RESISTOR 2.a9K ix. 125 W F TC=04-100 | 24546 | C401/8-T0-2491-F |
| R201 R 202 R 202 | 0698.0063 2100.3273 | 4 | 1 |  | $91637$ | CHF-1/8-71-5231-F $2100=1271$ |
| R202 R203 20, | 2100.3213 0698.3447 | a |  | RESISTOR-TRMR 2K 10K C SIOE-AOJ 1-TRN RESIETOR $4221 \%, 125 \mathrm{~F}$ F TE=04-100 | 28480 24546 | $\begin{aligned} & 2100-3273 \\ & C 4-1 / 8-10=422 R-F \end{aligned}$ |
| R20a | 0698.3153 | $\bigcirc$ | 1 | RESISTOR 3.83k 1\% .125w Ferot-100 | 24546 | C4-1/8-T0-3631-F |
| R205 | 0757-0284 | 7 |  | RESISTOR 150 1x , 125 W F TC=0+0100 | 24546 | C4-1/8-70-151-F |
| ${ }_{2} 206$ | 0698-4020 | $!$ |  | RESISTOR 9.53K ix . 125 W F TCOO*-100 | 24546 | $C 4-1 / 8+10-9531=F$ |
| R207 R208 | 0698.3270 0698.4439 | 0 |  |  | 24546 24546 | $C 4-1 / 8-T 0-44910 F$ $C 4-1 / 8-10-3241-F$ |
| R208 R209 | 0698.4439 $0757-0284$ | 6 |  |  | 24546 24546 | $C 4-1 / 8-10-32410 \%$ $C 4-1 / 8-10-1510 \%$ |
| R210 | 0757.0260 | 3 |  | RESİTOR IK ix. $i 25 \mathrm{~W}$ F iC $=0+0100$ | 24546 | C4-1/8-10-10010F |
| R211 | 0757-0442 | 9 |  |  | 24546 | C4-1/8-10-1002-F |
| R21 R213 R214 | $0757-0280$ $0757-0442$ | 3 |  |  | 24546 24546 | $\begin{aligned} & \operatorname{cac}=1 / 8-T 0=1001-F \\ & \operatorname{ca-1/8-T0-1002-F} \end{aligned}$ |
| R213 R214 | $0757-0442$ $0757-0284$ | 9 |  |  | 24546 24546 | $C A-1 / 8-10-1002 * F$ $c a-1 / 8-10-151-F$ |
| R215 | 0698.3279 | 0 |  | RESISTOR 4.99K IX . 125 W F TCEO+-100 | 24546 | C4-1/8-10-4991 ${ }^{\text {F }}$ |
| R216 | 0698-3279 | 0 |  | REBISTOR 4.90k 1\% 125 W F TE00+0100 | 24546 |  |
| R220 | $0757-0442$ 0698.3270 | 9 |  |  | 24546 24546 | $C a-1 / 8-T 0-1002-F$ $C a-1 / 8-70-49910 F$ |
| R221 | 0698.3270 | 0 |  | REBIATOR 4.99\% 1x . 125w F TEsotol00 | 24546 | Ca-1/8-10-49910F |
| RPI05 | 1810.0279 | 5 |  | NETWORK-RES 10 -PIN-SIP /I-PIN-SPCG | 11236 | 750-101-R4, 7k |
| RP106 | $1810-0279$ | 5 |  | NETMORK-RES $10-P I N-B I P \quad 1-P I N=S P C G$ | 11236 | 750-101-R4,7K |
| RP107 | 181000270 | 5 |  | NETWORK*RES 10-PIN-SIP :I PIIN-SPCG | 11236 | 750-101-R4.7K |
| ${ }_{4}$ | 1820-0500 | 0 | $\frac{1}{7}$ | If CONY 10-B-D/A 16-DIP-C | 03285 34371 | $\begin{aligned} & \text { M0561JD } \\ & \text { MA2-2605.5 } \end{aligned}$ |
| U2 | $1826-0413$ 1826.0413 | 2 | 7 | IC OP AMP $10-90$ IC OP AMP 10.90 | 34371 34371 | M12-2605-5 $H 12-2605-5$ |
| U4 | 1826-0021 | 8 | 6 | IC OP AMP 10.99 | 27014 | LM310H |
| US | 1826-0302 | , | 1 | IC OP AMP 10-99 | 04713 | MC174186G |
| U6 | 1826-0413 | 2 |  | IC OP AMP 10.99 | 34371 | HA2-2605-5 |
| 47 | 1826.0188 | 8 | 5 | IC 1408 CONV 1600IP-C | 04713 27014 | $\text { MC } 1408 \mathrm{~L}-8$ |
| U88 | $1826-0021$ $1826-0026$ | 8 3 |  | IC OP AMP TO-99 ic 311 COMPARATOR 70.99 | 27014 04713 | $\begin{aligned} & L M 31 O H \\ & M L M 3116 \end{aligned}$ |
| U10 | 1826-0188 | 8 |  | IC 1408 CONV $16=01 p=C$ | 04713 | MC1408L-8 |
| 41 | 1826-0183 | 8 |  | If 1408 CONV $16=$ DIP-C | 04713 | $\text { MC } 1408 \mathrm{~L}=8$ |
| $U 12$ $U 13$ | $1826=0021$ $1826-0188$ | 8 |  | IC DP AMP 10-90 IC 1408 CONY $16-01 P=C$ | 27014 04713 | LM310N <br> MC14086-8 |
| 414 | 1826-0413 | 2 |  | 1 C OP AMP TO-99 | 34371 | HA2-2605.5 |
| $U_{15}$ | 1820-1941 | 1 | 2 | 1c SW ANALOG | 27014 | LFI3201N |
| $\mathrm{U}_{16}$ | 1826-0021 | 8 |  | 1 COP AMP T0.99 | 27014 | LM310M |
| U17 $U 18$ | $1820-1941$ $1826-0021$ | $1$ |  | IC SW ANALOG | 27014 <br> 27014 | LFI3201N |
| 118 18 | $1826-0021$ | $18$ |  | IC OP AMP 90-99 | $\begin{aligned} & 27014 \\ & 27014 \end{aligned}$ | LM310H |
| 119 $U_{21}$ | $1826-0021$ $1820-1197$ | 8 |  |  | 27014 01295 | LM310H 3N74LSOON |
| U23 | 1826-0026 | 3 |  | IC 311 COMPARATOR TO-99 | 04713 | MLM3116 |
| 4201 | 1826-0557 | 5 | 1 | IC OP AMP GP QUAD 14-D1P-C | 03406 | LM348J |
| U202 | 1820.1196 | \% |  | IC FF TTL LS D-TYPE PDSOEDGE-TRIG COM | 01295 | ON74LS174N |
| U203 | 1820-1196 | 8 |  | IC FF TTL LS D-TYPE PDS-EDGE-TRIG COM | 01295 | 8N74L8174N |
| U204 | 1820-1196 | 8 |  | IC FF TTL LE D-TYPE POS-EDGE-TRIG COM | 01295 | 3N74L8174N |

Table 8-5-3. Replaceable Parts (Cont'd).

| Reference Designation | HP Part Number | \|c| | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & 4205 \\ & \hline \end{aligned}$ | 1820-1106 <br> 826-0356 <br> 1826-0356 <br> $4040-0748$ <br> $4040-0749$ $6460-0080$ $\qquad$ | 23 |  | IC "Fitl Ls d-tyPe pos-Edeg-trig com Sc IC IS 350 30 <br>  <br> Extactoop-pt boabo glk polve CLUGGOLE RL-HD FOR , 1 AS-D-HOLE TEE | $\begin{aligned} & 01295 \\ & 03285 \\ & 03285 \\ & \\ & \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | SN74L8174N <br> AD7530JD <br> AD75300D <br> $4040-0748$ <br> $4040=0749$ $6940-0080$ |
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# SERVICE GROUP 6 HIGH VOLTAGE SECTION 

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# HIGH VOLTAGE SECTION <br> SERVICE GROUP 6 

## 8-6.1. INTRODUCTION.

8-6-2. The High Voltage Section contains the necessary circuits to provide all of the CRT drive voltages. While most of the circuits may be found on the A13 board (schematics L and M ), the drive voltages of over +150 V are supplied by the $\mathrm{M}(\mathrm{A} 65)$ high voltage rectifier circuit, located beneath the rear of the CRT. Inputs to the L(A13) board are low dc levels and TTL blanking signals which are produced in the Display Control section.

## 8-6-3. GENERAL INFORMATION.

8-6-4. Use extreme caution when performing any type of maintenance or adjustment in this area. Voltages of up to +18 KV are present on circuit components, even after the instrument is turned OFF. High voltage measurements are critical and should be made with the equipment suggested in Adjustment (Section V). Incorrect adjustment of CRT voltages may lead to a shortened CRT life.

## WARNING

Dangerous voltages (up to +18 KV ) capable of causing death are present in circuits even when the instrument is turned OFF. Use extreme caution when working in this area.

### 8.6.5. HIGH VOLTAGE SECTION THEORY.

8.6-6. The $X$ Axis and $Y$ Axis Amplifiers L(A13).

8-6-7. The $\mathbf{X}$ and Y Axis Amplifiers are identical, therefore, only the $\mathbf{X}$ Axis Amplifier is explained in the following paragraphs.

8-6-8. The X Axis input signal causes the percentage of current in the Differential Current Amplifier to vary between Q14A and Q14B. The current is supplied by a constant current source Q15. The variable resistor R54 sets the X Axis gain and the variable resistor R60 sets the X Axis position.

8-6-9. The current from the collector of Q14A is converted by the X1 Deflection Amplifier to a voltage between +8 Vdc and +90 Vdc which is used to drive the X 1 deflection plate of the display CRT. R70 and C29 form a feedback network to provide gain stability. Note that each deflection amp has essentially zero input impedance.

## 8-6.10. The Z Axis Amplifier.

8-6-11. The Z Axis Amplifier controls the intensity of the display by supplying a bias signal to the High Voltage Rectifier A65 which in turn operates the control grid of the display CRT.

8-6-12. The Z Axis input has a voltage proportional to the line length in graphics mode and a fixed dc voltage in the alpha mode each multiplied by the position of the front panel pot. If the gain of $U 1$ is $\frac{R 12}{R_{F}}$ where the value $R_{F}$ is the resistance of the FET Q1B. Q220,221, and Q1A generate the gate voltage necessary to cause $\mathrm{R}_{\mathrm{F}}$ to be proportional to the intensity pot. Q202 is a constant current source.

8-6-13. To produce the character matrix dots in the alpha mode, the H BLANK line is pulsed causing the current Switch (A2 and Q3) to blank the display between dots. The current from the collector of Q3 is applied to the Grid Drive Amplifier which supplies a voltage to the high voltage rectifier.

8-6-14. The CRT control grid voltage is produced in the High Voltage Rectifier by a voltage shifting circuit which references it to the -4000 Vdc cathode voltage. The amount of maximum intensity is determined by the setting of the Intensity Limit control A13R109. The Z Gate input from A13 modulates the dc grid voltage to produce variations in display intensity.

## 8-6-15. The High Voltage Oscillator and High Voltage Rectifier M(A13,A65).

8-6-16. Transistor A13Q13 and transformer A66T1 together form a class C oscillator stimulating the primary of A66T1 with a 20 to 30 kHz signal. The highly stepped up signal from the secondary of A66T1 is rectified by A65CR1 and filtered by the Pi network filter consisting of $\mathrm{A} 65 \mathrm{C} 1, \mathrm{~A} 65 \mathrm{C} 2$, and A 65 R 2 providing a -4000 Vdc cathode voltage. This voltage is sampled by the feedback network consisting of A65C3, A65R4, A12R46 and A13R44. This feedback signal is applied to IC regulator A13U2 regulating the dc level of the base winding of A66T1 causing A13Q13 to maintain the cathode voltage at -4000 Vdc (see Figure 8-6-1).


Figure 8-6-1. HV Oscillator Block Diagram.

8-6-17. The focus voltage is determined by a resistor string with two variable resistors. The fine adjustment is varied by the Front Panel Focus control. Gross adjustment is provided by A65R13.

8-6-18. A tap off from the secondary output of A66T1 is applied to a voltage sixtupler which increases the voltage to +18000 Vdc for the post accelerator.

## 8-6-19. The Flood Gun.

8-6-20. The Flood Gun circuit supplies an additional source of electrons from a second filament in the tube, which cause the phosphor of the CRT to radiate illuminating the graticule. A13R105 adjusts the uniformity of the Flood Gun.

## 8-6-21. The +100 Regulator.

8-6-22. A reference signal is generated by A13U3 at pin 4 and is applied to the non-inverting input pin 3 through a resistor divider network consiting of A13R36, A13R37, and A13R38. The output of the Regulator is sensed and compared to the reference by resistors A13R40 and A14R39. The result of the comparison is applied to A13U3 pin 2 which drives the pass transistor A13Q11 through zener diode A13CR11. A13R41, A13R42 and A13R43 act as a foldback current sensing network and supply a voltage between pin 10 and 1 which limits the drive to A13Q11 (see Figure 8-6-2).

8-6-23. A13Q12, A13CR10, and A13R35 are connected to provide the 13 V relative positive and negative Vcc inputs to A13U3. See Figure 8-6-2 for a simplified representation. CR30 acts as a clamp for the +100 V output to protect the display from regulator failure.


Figure 8-6-2. +100V Regulator.

## 8-6.24. TROUBLESHOOTING THE HIGH VOLTAGE OSCILLATOR.

8-6-25. Because the high voltage oscillator incorporates a closed loop feedback circuit, ac signal levels may vary between instruments due to the differences in high voltage settings for the CRT. One way of breaking the loop, which permits testing under static conditions, is to remove the transistor mounting screws from A13Q13. This opens the circuit at the collector of Q13 which disables the oscillator. Now, characteristic dc levels may be measured at various parts of the circuit, which should aid in determining the malfunction. This technique is useful even if the circuit was operating, but failed to produce the proper high voltage levels. In this case, areas of concern would involve leaky capacitors or zener diodes.

8-6-26. If this procedure does not indicate a malfunctioning component, then the problem area may exist inside the high voltage rectifier box (A65). Troubleshooting in the high voltage recitifier box is not recommended because of the danger from lethal voltages (as high as +18 KV ) which remain on circuit components even after the instrument is turned off. Therefore, the high voltage rectifier box should be replaced as a unit if any of the components within are suspected or known to be defective.

8-6-27. Perform the following procedure.
a. Set the LINE switch to OFF.
b. Remove the top instrument cover and the plastic shield scovering the A13 board.
c. Remove the two transistor mounting screws from A13Q13.
d. Set the LINE switch to ON.
e. Make dc voltage measurements as indicated in Figure 8-6-3.
f. Set the LINE switch to OFF.
g. If all the voltages given in Figure 8-6-3 are correct, it is still possible that U 2 or Q 13 is defective.
h. If replacement of all indicated defective parts does not result in an operating oscillator, then replace the High Voltage Rectifier.
i. Once the High Voltage Oscillator is operational, perform the high voltage adjustment given in Section V.


Figure 8-6-3. DC Measurements In The High Voltage Oscillator.

## A13 INPUT ANALOG CHECKS

To perform the following analog checks, set the TEST switch on the top of the A9 board to TEST. All of the signal points are accessible through holes provided in the A13 plastic cover.


Analog Signal Points

$X$-axis input to $A 13$
Internal trigger
$0.02 \mathrm{v} / \mathrm{div} ; \times 10$ probe
Ovdc 2.5 cm from bottom
2ms/div sweep

(3) Z-axis input to A13

Internal trigger
$0.01 \mathrm{v} / \mathrm{div}$; X 10 probe
Ovdc 2 cm from bottom
2ms/div sweep

(2) Y -axis input to A 13

Internal trigger $0.02 \mathrm{v} / \mathrm{div}$; $\times 10$ probe Ovdc 2.5 cm from bottom $2 \mathrm{~ms} /$ div sweep

(4) High blank
$0.02 \mathrm{v} / \mathrm{div} ; \mathrm{X} 10$ probe Ovdc 2.5 cm from bottom $2 \mathrm{~ms} /$ div sweep int. trigger

Figure 8-6-4. $\mathrm{X}, \mathrm{Y}$, and Z Inputs To A13.





465
Typical Resistance Measures of XFMR out of CKT.

(1) HV Oscillator TP

Internal trigger
$0.5 \mathrm{v} / \mathrm{div}$
Ovdc 1 cm from bottom $\times 10$ probe 1 Ousec/div

| Pins |  |
| :---: | :---: |
| 3 to | OHMS |
| 5 to | 6 |
| 7 to 8 | $.01 \Omega$ |
| 9 to | .080 |
| 9 to | 2 |
| 9 to 10 | 2500 |





Table 8-6-1. Replaceable Parts.

| Reference Designation | HP Part Number | C | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 113 | 03502-66513 | 3 | 1 | PC AssEmaly, $X=Y$-2- AMPLIFIER | 28480 | 03502-66513 |
| ${ }_{c} 1$ | 0150-0012 | 3 | 19 | CAPACITOR-FXD .01UF ${ }^{\text {c-20x }}$ 1KVDC CER | 04200 | CO23A102J103MS38 |
| $\mathrm{C}_{2}$ | 0150-0012 | 3 |  | CAPACITORAFXD O1UF + -20x 1KVDC CER | 04200 | C023A102J103MS 38 |
| ${ }^{\text {c }} 3$ | 0160-3622 | 8 |  | CAPACITOR-FXD. 14 F \$80-20x 100VOC CER | 28480 | 0160-3622 |
| ${ }^{\text {cas }}$ | $0160-3622$ | 8 |  | CAPACITOR-FXD, 1 UF +80-20\% $100 Y$ OC CER | 28480 | 0100-3622 |
| C5 | 0160-2241 | 5 | 1 | CAPACITOR-FXD 2.2PF +0.25PF SOOVDC CER | 28480 | 0160-2241 |
| ${ }_{6} 6$ | 018000269 | 5 | 2 | CAPACITOR-FXD 1UF\$50-10x 150VDC AL | 56289 | 30010561508A2 |
| ${ }^{C 7}$ | $0160-2109$ 0160.3622 | 2 |  |  | 28480 28480 | $0160-2199$ $0160-3622$ |
| Ca Ca | $0160-3622$ $0180-0197$ | 8 | 14 |  | 28480 50289 | $0160-3622$ $1500225 \times 902042$ |
| C10 | 0160-3622 | 8 |  | CAPACITOR -FXD.IUF +BO-20x loovoc Cer | 28480 | 0160-3622 |
| $\mathrm{c}_{11}$ $\mathrm{c}_{12}$ | $0160-3622$ $0150-0012$ | 8 |  | CAPACITOR-FXD . IUF 80020 O IOOVDC CER CAPACITOR-FXD .01UF *-20XIKVCD CER | 28480 04200 | $\begin{aligned} & 0160-3622 \\ & \text { CO23A102 } \end{aligned}$ |
| c12 $\mathrm{c}_{13}$ | $0150-0012$ $0150-0012$ | 3 3 |  |  | - 04200 | C023A102J103MS38 |
| ${ }_{6} 14$ | 0180-0269 | 5 |  | CAPACITOR-FXO IUF\$50-10X 150 VDC AL | 56289 | 30010561508A2 |
| C15 | 0150-0012 | 3 |  | CAPACITOR -FXO .01UF +-20x 1KVCD CER | 04200 | C023A102J103MS38 |
| $C 16$ c17 | 0180.0197 0160.2237 | 8 |  | CAPACITOR-FXD $2.2 U F+=10 x$ 20VDC TA | 56289 28080 | $1500225 \times 902042$ |
| $\mathrm{C}_{1} 17$ C 18 | $0160-2237$ $0160-3456$ | 9 | 5 |  | 28080 28480 | $\begin{aligned} & 0160-2237 \\ & 0160=3456 \end{aligned}$ |
| ${ }^{19}$ | 0180-0089 | 7 | 2 | CAPACITOR-FXD 10UF+50-10X 150 VDC AL | 56289 | $300100 \mathrm{~F}_{130002}$ |
| c20 | 0160-3468 | 0 | 1 | CAPACITOR-FXD .12UF tolox BovDC POLYE | 28980 | 0160-3468 |
| ${ }_{4} 21$ | 0160.3622 | 8 |  |  | 28480 | $0160=3622$ |
| $C 22$ $C 23$ | $0160-0166$ $0180-0141$ | 9 | 1 |  | 28480 56289 | $\begin{aligned} & 016000166 \\ & 3005066050002 \end{aligned}$ |
| C24 | 018000197 | 8 |  | CAPACITOR-FXD 2, 2UF+C10X 2OVOC TA | 56289 | $1500225 \times 902042$ |
| ${ }^{6} 25$ | 0150-0012 | 3 |  | CAPACITOR-FXD .01UF +E20K 1KVDC CER | 04200 | CO23A102J103MS38 |
| ${ }^{C} 26$ | 0160.4676 | 4 |  |  | 28480 28460 | $0160-4676$ 016004676 |
| C27 C 28 | $0160=4676$ 018000197 | 4 |  |  | 28480 56289 | $0160-4676$ $1500225 \times 902042$ |
| C29 | 0160-223 | $\bigcirc$ |  | CAPACITOR-FXO 1,2PF + - 25PF SOOVDC CER | 28480 | 0160-2237 |
| C30 | 0150-0012 | 3 |  | CAPACITORaFXD .01UF +-20x 1KVDC CER | 04200 | CO23A102J103MS38 |
| C31 | 0150-0012 | 3 |  | CAPACITOR-FXD . O1UF +azox 1KVDC CER | 04200 | CO23A102J103MS 38 |
| ${ }_{6} 32$ | 0150-0012 |  |  | CAPACITOR-FXD 01UF ${ }^{\text {c-20x }}$ IKVDC CER | 04200 | C023A102J103MS 38 |
| $C 33$ $C 34$ $C 3$ | $0180-0197$ $0160-2237$ | 8 |  | CAPACITOR-FXD $2.2 U F+=10 \mathrm{X}$ 20VDC ${ }^{\text {CA }}$ | 56289 28480 | $1500225 \times 902042$ $0160-2237$ |
| C35 | 0180-0107 | 8 |  | CAPACIYOR-FXD 2, 2UF*-10\% 2OVDC TA | 56289 | $1500225 \times 902042$ |
| ${ }_{6} 36$ | 0150-0012 | 3 |  | CAPACITORRFXO .01UF +-20\% 1KVDC CER | 04200 | CO23A102J103MS38 |
| C37 C38 | 0150-0012 | 3 3 3 |  |  | 04200 04200 | CO23A102J103MS 38 CO23A102J103MS |
| $C 38$ C 30 | $0150-0012$ $0180-0197$ | 3 8 |  |  | 04200 56289 | CO23A102J103MS 38 $1500225 \times 902042$ |
| cad | 0160.2237 | 9 |  | CAPACITOR-FXD 1.2PF \$0.25PF SOOVDC CER | 28480 | 0160-2237 |
| ${ }^{C 4} 1$ | 0150-0012 | 3 |  | CAPACITOR-FXD .01UF +-20x 1KVDC CER | 04200 | CO23A102J103MS 38 |
| $\mathrm{Ca}_{2}$ | 0150-0012 | 3 |  |  | 04200 04200 | CO23A102J103MS 38 |
| C43 C44 | $0150-0012$ 018000197 | 3 |  |  | 04200 56289 | CO23A102J103MS $1500223 \times 9020 A 2$ |
| C45 | 0160-2237 | - |  |  | 28480 | 016002237 |
| C46 647 | $0180=0089$ $0160=3622$ | 7 |  | CAPACITORAFXD 10UF $\$ 50.10 \mathrm{X}$ 150VDC AL CAPACITOR-FXD •JUF * 80-20X loovoc CER | 56289 28480 | $\begin{aligned} & 300106 \% 150002 \\ & 0160-3622 \end{aligned}$ |
| C48 | 0160-3622 | 8 |  | CAPACITDR-FXO .1UF + BO-20x loovoc CER | 28400 | 0160-3622 |
| Cas | 0160-3622 | 8 |  | CAPACITOR-FXD .1UF $\boldsymbol{8} 0$-20x 100 VDC CER | 28480 | 0160-3622 |
| C50 | 0160-3622 | 8 |  | CAPACITOR OFXD , 1UF +BO-20X 100 VDC CER | 28480 | 0160-3622 |
| ${ }_{5} 51$ | 0150-0012 | 3 |  | CAPACITOR-FXD .01UF + -20x 1 KVDC CER | 04200 | CO23A102, 103 MS 38 |
| C52 | 0160-3622 | 6 |  | CAPACITOR-FXO .1UF $+80-20 x$ L 100 VDC CER | 28480 | $0160-3622$ |
| 653 | 0160-3622 | 8 |  |  | 28480 | 0160.3622 |
| 654 $C 55$ | $0150-0012$ $0160-0159$ | 0 | 1 |  | 04200 28480 | $\begin{aligned} & \text { Co23A102J103MS38 } \\ & 0160=015 \theta \end{aligned}$ |
| C56 | 0180-0197 | 8 |  | CAPACITOR=FXD 2,2UF¢-10x 20VDC TA | 56289 | 1500225x902042 |
| C51 | 0180-0197 | 8 |  | CAPACITOR-FXD 2,2UF+-10X 2OVDC TA | 56289 | $1500225 \times 902042$ |
| C58 | 0180-0197 | - |  | CAPACITOR-FXD $2,2 \mathrm{LFF-10x} 20 \mathrm{VDC}$ TA | 56289 | $1300225 \times 902012$ |
| 659 660 | $0180-0197$ $0160-3622$ | 8 |  |  | 56289 28480 | $\begin{aligned} & 1500225 \times 902012 \\ & 0160=1622 \end{aligned}$ |
| ${ }_{6} 61$ | 0180-0197 | 8 |  | CAPACITOR-FXO 2,2UF*-10x 20VDC TA | 56289 | $1500225 \times 902042$ |
| ${ }_{6} 65$ | 0160.3622 | 8 |  | CAPACITOR-FXO IUF *BO-20x 100 VOC CER | 28480 | $0160-3622$ |
| c 201 | 014000193 | 2 |  | CAPACITOR-FXO 130 PF \$-5x 300VOC MICA | 72136 | DM15F131J0300WVICR |
| $\begin{aligned} & C_{202}^{202} \\ & c_{203} \end{aligned}$ | $0140-0195$ $0160-3622$ | 2 |  | CAPACITDRDFXD 130 PF +05\% 300VOC MICA CAPACITOR OFXD .1UF $8 \mathbf{8 0} 20 \mathrm{X}$ loovDC CER | 72136 | DMISFI31J0300WVICR $0160-3622$ |
| $\begin{aligned} & c 204 \\ & c 205 \end{aligned}$ | $\begin{aligned} & 0160-3622 \\ & 0160-3622 \end{aligned}$ | 8 |  | CAPACITOR-FXD . 1 UF * $80-20 \mathrm{~K}$ loovDC CER CAPAEITOR-FXO .1UF *BO-20X LOOVDC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0160-1622 \\ & 0160=3622 \end{aligned}$ |
| $\begin{aligned} & C R_{1} \\ & C R 2 \end{aligned}$ | 1902-3237 | 7 | 3 |  <br> OIODEEINR 36.3V 5K OO-7 PDE.4W TCE\$,001X | 28400 28480 | $1902-3237$ $1902-3311$ |
| $\mathrm{CR}^{2}$ | 1902-3311 | 7 |  | DIODE-2NR 38.3V 5\% DO-7 PDE.4W TCE4.081x | 28480 | 190203311 |
| CR4 | 1902-0049 | 2 | 13 | DIODEEINR 6.19V 5X DO-7 PD= 4W TCE中,022X | 28480 | 1902-0049 |
| CR5 | 1902-3237 | 6 |  | DIODE-2NR 20 V 54 DO-7 PD..4m TC-4.013\% | 28480 | 1902-3237 |

Table 8-6-1. Replaceable Parts (Cont'd).

| Reference Designation | HP Part <br> Number | C | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CR6 | 1901-0096 | 7 | 1 | OIODE-SWITCHING L20V SOMA 100 NS | 28480 | 1901 -0096 |
| CR | 1901.0029 | 6 | 1 | DIODE-PWR RECT 600V 750 MA DO-29 | 28480 | 190100029 |
| CRa | 1902-0049 | 2 |  | OIODE-2NR 6.19V 5X DO-7 PDE.4W TCE4.022X | 28480 | 1902-0049 |
| CRio | 1902-3193 | 3 | 1 | DICDE-2NR 13.3V 5\% D0-7 PDE.4W TCE4.059x | 28480 | 1902-3193 |
| CR11 | 1902-0049 | 2 |  | O100E-2NR 6.19V 5\% D0.7 PDE, 4W TCE4.022\% | 28480 | 1902-0049 |
| $\mathrm{CR}_{\mathrm{R} 13}$ | 1902-3311 | 7 |  | OIODE-2NR 38,3V 5x Do-7 PDE, 4w TCE4.081\% | 28480 | 1902-3311 |
| CR14 | 1902-0049 | 2 |  | DIODE-2NR 6.19V 5\% 00-7 PDE.4W TCE4.022\% | 28480 | 190200049 |
| CR15 | 1902-0049 | 2 |  | OIOOE-2NR 6.19V 5\% DO-7 PDE,4W TCE4.022\% | 28480 | 1902-0049 |
| CR16 | 1901-0040 | $!$ |  | DIODESNITCHING JOV SOMA 2NS OO-35 | 28480 | 1901 -0040 |
| CR17 | 1901-0040 | 1 |  | OIODEAWITCHINE 3OV 50MA $2 N S$ Do-35 | 28480 | 190100040 |
| CR18 | 1901-0029 | 6 |  | DIODEAPWR RECY G00V $750 \mathrm{ma} \mathrm{D0-29}$ | 28480 | 1901-0029 |
| CR19 | 1901-0029 | 6 |  | DIODEAPWR RECT GOOV 750MA DO-29 | 28480 | $1901-0029$ |
| CR20 | $1902-0049$ | $?$ |  | DIOOE-2NR 6.19V 5\% DO-7 PDE, 4W TCEE.022\% | 28480 | 1902.0049 |
| CR21 | $1902-0049$ $1902-0049$ | 2 |  |  | 28480 28480 | 190200049 $1902-0049$ |
| CR22 | 1902-0049 | 2 |  | DIDDE-2NR 6, 19V 5\% DOeT PDE,4w TCE4.022\% | 28480 | 1902-0049 |
| Cr 23 CR24 | $1902-0049$ $1902-0049$ | 2 |  |  | 28480 28480 | $\begin{aligned} & 1902-0049 \\ & 1902-0049 \end{aligned}$ |
| CR24 CR25 | $1902-0049$ $1902-0049$ | 2 |  |  | 28480 28480 | 190200049 $1902-0049$ |
| CR26 | 1902-0244 | 9 | 1 | DIODE-2NR 30,1V 5\% DO-15 PDiw TCEP0075\% | 28480 | 1902 -0244 |
| CR27 | 1902-3302 | 6 | 1 |  | 28480 | 1902-3302 |
| CR28 | 1901-0040 | 1 |  | DIODE-8WITCHING JOV 50MA $2 N 8$ OD-35 | 28480 | 1901-0040 |
| CR29 | 1901-0029 | 6 |  |  | 28480 | 190100029 |
| CR30 CR31 | 190200934 190100040 | 4 | 1 |  | 04713 20480 | 1053808 190100040 |
| crezo | 1901-0518 | 8 |  | DIODE-SCHOTTKY | 28480 | 1901-0518 |
| $\mathrm{FFCl}_{\text {Fla, }}$ | $\begin{aligned} & 211000269 \\ & 2110=0339 \end{aligned}$ | 5 | 1 |  | 28480 28480 | $\begin{aligned} & 2110=0269 \\ & 2110=0339 \end{aligned}$ |
| L 19 L2 | $9140-0171$ $91000-1641$ | 3 0 | $!$ | CDIL-MLD 4OUM 10\% 0=20. $2960 \times .968$ GONOM COIL-MLD 240 UH 5\% Q.65 . $1550 \times 375 L 60$ NOM | 28480 28480 | $\begin{aligned} & 9140=0171 \\ & 9100=1641 \end{aligned}$ |
| Q1 | 1855.0308 | 5 |  | TRANSIBTOR-JFET DUAL N-CHAN D=MDDE SI | 28480 | 1855.0308 |
| 02 | 1854.0071 | 7 |  | TRANSISTOR NPN SI PDESOOMW FTE200MHZ | 28480 | 1854.0071 |
| 03 | 1854-0071 | 7 |  | TRANSISTDR NPN SI PDE300Mm FFE200MHZ | 28480 | 185400071 |
| 04 | 1854-0475 | 2 |  | TRANBISTOR-DUAL NPN POE 750 Mm ( 20 mL | 28480 28480 | 1854.0475 185300036 |
| 0.5 | 1853 -0036 | 2 | 7 | TRANSISTOR PNP SI PDE310Mm Fire2somhz | 28480 | 1853.0036 |
| 0. 08 08 | $1854-0071$ $1853-0232$ | 7 |  |  | 28480 26480 | $1854-0071$ $1853-0232$ |
| 08 08 08 | $1853-0232$ $1854-0419$ | 7 | 5 | TRANSISTOR PNP OI TO-39 PDEIW FTE200MHZ | 28480 28480 2848 | $1853-0232$ 185400419 |
| 09 | 1854.0071 | 7 |  | TRANSISTOR NPN SI PDE300Mm FTE 200 MHZ | 28480 | 1854.0071 |
| 010 | 185400234 12050012 | 0 | 2 | TRANSISTOR NPN $2 N 3440$ SI TO-5 PDEIW HEAT SINK TO-5/P0-39-PKG | 01928 28480 | $\begin{aligned} & 2 N 3440 \\ & 120500012 \end{aligned}$ |
| 011 | $\begin{aligned} & 1854-0237 \\ & 1205-0347 \end{aligned}$ | 7 | 2 | TRANSISTOR NPN SI TO-66 PDE2OW FTEIOMHZ MEAT SINK SGL TO-66-PKG | 28480 28480 | $\begin{aligned} & 1854-0237 \\ & 1205=0347 \end{aligned}$ |
| Q12 | 1854 -0234 | 4 |  | TRANSISPOR NPN 2 N3440 SI TO-5 POEIW | 01928 | 2 N 3440 |
|  | 1205-0011 | 0 |  | MEAT SINK TO-5/TD-39-PKG | 28480 | 1205.0011 |
| 013 | $\begin{aligned} & 1854=0476 \\ & 1205=0347 \end{aligned}$ | 5 | 1 | PRANBISTOR NPN $2 N 3879$ SI PO-66 PDE35w MEAT BINK BGL TO-66-PKG | 01928 28480 | $\begin{aligned} & 2 N 3879 \\ & 1205-0347 \end{aligned}$ |
| 014 | 1854-0475 | 5 |  | TRANSISTOR-DUAL NPN PDEF50mm | 28480 | 1854.0475 |
| 015 | 1854.0071 | 7 |  | TRANSISTDR NPN SI PDE300MW FTE200MHZ | 28480 | 185400071 |
| 016 | 1853.0036 | 2 |  | TRANSIATOR PNP SI POC310MW FTE2SOMHZ | 28480 | 1853.0036 |
| 017 | 1854.0071 | 7 |  | TRANSISTOR NPN SI PDE300mm FTE200MHz | 28480 | 1854.0071 |
| 0.8 | 1853-0232 | 0 |  | TRANSISTOR PNP SI TD-39 PDEIW FTE200MHZ | 28480 | 1853-0232 |
| 019 | 1854.0419 $1853-0036$ | 7 |  | TRANBISTOR NPN AI PO-39 PDEIW FTE200MHZ TRANSIAYOR PNP SI PDE310Mm FTE250MHz | 28480 28480 | 1854.0419 1853.0036 |
| 020 021 | $1853-0036$ 185440071 | 2 |  | TRANSISTOR PNP SI PDE310Mm FTE 250 MHz TRANSISTOR NPN SI PDE300Mm Fia SROOMHZ | 28480 28480 | 185300036 1854.0071 |
| 022 | 1853-0232 | 0 |  | TRANSISTOR PNP 8I TO-39 PDEIW FTE200MHz | 28480 | 1853.0232 |
| 023 | 1854-0419 | 7 |  | TRANSISTOR NPN SI TO-30 PDEIW FTE200MHZ | 28480 | 1854.0419 |
| 029 | 1854-0475 | 5 |  | TRANSISTOR-DUAL NPN PDE 750 MW | 28480 | 1854.0475 |
| 025 | 1854-0071 | 7 |  | TRANSISTDR NPN SI PDE300MW FTEZ00MHZ | 28480 28480 | 1854.0071 |
| 026 | 1853.0036 | $?$ |  | TRANBISTOR PNP SI PDE310MW FTa 250 MHZ | 28480 28480 | $1853-0036$ 1854.0071 |
| 027 028 | $1854-0071$ 18530232 | 7 |  | TRANSISTDR NPN SI PDE300MW FTEZOOMHZ TRANSISTOR PNP BI TD-30 PDEIW FTE200MHZ | 28480 28480 | 1854.0071 1853.0232 |
| 029 | 1854.0419 | 7 |  | TRANSISTOR NPN SI TO-39 PDEIW FTE200MMZ | 28480 | 1854.0419 |
| 030 | 185300036 | $?$ |  | TRANSISTOR PNP SI PDe 310 MW FTE250MHz | 28480 | 1853-0036 |
| 031 | 1854-0071 | 7 |  | PRANBISTOR NPN SI PDE300MW FTEzoomhz | 28480 | 1854.0071 |
| 032 | 185300232 | $\bigcirc$ |  | TRANSISTOR PNP 81 TO-39 PD=IW FTE200MHZ TRANSIETOR NPN | 28480 28480 | $1853-0232$ $1854-041$ |
| 033 | 1854-0419 | 7 |  | TRANSIETOR NPN EI TO-39 PDEIW FTEzOOMHZ | 28480 | 1854-0410 |
| 035 036 | 188400073 $1853-0232$ | 0 | 1 |  | 28480 28480 | $\begin{aligned} & 1884-0073 \\ & 1853-0232 \end{aligned}$ |
| 036 0201 | 185300232 185440071 | 9 |  | TRANSISTOR PNP SI TOE39 PDEIN TRANSISTOR NPN SI PDESOOMW FTE200MHZ | 28480 | 185400071 |
| 0202 | 1854-0071 | 7 |  | TRANSIETOR NPN SI PDE300MW FTE200MMZ | 28480 | 1854-0071 |
| 0220 | 185300036 | 2 |  | PRANSISTOR PNP SI PDESIIOMW FTE250MHz | 28480 | 1853.0036 |
| 0221 | 1853-0036 | 2 |  | TRANSISTOR PNP AI PDESIOMm FTE250mmz | 28480 | 1853-0036 |
| $R_{1}$ $R_{2}$ $R_{3}$ | $2100-0558$ 210000058 210003253 | 9 | 4 |  | 28480 28480 28480 | $\begin{aligned} & 2100=0558 \\ & 2100=0550 \\ & 2100=3253 \end{aligned}$ |
| Ru | 0683-5135 | 0 | 1 |  | 04121 | CBE115 |
| RS | 0683-2225 | 3 | $\begin{aligned} & \text { See } \\ & \text { *Ind } \end{aligned}$ | RESISJOR 2.2K.5x. 15W PC TCEa400/4700 oduction to this section for ordering inform tes factory selected value | $\mathrm{n}^{01121}$ | C82225 |

8-6-12

Table 8-6-1. Replaceable Parts (Cont'd).

| Reference Designation | HP Part Number | c | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| R ${ }_{\text {R }}^{\text {R }}$ | ${ }^{29190-3283} 0$ | 7 |  |  | 28080 24546 |  |
| ${ }_{\substack{\text { R8 } \\ R 8}}$ |  |  |  |  | 24546 24546 2454 |  |
| ${ }_{\text {R }}^{\text {R9\% }}$ | -0757-0453 | $\stackrel{\square}{0}$ | 1 |  | 2454 <br> 24546 <br> 246 |  |
| 811 | O757-0426 | - | 2 |  | 24546 24546 |  |
|  |  | 3 | ${ }^{6}$ |  | 24546 <br> 24546 |  |
|  |  | ${ }_{2}^{2}$ | 3 |  | ald 0 0 0 121 |  |
| R16 | -0757-0426 | ${ }^{2}$ |  |  | 24546 | C4-1/8-70-1301-F |
|  | - 060301155 | ${ }_{2}^{2}$ |  |  | 21121 24546 |  |
| Rel | - 07577.04897 | : | 4 |  | 24454 24546 |  |
| R21 | -0688-0470 | 3 | ${ }_{2}^{3}$ |  | 24546 24546 |  |
|  | - | 1 | 3 |  | 24546 <br>  <br> 20454 |  |
|  |  | : |  |  | 24546 24546 |  |
| R2\% | 069832319 $0757-043$ | $\bigcirc$ | - |  | 24446 |  |
| R28 R28 R29 |  |  | - |  | 218121 01218 24546 |  |
|  | - | 2 | 11 |  | 放245466 |  |
| R831 | $0757-0190$ 068604315 | 4 | 5 |  | 28480 | ${ }^{0} \mathbf{0} 587870100$ |
| Re32 | - 06868.4335 | 4 | 5 | Resisior |  |  |
|  | -09884471 | ¢ | 1 |  |  |  |
| R36 | -0757-0273 | 4 |  |  | 24546 |  |
| ${ }^{\text {a }}$ A8 | 20607353 | ${ }_{4}$ | 1 |  | ${ }^{26450}$ | 21000558 |
|  | - $\begin{aligned} & 0698.5459 \\ & 0888.3097\end{aligned}$ | 4 |  |  | 294546 |  |
| Rel | - $\begin{aligned} & \text { 0886-3005 } \\ & 0757 \text {-0273 }\end{aligned}$ | 5 | 1 |  | 01121 24546 | E83005 |
|  | - | 3 |  |  | 21124 01121 0 | cious |
|  | 0757.0436 075700465 |  | $\frac{1}{3}$ |  | 24546 24546 |  |
| Rab | 2100-3214 | : | 1 |  | 28480 |  |
| R48 | 0757-0465 | \% |  | ${ }_{\text {Regrisior io }}$ | 220546 | C4-1/8-70-1003 ${ }^{\text {a }}$ |
| ¢ |  | ! | 1 |  | 0121 01121 01121 |  |
| R51 R52 | O757-0499 | $\stackrel{2}{2}$ | 1 |  | 109701 | Mf4c1/8-70-3023-F |
|  | - 0873 | - |  |  | 20121 | cole |
| ¢55 |  | \% | $\stackrel{2}{1}$ |  |  |  |
| R256 | 0757.0280 $0757-0280$ | 3 |  | Resisior lik | 24546 24546 |  |
| ${ }_{\substack{\text { Ress } \\ \text { R59 }}}$ | -0,08831136 | $\stackrel{8}{5}$ |  |  |  |  |
| R890 |  | $\stackrel{5}{4}$ | $\stackrel{2}{2}$ |  | 288480 |  |
| Rot | - 7577.04288 | 1 |  |  | 248546 |  |
|  |  | ! |  |  |  |  |
| Res | O6983329 0 0 0 | $\stackrel{1}{2}$ |  |  | 244896 24560 |  |
| ${ }_{\text {Re7 }}^{\text {R }}$ R66 |  | 2 |  |  | 01121 24546 | C81525 |
| ${ }_{\substack{\text { Reb } \\ \text { Rog }}}$ | - 0868043355 | ¢ |  |  | 01121 24546 |  |
| R870 | -157-0, | $\stackrel{4}{4}$ |  |  | ${ }_{2}^{244480}$ |  |
| Rr11 |  | O |  |  | 24546 | C80118-70-4991-F |
|  |  | $\stackrel{1}{2}$ |  |  | 204546 <br> 24546 |  |
|  |  | $\stackrel{4}{4}$ |  |  | 20122 | C81525 |
|  |  |  |  |  |  |  |
|  |  | 2 |  |  | ${ }_{2}^{245446}$ |  |
| (880 | $\begin{array}{r} 2100-3212 \\ 0698-4123 \end{array}$ | \% |  |  | $\begin{aligned} & 2828400 \\ & \begin{array}{l} 28400 \\ 24546 \end{array} \end{aligned}$ | $0757=0190$ $2100-3212$ <br> $2100-3212$ $E 4=1 / 8-70-499 R-F$ |

Tahle 8-6-1. Replaceable Parts (Cont'd).


Table 8-6-1. Replaceable Parts (Cont'd).


## SERVICE GROUP 7

FRONT PANEL SERVICE GROUP

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# FRONT PANEL SERVICE GROUP SERVICE GROUP 7 

## 8-7.1. INTRODUCTION.

8-7-2. The Front Panel electronics consist primarily of digital switches in push button or rotary form, latches, and buffers. The signals derived from the different switch positions are latched into buffers and interrogated by the Processor F(A7) over the I/O Bus approximately ten times a second. Analog signals are cabled from each front panel control to its respective board. Some of the analog signals pass through the mother board via a front mounted connector.

## 8-7.3. GENERAL INFORMATION.

8-7-4. Suspected Front Panel problems should be verified using the Internal Self Tests (Front Panel Test). These tests will check out the digital circuits and the Rotary Pulse Generator (RPG) which is connected to the N(A12) board. Analog controls may be troubleshot from the board end of the cables connected to the controls. Analog control cables connected to the Display High Voltage section (schematics L and M) may be carrying dangerous voltages capable of causing personal injury.

### 8.7.5. TROUBLESHOOTING THE FRONT PANEL.

### 8.7.6. Removing The Front Panel For Service.

8-7-7. The Front Panel switch electrical pins are accessible when the Front Panel is folded forward and down. Use the following procedure for removing the Front Panel.
a. Disconnect the power and place the instrument on one side.
b. Remove the four plastic feet and the instruction card holder.
c. Remove the plastic strips on the top and bottom of the front panel casting using a small flat bladed screwdriver (inserted into the slots at the rear of each strip) to pry them out. This will reveal the front panel securing screws.
d. Remove eight screws from the top and three screws from the bottom.
e. Place the instrument in the normal position with a piece of soft material before the Front Panel.
f. Carefully slide the Front Panel forward while swinging it down taking care that connecting cabies do not bind (slide the main digital ribbon cable from beneath the plastic guard).
g. With the Front Panel folded down, remove four screws from the A12 board and carefully fold it forward (away from the instrument).
h. The instrument may now be reconnected to a power source and turned on for board level troubelshooting.


Figure 8-7-1. Detaching The Front Panel.

## 8-7.8. Troubleshooting The RPG (Rotary Pulse Generator).

8-7-9. The most typical failure mode of the RPG results in an inability to adjust the start or center frequency in the set start or set center modes. To check the entire A12 assembly and RPG, go through front panel self-test zero, described in Paragraph 8-7-10. If this test fails, remove the front panel and turn the instrument on. As the RPG is turned, pulses should appear at pins 1 and 3 (pins 1 and 3 should be complimentary signals). If no pulses appear, check for +5 on pin 4 and gnd on pin 5. If these are OK, the RPG is most likely at fault.

8-7-10. RPG Front Panel Self-Test. Initiate front panel self-test zero by pressing RESET while holding in average RESTART.

8-7-11. Condition codes 6 and 7 show the current RPG count and the most recent RPG increment, respectively. With the FREQUENCY MODE switch in the $0-25 \mathrm{kHz}$ SPAN or 0 START positions these numbers should remain unchanged when the FREQUENCY ADJUST knob is turned. When the FREQUENCY MODE switch is in the SET START or SET CENTER positions, however, condition codes 6 and 7 should respond to the FREQUENCY ADJUST knob.

8-7-12. Condition code 6 RPG count, should count up or down as the FREQUENCY ADJUST knob is turned right or left, with limits on the RPG count of 000000 thru 061777 (octal).

8-7-13. Condition code 7, RPG increment, shows the most recent change in the RPG count, and it should be possible to see the values 000001,000005 , and 000036 while turning the FREQUENCY ADJUST knob right at low, medium, and high velocity, respectively.

Similarly, turning the FREQUENCY ADJUST knob left at low, medium, and high velocities should give RPG increments of 177777, 177773, and 177742, respectively. When the RPG count arrives at either of its limits, the RPG increment may be left with a value different from those listed above; but, otherwise, errors in the RPG increment indicate front panel malfunctions. In particular, negative increments while adjusting right, or positive increments while adjusting down indicate errors.


Figure 8-7-2. Controls and Connectors.




Table 8-7-1. Replaceable Parts.

| Reference Designation | HP Part Number | $\begin{aligned} & c \\ & D \end{aligned}$ | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\because \times 11$ | 03582-60551 | 9 | 1 | pe assembly, front panel | 28480 | 03582-66551 |
| $c_{1}$ $c_{2}$ | $0160-3622$ 018000210 | 8 |  |  | 28480 56289 | $0160-3622$ $1500335 \times 0015 a z$ |
| ${ }^{6}$ | 018000210 | - |  | CAPACITOR-FXD 3, 3UP +-20x isvoc ta | 56289 | $1500335 \times 001542$ |
| 091 082 085 | 199000487 199000487 | , | 6 |  | 26480 28480 | 500204584 508204584 |
| 092 083 | 19900489 199000489 | ? |  | LED-VISI日LE LUMM INT:MCD IFramamax | 28480 28480 2680 | 5082.4584 50820.4584 |
| Os 085 085 | 199000489 $1900=0487$ | 7 |  |  | 28480 28480 | 5082.4584 508204584 |
| 0s6 | 1990-0487 | , |  | LED-VISIaLE LUM-INTIMCD IF-20ma max | 28480 | 5082-4584 |
| 0s7 | 1990-0487 | , |  | LEDOVISIBLE LUMANTIMCD IFE2OMAMAX | 28480 <br> 28480 | 508200584 |
| 0s8 | 199000487 | , |  | LED-VISIBLE LUM-INTAMCD IF-roma Max | 28480 <br> 28480 <br> 1800 | 5082.4584 5082.4684 |
| ps9 | 199000486 190000486 | $\bigcirc$ |  |  | 28488 28480 | 508204684 |
| J1 J 2 | A120-2622 125125030 125050 | : | 1 | CABLE-SHLD ${ }^{18 A W G} 5$ S-CNOCY JGK-JKT | 28480 22526 28480 | $8120-2022$ 65500118 12510.419 |
| ${ }_{3}$ | 125104170 | , | 1 | CONNECTOR 7 -PIN M POST TYPE | 28480 | $1251-4170$ |
| R1 <br> $R_{2}$ | 0098.4415 0698.4415 | 8 | 11 | RESISTOR 165 1\% , 125W F TC=0.0. 100 RESISTOR 165 1\%. 125W F TC=04-100 | 24596 24540 28480 | C4-1/8-70-16SR-F $C 4.1 / 8=10-165 R-F$ |
| ${ }^{2}$ | 0698.4415 | 8 |  | RESISTOR 165 ix , 125M F TC=0+-100 | 24546 | Ca-1/8-70-16SR-P |
| R R ${ }_{\text {R }}$ | O698-4415 0698.4415 | 8 |  |  | 24546 24546 |  |
| R ${ }_{6}$ | 0698-4415 | 8 |  | RESISTOR 16518.125 F F TC-00+100 | 24546 | C4-1/8-10-165RoF |
| R 1 | 0698-4415 | 8 |  |  | 24546 | $C^{4}=1 / 80-70-165 R-F$ |
| R88 | 069884415 $0698-4415$ | 8 |  |  | 24546 24546 |  |
| $\mathrm{R}_{10}$ | 0698-4415 | 8 |  | RESISTOR 165 ix. 125 FW F $\mathrm{C}=0+-100$ | 24546 | C4-1/8-70-165R-F |
| $\mathrm{R}_{11} \mathrm{R}_{1}$ | 0698.4415 | 8 |  |  | 24546 28400 | C4-1/8-70-165R-F |
| R12 |  | 9 |  |  | 28480 28480 | $\begin{aligned} & 0698-322 \\ & 0698=3228 \end{aligned}$ |
| R14 8.15 | - 07570433 | 8 | 2 |  | 24546 26400 | CC4-1/1-70-70-3321-F |
| $\mathrm{R}^{15}$ | 2100-3685 | 9 | 2 | RESIStor-var m/Sm 5k 10x LiN spoteno | 26480 | 2100-3685 |
| R16 R 17 | $\begin{aligned} & 2100=3685 \\ & 2100=3737 \end{aligned}$ | $\stackrel{9}{2}$ | 1 | RESISTOR-VAR W/SW 5K 10X LIN SPST-NO resistor-variable w/Sw 5 K OHM; +-108 | 28480 28480 | $2100-3685$ $2100-3731$ |
| RP1 | 1810-0049 | ? |  | NETWORK-RES 12-PIN-SIP 15 -PIN-SPCG | 28480 | 181000049 |
| RPD R ${ }^{3}$ | 181000049 181000049 | ? |  | NETWORK-REE | 28480 28480 | 18100049 181000049 |
| ${ }^{3} 1$ |  | 1 | 12 | OWITCHOPB SPDT MOM 2254115 SAC | 28480 |  |
| ${ }^{3}$ | 3101.2272 | 1 |  | Smitchapa spot mom . 25 ilisvac | 28480 | 310102272 |
| ${ }^{33}$ | 3101-2272 | 1 |  | SWITCH-日B spot mom $2525115 V A C$ | 28480 | $3101-2272$ |
| S5 | - $3101-2272$ | $\stackrel{1}{9}$ | 1 | SWITCHPB SPOT MOM, ${ }^{\text {S }}$ | 28480 28480 | 310102272 $3101-2189$ |
| 36 | 3101-2292 | $\frac{1}{2}$ |  | SWITCH-PB SPDP MOM 25 A / 115 SVAC | 28480 | 3101.2272 |
| 88 8 | $3101-2124$ | 2 | 16 |  | 28480 28480 | - 31010102124 |
| 38 | 310102272 310102124 310253 | $\frac{1}{2}$ |  |  | 28480 28480 | 310102272 310102124 310 |
| 310 | 3100-3433 | 6 | 1 | SWITCHORTRY SPatess , 562-DIA IDX=ANGE30 | 28480 | $3100 \cdot 3433$ |
| ${ }^{311}$ | 3101-2124 | 2 |  | SWITCH-PP DPDY ALTNG 250 25a 115 SVAC | 28080 <br> 28480 | $3101-2124$ 310102124 310020 |
| 312 313 | 310102124 $3101-2124$ 312012 | 2 2 2 |  |  | 28480 28480 | 310102124 310102124 310124 |
| ${ }_{314}$ | 3101-2275 | 4 | 1 |  | 28480 | 3101-2275 |
| 315 | 310102124 | 2 |  | SWITCH-PB DPDI ALTNG .25a 115 VAC | 28480 | 3101 -2124 |
| 316 317 | 3101-2124 | 2 |  | SWITCHOPB DPOY ALTNG 25 25A :15VAC | 28480 28480 | 310102124 310102124 310 |
| 317 318 | 310102124 3101.2272 3 | $\stackrel{2}{1}$ |  | SWITCHOPB DPOT ALTMG 25 25A 115VAC | 28480 28480 | 3101012124 $3101-2272$ |
| ${ }_{319}$ | $3101-2272$ | 1 |  | Smitchope spot mom isa 115 SVA | 28480 | 3101.2272 |
| 320 | 3101-2128 | 2 |  | SwITCHEPB DPDT ALTNG .25a lisvac | 28480 | 310102124 |
| 821 822 822 | $3101-2274$ 310102273 3102029 | 3 | $\frac{1}{2}$ |  | 28480 28480 | 310102274 310102273 |
| ${ }_{3} 82$ | 3101-2272 | 1 |  | SWITCHOPG BPDT MDM, 254115 VAC | 28480 | 310102272 |
| 324 | 3101-2273 | 2 |  | SWITCHepe 4 -STATION 15 MM C-C SPACING | 28480 28480 | 310102273 31012124 |
| 325 | 3101-2120 | 2 |  | SWITCHOPS DPDT ALTNG . 254115 VAC | 28480 | 3101-2124 |
| S26 327 | 310102124 | 2 |  | SWITCHoPA OPDT ALTNG 254115 VAC | 28480 28480 | 310102124 310102124 3 |
| 327 <br> 328 <br> 28 | 310102124 310102272 31012 | 2 |  |  | 28480 | 310102129 3101022 31021 |
| 329 | ${ }^{3101-2124}$ | 2 |  | SWITCH-PB OPDT ALTNG .25A 115 VALC | 28480 28480 | 310102124 310102124 |
| 330 | 3101-2124 | 2 |  | SWITCHEPB DPDT ALTNG .25a lisvac | 28480 | $3101-2124$ |
| 331 332 331 | 310102272 <br> $3101-2124$ <br> 101 | 1 2 2 |  |  | 28480 26480 |  |
| S33 | 3101-2124 | $\stackrel{2}{2}$ |  | ${ }^{\text {SWITCHOPB }}$ DPDT ALTNG. 25 L 115VAC | 28880 | 3101-2124 |
| S34 s35 | 31012272 $3100-3437$ | ${ }_{0}^{1}$ | 1 |  | 26480 26480 28480 | $3101-2272$ $\mathbf{3 1 0 0 0 3 4 7}$ |
|  |  |  |  | :\%ON instruments prefixed 1747A - remove NOISE LEVEL POT 2100-2588 FOR REV A. |  |  |

Tahle 8-7.1. Replaceable Parts (Cont'd).


Table 8-7-1. Replaceable Parts (Cont'd).


Table 8-7-1. Replaceable Parts (Cont'd).


Table 8-7-1. Replaceable Parts (Cont'd).


Table 8-7.1. Replaceable Parts (Cont'd).


SERVICE GROUP 8 HP-IB

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## HP-IB <br> SERVICE GROUP 8

## 8.8-1. INTRODUCTION.

8-8-2. The HP-IB board provides an isolated link between the Processor and the HP-IB connector. Bus protocol is handled by a nanoprocessor which also sequences the operation of devices and circuits on the board through the data/instruction bus, device select, and direct control outputs. The HP-IB board communicates with the Processor using an interrupt scheme. The Processor F(A7) controls the HP-IB board by entering commands through the command register.

## 8-8-3. GENERAL INFORMATION.

8-8-4. The HP-IB board is the only board which may be removed from the instrument allowing full manual control to continue. Thus, if processor problems are suspected, try removing the HP-IB board from the instrument. This will help to eliminate I/O Bus problems where one or more lines may be held low, possibly resulting in an inability to enter a Front Panel Self-Test. Operation of the board is dependent on a clock signal from the Timing board C(A3). The HP-IB board has its own internal self-test loops in addition to Signature Analysis (SA).

## 8-8-5. TROUBLESHOOTING THE HP-IB BOARD.

## 8-8-6. Installation of HP.IB Board.

a. Install the board and check the following:

1. +12 V at $\mathrm{XA} 2 \mathrm{~A}(18)$
2. -18 V at $\mathrm{XA} 2 \mathrm{~B}(18)$
3. +5 V at $\mathrm{XA} 2 \mathrm{~A}(17)$
4. 4 MHz clock at $\mathrm{XA} 2 \mathrm{~B}(\mathrm{~N})$
b. Adjust $\mathrm{V}_{\mathrm{BG}}$ at TP3 with the pot to the voltage marked on $\mathrm{U} 16( \pm .2 \mathrm{~V})$.

## 8-8-7. Troubleshooting Procedures.

8-8-8. The first thing to do if there are problems associated with remote operation is to run the Blinking Light Test. If the A2 board passes this test, the board is OK and the problem is probably with the processor. Check that the FLG and STS lines to the processor aren't being held low and use the front panel I/O bus test to check the bus lines from the processor (details are given on the last page of this section).

8-8-9. If the board fails the Blinking Light Test, go to SA Test 1. This test runs through the test program until an error is detected and then branches to the end. This is in order to retain a signature characteristic of the error. If it passes this test, check the LED. If it fails, go to Test 2. This is the same as Test 1 except that it doesn't branch to the end on an error, allow-
ing SA troubleshooting. There are SA flow charts following this test that follow data flows. If the board fails the initial check of Test 2, the test program is wrong and the following tests check out the processor and instruction ROM.

## NOTE

For each test, the board is preset by momentarily shorting TP1 to ground. If you get a wrong signature, preset the board again and recheck.

## NOTE

Be sure NO HP-IB cable is connected to the rear panel.

## 8-8-10. Blinking Light Test.

a. Set the HP-IB address to 1018 . ( 1000001 )
b. Preset the board by momentarily shorting TP1 to ground.
c. A blinking light indicates the board is OK. If the light doesn't blink, go to SA Test 1.

Table 8-8-1. SA Test 1 Dverall Test With Program Branching.


Preset board by momentarily shorting TP1 to ground and disconnect the HP-IB cable.
Check the SA signature at +5 V . Should be 9C81. A correct signature at this point indicates the test ROM is generating the right test program which should make the light blink. If it is not blinking, check the LED itself. If the SA signature checks bad, check J 1 (4) and $\mathrm{J} 1(5)$. If the lines are static go to SA Test \#3 otherwise go to the SA Test 1 Trouble Table and attempt to localize the trouble. Then continue with SA Test 2 to pinpoint the trouble.

## SA Test 1 Trouble Tabla

Coda Possible Trouble

9515 U16(37) signal.
5159 U16(37) signal.
159A U16(32) signal.
59A4 U16(32) signal.
6929 U16(33) signal.
$29 F 3$ U16(36), U16(35), U16(31) signals.
70FC U16(36) shorted to ground.
$32 \mathrm{HF} \quad \mathrm{U} 16(35)$ shorted to ground.
29F3 U16(31) shorted to ground.
70HA U16(36), U16(35), U16(31) signals.
3696 U16(36), U16(35), U16(31) signals.
ASC1 U9(6), U1(8), U1(3), to Data Bus or Device Select to U24(13), U3(1).
H6PC Received wrong data thru Bus; Data Latch U5, U6.
6PCP Received wrong data thru Bus Control Latch U23, U8, U9, U38, U39, U21, U22, U26, U27.
PCP5 Received wrong data thru BPC - Data Latch U30.
UP64 Error in EOI line.
593A Error in ATN line.
4PC7 Error in REN line.
H5H8 Same as H6PC; U35.
5H82 Same as PCP5; U30.
OAU9 Error in REMOTE line; not necessarily in "REN".
U9H5 Same as 6PCP.
C45H Error in IMD not floating bus lines.
66PO Same as H6PC.
PFHF No ATN interrupt.

Table 8-8-2. SA Test 2 General SA Test
(Same as Test 1 without branching)

| Address switch $=104_{8}$ |  |  |
| :---: | :---: | :---: |
|  | Clock | J1(3) |
| SA Test Jack J1 | Start | J1 (4) |
|  | Stop | J 1 (5) |

Preset board by momentarily shorting TP1 to ground.
Check the SA signatures at +5 V and at $\mathrm{U} 16(1)$. These should be UHC8 and FUU5 respectively.

If either signature checks bad, a wrong test program is being generated. Continue with SA Test 3 in this case.

If both signatures check OK, pinpoint the trouble by using the SA signatures given as follows:

| Flow Chart 1: |  | Bus Buffers $\longrightarrow$ Isolation |  |  |  | Circuits $\longrightarrow$ Processor |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | (Test Jack J1) |  |  |  |  |  |  |  |
| U36(14) | Cu99 | U36(13) | Cu99 | U35(2) | 4221 | U35(3) | 187A | U16(1) | FUU5 |
| 10 | 9592 | 11 | 9592 | 5 | 682A | 4 | 810A | 2 | 5A86 |
| 6 | P3U9 | 5 | P3U9 | 6 | 1 P 41 | 7 | 14 HH | 3 | $33 \mathrm{P6}$ |
| 2 | 65AO | 3 | 65AO | 9 | 9819 | 8 | P3C1 | 4 | $1 \mathrm{U6H}$ |
| U37(14) | A5F7 | U37(13) | A5F7 | 12 | 5870 | 13 | UU63 | 5 | 4HU6 |
| 10 | P850 | 11 | P850 | 15 | 15P8 | 14 | POU1 | 6 | F615 |
| 6 | OU57 | 5 | OU57 | 16 | U2PU | 17 | 6HP4 | 7 | 4470 |
| 2 | 372 H | $\longrightarrow 3$ | 372 H | $\rightarrow 19$ | FAC5 | 18 | A4PC | 8 | 0000 |
| U38(14) | FFO6 | U38(13) | FFO6 | U21(3) | 1 A00 | $\rightarrow$ U27(7) | 980F- | $\rightarrow 9$ | 4FU4 |
| 10 | 0369 | 11 | 3UUH | 6 | F377 | 9 | 7UUC | 26 | AC6A |
| 6 | HU6C | 5 | P3UU | 11 | CUP2 | 11 | F7UU | 31 | 980F |
| 2 | 2694 | 3 | 1 A00 | 14 | C306 | U28(10) | 7UPO | 32 | 7UPO |
| U39(14) | F377 | U39(13) | F377 | U27(1) | FF06 | U21(4) | UU63 | 33 | UHC8 |
| 10 | CUP2 | 11 | CUP2 | 14 | 3UUH | 5 | POU1 | 34 | UHC8 |
| 6 | C306 | 5 | C306 | 13 | P3UU | 12 | 187A | 35 | F7UU |
| 2 | UHC8 | 3 | UHC8 | 2 | 1 A00 | 13 | 6HP4 | 36 | 7UUC |
| U40(15) | 3F94 | U40(13) 14 | F377 |  |  |  |  | 37 | 38 CU |

Table 8-8-2. SA Test 2 General SA Test (Cont'd).

| Flow Chart 2: | $1 / 0$ Bus |  | - I/O Buffers <br> (Test Jack J1) |  | - Processor |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |
|  | U32(3) | UHUC | U32(2) | 0884 | U3313) | 187A |
|  | 5 | 799C | 4 | AOAA | 4 | 810A |
|  | 7 | C771 | 6 | 7905 | 7 | 14 HH |
|  | 9 | 458 C | 8 | 6060 | 8 | P3C1 |
|  | 17 | A192 | 18 | 61 UF | 18 | UU63 |
|  | 15 | 424H | 16 | 57 A 1 | 17 | POU1 |
|  | 13 | $8 \mathrm{CO6}$ | 14 | FCCH | 14 | 6HP4 |
|  | 11 | U8HA | 12 | C113 | 13 | A4PC |

Flow Chart 3:
Device Select
(Test Jack J1)

| U4(15) | P6A8 |  | U4(1) | H47U |
| :---: | :---: | :---: | ---: | ---: |
| 14 | $44 A F$ |  | 2 | $1 C 5 H$ |
| 13 | $7 C 13$ |  | 3 | $C C 95$ |
| 12 | $9 U 3 A$ |  | 4 | $8 A H U$ |
| 11 | H519 |  | 5 | 0000 |
| 10 | $9.1 U 8$ |  | U16(16) | 7039 |
| U23(12) | $7 F 68$ | U23(3.5) | $14 F P$ |  |
| 9 | POC5 | 10,14 | 6165 |  |
| 7 | $3 H 61$ |  |  |  |
| 4 | $H 417$ |  |  |  |

Flow Chart 4: Incomming Buffer and Isolation Circuits

$$
\text { Address switch }=104_{8}
$$

This test writes out through U35 and back through the buffers and isolation circuits, allowing SA testing.

| CIk: | U16(16) |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Start: | U16(9) | $\Gamma$ |  |  |  |
| Stop: | U16(9) |  |  |  |  |
| Preset Board |  | +5 Signature 3395 |  |  |  |
| U5(2) | H966 | U36(15) | H966 | U25(10) | PAU3 |
| 3 | F8FU | 9 | 8PFC | 8 | CH5P |
| 5 | 8PFC | 7 | 043P | 6 | 37AC |
| 6 | 919A | 1 | C560 | 4 | $86 \mathrm{U5}$ |
|  |  | U37(15) | 434C |  |  |
| 11 | 043P |  |  | U26(10) | 70HP |
| 10 | 4823 | 9 | 3H8P | 8 | OP1C |
|  |  | 7 | 3256 |  |  |
| 14 | C560 |  |  | 6 | 01F3 |
|  |  | 1 | 3349 |  |  |
| 13 | 3395 | U38(7) | F8FU | 4 | 003F |
| U6(2) | 434C | 9 | 919A | U27111) | F8FF |
| 3 | 97H6 | 15 | 4823 | 9 | 9199 |
| 5 | $3 \mathrm{H8P}$ | 1 | P910 | 7 | 4823 |
|  |  | U39(15) | 97H6 |  |  |
| 6 | 99FH |  |  | 5 | P913 |
|  | 3256 | 9 | 733P | U28(10) | 0003 |
|  |  | 7 | 980P |  |  |
| 10 | 980P |  |  |  |  |
|  |  | 1 | 3395 |  |  |
| 14 | 33A9 |  |  |  |  |
| 13 | P910 |  |  |  |  |

Table 8-8-3. SA Test 3.

## Remove U34

Verify that $\mathrm{U} 16(29)$ is high; a low level at this pin means that the nanoprocessor is constantly being interrupted due to a DC level problem. Check the interrupt circuitry to determine what holds U16(29) low.

Check for a clock signal at J2(4); the absence of a signal indicates a nanoprocessor problem.


Check for following signatures:

| U16 pin | 1 | C21A | U16 pins 17,26,28,30,33,38 all zero |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| pin | 2 | HA07 |  |  |  |
| pin | 3 | HOAA | U16 pins 12-40 except above all ones (7A70) |  |  |
| pin | 4 | P030 |  |  |  |
| pin | 5 | 4442 |  |  |  |
| pin | 6 | 4U2A |  |  |  |
| pin | 7 | 0772 | U15 pin | 9 | COC8 |
| pin | 8 | 9635 | pin | 10 | 3UP7 |
| pin | 9 | 1734 | pin | 11 | 9507 |
| pin | 10 | 8P54 | pin | 13 | CC96 |
| pin | 11 | 0000 | pin | 14 | 24HC |
| $+5 \mathrm{~V}$ |  | 7 7 70 | pin | 15 | 5H44 |
|  |  |  | pin | 16 | 429F |
|  |  |  | pin | 17 | 6PUA |

Change addess to 000 . (0000000)
Check for following signatures:

| U15 pin | 9 | UAU6 | If any of the signatures are bad, the |
| ---: | ---: | ---: | :--- |
| pin | 10 | HOPU | problem is either the ROM or the nano- |
| pin | 11 | U255 | processor. |
| pin | 13 | $4 A F 2$ |  |
| pin | 14 | UAU7 | If all signatures are OK, continue with |
| pin | 15 | 7412 | SA Test 4. |
| pin | 16 | PUPP |  |
| pin | 17 | U6A5 | Insert U34 |

Table 8-8-4. SA Test 4.


Check for the following correct signatures:

| + 5 V-----------------UP73 |  |  |
| ---: | ---: | ---: |
|  |  |  |
| U16 pin | 1 | $55 H 2$ |
| pin | 2 | $334 H$ |
| pin | 3 | OU16 |
| pin | 4 | OOUP |
| pin | 5 | 0 |
| pin | 6 | UP73 |
| pin | 7 | UP73 |
| pin | 8 | 0 |
| pin | 9 | UP73 |

SA Test Jack J1

| U16 pin | 10 | UP73 |
| ---: | ---: | ---: |
| pin | 11 | 0 |
| pin | 18 | UP73 |
| pin | 19 | UP73 |
| pin | 20 | UP73 |
| pin | 21 | UP73 |
| pin | 22 | UP73 |
| pin | 23 | UP73 |
| pin | 24 | UP73 |
| pin | 25 | UP73 |
| pin | 34 | UP70 |

Clock J1(3) ک
Start J1(4) -
Stop J1(5) L
Preset board
Check for the following correct signatures:

| U16 pin | 29 | P545 |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| U4 pin | 1 | 3 H 3 C | U4 | pin | 9 | U1P7 |
| pin | 2 | 5077 |  | pin | 10 | C7FF |
| pin | 3 | F203 |  | pin | 11 | AU61 |
| pin | 4 | FC24 |  | pin | 12 | FHH7 |
| pin | 5 | 0 |  | pin | 13 | 470 P |
| pin | 6 | P545 |  | pin | 14 | 6F69 |
| pin | 7 | PO6H |  | pin | 15 | F1U6 |
| pin | 8 | 0 |  | pin | 16 | P545 |
| U23 pin | 1 | 4PP7 | U23 | pin | 9 | U1PU |
| pin | 2 | P545 |  | pin | 10 | U1P7 |
| pin | 3 | P06H |  | pin | 11 | P545 |
| pin | 4 | P06U |  | pin | 12 | P54H |
| pin | 5 | PO6H |  | pin | 13 | P545 |
| pin | 6 | P545 |  | pin | 14 | U1P7 |
| pin | 7 | P547 |  | pin | 15 | 0 |
| pin | 8 | 0 |  | pin | 16 | P545 |

If all signatures checked OK, continue with DSA Test 5 .

Table 8-8-5. SA Test 5. Read Switch Test


Table 8-8-6. SA Test 6 Interrupt Test.


Table 8-8-7. Front Panel I/O Bus Test.
This test checks the I/O bus lines from the processor. Do this test only if the board passes the Blinking Light Test and you are having bus problems that aren't external.

Put HP-IB address to $013_{8}$
Select I/O Bus Test \#6
(Front panel self-test, Ave \#256, then short A7 J4 and push RESTART).

| Clk: | $036[\mathrm{U}(13)]$ |  |
| :--- | :--- | :--- |
| Start/Stop: | I/O \#7 [U32(11)] |  |
| +5 Signature: | UFP6 | 0000 |
|  |  |  |


| I/O 7 | U3O(13) | O1UF | U3O(12) | 026 C |
| ---: | ---: | ---: | ---: | ---: |
| 6 | 14 | $03 U 9$ | 15 | 0369 |
| 5 | 17 | $07 U 3$ | 16 | $016 F$ |
| 4 | 18 | OUP7 | 19 | 0566 |
| 3 | 8 | 1 UFP | 9 | OH72 |
| 2 | 7 | $3 U 9 F$ | 6 | $1 H 5 C$ |
| 1 | 4 | $7 U 39$ | 5 | $3 H O 9$ |
| 0 | 3 | UP73 | 2 | $7 H A F$ |

Table 8-8-8. HP-IB Interconnections.


Table 8-8-9. Mnemonic Dictionary.

| Code | Definition |
| :---: | :---: |
| ATN | Attention |
| DAV | Data Valid |
| D6-D7 | Data I/O |
| DC0-DC6 | Direct Control |
| DS0-DS3 | Device Select |
| ENA | Interrupt Enable |
| EOI | End or Identify |
| IFC | Interface Clear |
| IMD | Interface Multiplex Data |
| INT ACK | Interrupt Acknowledge |
| PG | Program Gate |
| PAO-PA10 | Program Rom Address |
| PDAC | Peripheral Data Accepted |
| PDAV | Peripheral Data Valid |
| PFLG | Peripheral Flag |
| PREN | Peripheral Remote Enable |
| PRFD | Peripheral Ready For Data |
| PSTS | Peripheral Status |
| PWRCL | Power Up Clear |
| PWRINT | Power Up Interrupt |
| R/W | Read/Write Select |
| REN | Remote Enable |
| REQ | Interrupt Request |
| RFD | Ready For Data |
| RCCR | Read Computer Command Register |
| RCOD | Read Computer Output Data |
| RIBA | Read Interface Binary Address |
| RIBC | Read Interface Binary Control |
| RIBD | Read Interface Binary Data |
| SCID | Send Computer Interface Data |
| SIBC | Send Interface Binary Control |
| SIBD | Send Interface Binary Data |
| TSTSTB | Tri-state, Tri-state to Buffer |
| Vbg | Back Gate Voltage Bias |
| WCCR | Write Computer Command Register |
| WIRR | Write Interface Remote Register |

Table 8-8-10. Line Functions.

| Line | Definition |
| :--- | :--- |
| STATUS | Tells the computer the peripheral is OK and running. <br> Tells the computer the peripheral is busy processing <br> data or is ready for a data transfer. |
| IOB15 | Tells computer when remote is initiated. <br> Tells computer when the HP-IB board is in place. <br> IOB9 <br> CLEAR <br> sequence. <br> sells the Nanoprocessor that a data transfer is <br> complete <br> Tells Nanoprocessor whether computer is reading or <br> writing. |
| Tells Nanoprocessor the type of Data coming down |  |
| the I/O Bus. |  |

Table 8-8-11. HP.IB Troubleshooting Hints.

1. Always check power supply voltages and back gate bias (Vbg) voltage on nanoprocessor.
a. A misadjusted Vbg can cause:
(1) Failure after warm-up (too high).
(2) Relays on A1 board to clatter and processor to run erratically (too low).
b. An inability to adjust Vbg (usually less than .6 V ) may indicate a bad nanoprocessor.
2. Some resistor packs were installed and soldered into the board and appear to be bent over. These resistor packs may function correctly; however, do not straighten them up as broken traces may result.
3. If the blinking light test passes, but bus problems persist, check inverter U2D.
4. If preliminary DSA tests fail, check HP-IB address switches for continuity when closed. Also check outputs on U22 for low true signal when the gate on pins 1 and 15 is activated.
5. Be sure that the HP-IB cable is disconnected before performing the SA tests.




Table 8-8-12. Replaceable Parts.

\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Reference Designation \& HP Part Number \& C \& Oty \& Description \& Mfr Code \& Mfr Part Number <br>
\hline ${ }_{4}^{4}$ \& 03582-66502 \& 0 \& 1 \& PC Assembly, mpaib interface \& 28480 \& 03582-66502 <br>
\hline ${ }^{C} 1$ \& 0160-3847 \& 9 \& 53 \& CAPACITOROFXO . O1UF \$100-0X SOVOC CER \& 28480 \& <br>
\hline $C 2$
$C 3$ \& $0160-3847$
$0160-3847$ \& 9 \& \& CAPACITOR-FXD OIS
CAPACITOR-FXD
OIU
O \& 28480
28480 \& $0160-3847$
$0160-3847$ <br>
\hline ca \& 0160-3647 \& 9 \& \& CAPACITOR-FXD .01UF +100-0X SOVDC EER \& 28480 \& 0160-3847 <br>
\hline C5 \& 0180-0228 \& 6 \& \& CAPAEITORAFXD 22UF+EIOX 15VDC TA \& 56289 \& 1500226×901582 <br>
\hline ${ }_{6} 6$ \& 0160-3047 \& 9 \& \& CAPACIYOROFXD .01UF \$100-0\% SOVDC CER \& 28480 \& 0160-3847 <br>
\hline ${ }_{\text {c }}{ }^{\text {c }}$ \& 01800011
$0160-3047$ \& 9 \& \& CAPACITOR-FXD 6, BUF + -10x 35VOC TA \& 56289
28480 \& $1500685 \times 903582$
0160.3847 <br>
\hline C8 \& $0160-3047$
$0160-3847$ \& 9 \& \&  \& 28480
28480 \& $0160-3847$
$0160-3847$ <br>
\hline $c_{10}$ \& 0160-3647 \& 9 \& \& CAPACITOR-FXD .01UF $+100=0 \mathrm{X}$ SOVDC CER \& 28480 \& 0160-3847 <br>
\hline ${ }_{6} 11$ \& 0160-3847 \& 9 \& \& CAPACITORAFXD .01UF $+100=0 \times$ SOVDC CER \& 28480 \& 0160-3847 <br>
\hline C12
c13 \& $0160-3847$
$0160-3847$ \& 9 \& \& CAPACITOR-FXD .01UF \$100-0X SOVDC CER
CAPAEITOR-FXD \& 28480
28480 \& $0160-3847$
$0160-3847$ <br>
\hline C13
C14 \& $0160-3847$
$0160-3847$ \& 9 \& \& CAPACITOR-FXD .01UF $+100=0 \mathrm{X}$ SOVDC CER
CAPACITOR-FXD .01UF $\$ 100-0 X$ SOVDC EER \& 28480
28480 \& $0160-3847$
$0160-3847$ <br>
\hline ${ }_{4} 15$ \& 0160-3847 \& 9 \& \& CAPACITOR-FXD .01UF +100 -0X SOVDC CER \& 28480 \& 0160-3847 <br>
\hline ${ }_{1} 16$ \& 016003047 \& 9 \& \& CAPACITOR -FXD
CAPACITOR-FXD
S OUF \& 28480
56289 \& <br>
\hline ${ }_{6} 17$ \& 0180-0229 \& 7 \& 5 \&  \& 56289
56289 \& $1500336 \times 901082$
$1500685 \times 903582$ <br>
\hline C18
C19

189 \& 018000116
018000229 \& 7 \& \&  \& 56289
56289 \& $1500685 \times 903582$
$1500336 \times 901082$ <br>
\hline C20 \& 0160.3847 \& 9 \& \& CAPACITORAFXD .01UF $+100=0 \mathrm{~S}$ SOVDC CER \& 28480 \& $0160-3847$ <br>
\hline C21
C22 \& $0160-3847$
018000229 \& 9 \& \& CAPACITORAFXD OIUF $\$ 100=0 \%$ SOVDC CER CAPACITOR-FXD $33 U F \neq 10 \%$ 10VDC TA \& 28480

56289 \& $$
\begin{aligned}
& 0160-3847 \\
& 1500336 \times 901082
\end{aligned}
$$ <br>

\hline CRI \& 1901-0033 \& , \& \& OIODE-GEN PRP 1 BOV 200MA DO-7 \& 28480 \& 1901-0033 <br>
\hline CR3 \& 1901-0040 \& 1 \& \& DIODE-SWITCHING 30V 50MA 2NS DO-35 \& 28480 \& 1901-0040 <br>
\hline CR4
CR5 \& $1902-3030$
$1902-3054$ \& 7
5 \& 2 \&  \& 28480
28480 \& $1902-3030$
$1902-3054$ <br>
\hline CR6 \& 1901-0040 \& 5 \& 2 \& DIODESSWITCAINS SOV 50 MA 2NS DO.35 \& 28480 \& 1901-0040 <br>
\hline Cr8 \& 1902-3054 \& 5 \& \& DIODE-2NR 3.65V 5x Dow PDE.4N TCE*.055x \& 28480 \& 1902-3054 <br>
\hline DSI \& 1990-0486 \& 6 \& \& LED-VIsible Lumainteimed ifazomasmax \& 28480 \& 5082-4684 <br>
\hline $E_{1}$ \& 1810-0326 \& 3 \& 1 \& NETWORK=RD 10 PIN SIPI 0.1 IN SPAEING \& 28480 \& 1810-0326 <br>
\hline ${ }^{1} 1$ \& 1251-5202 \& - \& \& CONNECTOR S-PIN M POST TYPE \& 28480 \& 1251-5202 <br>
\hline $\mathrm{J}_{3}$ \& $1251-5202$
$1251-5202$ \& 8 \& \& CONNECTOR S-PIN M POST TYPE
CONNECTOR $5-P$ IN M POST TYPE \& 28480
28480 \& $1251-5202$
$1251-5202$ <br>
\hline 41 \& 9100-4031 \& 8 \& 1 \& TRANSFORMER IND: 225 MAY $-10 \%,+50 \%, D C$ \& 28480 \& 910004031 <br>
\hline 01 \& 1854-0071 \& 7 \& \& TRANSISTOR NPN SI PDE300mm FiE200mhz \& 28480 \& 185400071 <br>
\hline $\mathrm{R}_{1}$ \& 0083-1335 \& 4 \& 4 \&  \& 01121 \& CB1335 <br>

\hline | R2 |
| :--- |
| R3 | \& $0683-2715$

$0683-1525$ \& 4 \& 5 \&  \& 01121
01121 \& CB2715
CB1525 <br>
\hline Ra \& 0683-2715 \& 6 \& \& RESISTOR 270 5x. 25W FC TC=000/ 600 \& 01121 \& c82715 <br>
\hline R5 \& 2100-3273 \& 1 \& \& RESISTOR-TRMR 2K 10X C SIDE-ADJ I-TRN \& 28480 \& 210003273 <br>
\hline R6 \& 0083-3625 \& 9 \& 1 \& RESISTOR 3.6K 5x, 25w FC TCE-400/ 700 \& 01121 \& ${ }^{C} 83625$ <br>
\hline R8 \& 0683-5135 \& 0 \& \& RESISTOR S1K 5\% . 25 W FC TCE-400/4800 \& 01121 \& C85135 <br>
\hline R911 \& 0683-1335 \& 0
2
2 \& 2 \&  \& 01121 \& C81335
$C 87505$ <br>
\hline R12 \& 0683-2715 \& 6 \& \& RESISTOR 270 5\%.25W.FC TC $=-400 /+600$ \& 01121 \& CB2715 <br>
\hline R13
R14 \& $0683-3925$

$0603-7505$ \& 2 \& 1 \& RESISTOR 3.9K 5x, 25W FC TC-a400/* 700 RESISTOR 75 5x. 25w FC TC-400/4500 \& \[
$$
\begin{aligned}
& 01121 \\
& 01121
\end{aligned}
$$

\] \& \[

$$
\begin{aligned}
& C 83925 \\
& 687505
\end{aligned}
$$
\] <br>

\hline RP 7 \& 1810.0329 \& 6 \& 4 \& NETWORK-RES 10-PIN-SIP .I-PIN-SPCG \& 91637 \& CSP10E-01-7526 <br>
\hline AP 10 \& 181000329 \& 6 \& \& NETWORK-RES $10-P I N-S I P$ il 10 PIN-SPCG \& 91637 \& CSP10E-01-7326 <br>
\hline AP15 \& 1810-0329 \& 6 \& \& NETWORK-RES $10-P I N=S I P \cdot 1-P I N-S P C G$ \& 91637 \& CSP10E-01-7326 <br>
\hline RP16 \& 1810-0329 \& 6 \& \&  \& 91637 \& CSPIOE-01-7526 <br>
\hline $s_{1}$ \& 3101-2215 \& 2 \& 1 \& SWITCHERKR DIPGRKR-ASSY 7-14.054 3OVDC \& 28480 \& 3101-2215 <br>
\hline $U_{1}$ \& 1820-1198 \& 0 \& 4 \& IC gate itl ls nand quad z-inp \& 01295 \& 8N74L803N <br>
\hline ${ }_{4}$ \& 1820-1201 \& 6 \& 6 \& IC GATE TTL LS AND QUAD 2-INP \& 01295 \& SN7ALSOBN BN74LS173N <br>
\hline 43 \& 1820-1195 \& 7 \& 3 \& IC FFTTTL LS D-TYPE POS-EDEE-TRIG COM \& 01295
01295 \& 8N74L8175N SN74L8138N <br>
\hline 44
45 \& $1820-1216$
1820.1439 \& 3
2 \& 2 \& IC DCDR TTL LS 3-TO-B-LINE 3-INP
IC MUXRIDATA-SEL TTL LS $2-T \mathrm{O}$
IOLINE \& 01295

01295 \& $$
\begin{aligned}
& \text { SN74L8138N } \\
& \text { 8N74LS2S8N }
\end{aligned}
$$ <br>

\hline $U_{6}$ \& 1820-1439 \& 2 \& \& IC MUXR/DATA-EEL TTL LS 2-T0-1-LINE \& 01295 \& SN74L3258N <br>
\hline 47 \& 1820-1144 \& 6 \& \& IC GATE TTL LS NOR QUAD 2-INP \& 01295 \& SN74L802N <br>
\hline U8
40 \& $1820-1199$

$1820-1198$ \& 1 \& \& IC INV TTL L8 MEX 1 -INP \& $$
\begin{aligned}
& 01295 \\
& 01295
\end{aligned}
$$ \& SN74LIOCN

BN74LSOSN <br>
\hline 49
410 \& $1820=1198$
$1820-1112$ \& 0 \& \& IC GATE TTL LS NAND QUAD 2-INP

IC FF TTL LS DOTYPE POS-EDGE-TRIG \& $$
\begin{aligned}
& 01295 \\
& 01295
\end{aligned}
$$ \& \[

$$
\begin{aligned}
& 8 N 74 L 803 \mathrm{~N} \\
& \text { SN74L874N }
\end{aligned}
$$
\] <br>

\hline U11 \& 1820-1112 \& 8 \& \& \& 01295 \& 8N74L874N <br>

\hline $U_{12}$ \& 1820-1425 \& \[
6

\] \& 1 \& IC BCHMITT-TRIS TTL LS NAND QUAD Z-INP \& \[

01295
\] \& SN74L8132N <br>

\hline 413 \& \& ${ }^{6}$ \& \& If GATE TTL LE NOR QUAD 2-INP \& $$
01293
$$ \& BN74L802N <br>

\hline 114

415 \& $$
\begin{aligned}
& 1820=1112 \\
& 1816=1200
\end{aligned}
$$ \& 8 \& 1 \& IC FF TTL LS D-TYPE POS-EDGE-TRIG \& \[

$$
\begin{aligned}
& 01295 \\
& 28480
\end{aligned}
$$

\] \& \[

$$
\begin{aligned}
& \text { SN74LS74N } \\
& 1816-1200
\end{aligned}
$$
\] <br>

\hline
\end{tabular}

Table 8-8-12. Replaceable Parts (Cont'd).

| Reference Designation | HP Part Number | C | Oty | Description | Mfr Code | Mfr P | umber |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 416 | 1820-1691 | 8 | $\frac{1}{5}$ | IC MICPROC MOSSOCKET-IC $40-C O N T$ OIP-8LOR | 28480 28480 |  |  |
| U17 | 1200-0659 | 2 |  |  | 04713 | 1200-0659 <br> MLM339P |  |
| U18 | 182600138 | 8 |  | ic 339 COMPARATOR 14 -DIP-P | 04713 |  |  |
| U19 | 182600138 | 8 |  | IC 330 COMPARATOR 140 DiPap | 04713 | MLM339P |  |
| U20 | 1826-0138 | 8 | 3 | IC 339 COMPARATOR 14 -DIP.P <br> IC FF TTL LS DOTYPE POSOEOGETRIG COM <br> IC EFR TTL LS NONEINV HEX 1-INP <br> IC MUXRTDATAEBEL TFL LA 2-TO-ITLINE GUAD <br> IE INV TTL LS HEX IUINP | $\begin{aligned} & 04713 \\ & 01295 \\ & 01295 \\ & 01295 \\ & 01295 \end{aligned}$ | MLM339P <br> 8N74L8175N <br> 8N74L8367N <br> 8N74L8257N <br> 8N74L8OAN |  |
| U21 | 1820-1195 | 7 |  |  |  |  |  |
| U22 | 1820-1491 | 6 |  |  |  |  |  |
| 423 | 1820-1438 | 1 |  |  |  |  |  |
| 424 | 1820-1199 | 1 |  |  |  |  |  |
| 425 426 | $1826-0138$ 1826.0138 | 8 |  | IE 330 COMPARATOR 14 -DIPop |  | MLH339P MLM3300 |  |
| U26 U27 | 182600138 182600138 | 8 |  |  | 04713 04913 | $\begin{aligned} & \text { MLM339 } \\ & \text { MLM339P } \end{aligned}$ |  |
| U28 | 182600138 | 8 |  | If 339 COMPARATOR 140 DIPAP | 04713 | MLM339PSN74L874N |  |
| U29 | 1820-1:12 | 8 |  | IC PF TTL LS D-TYPE POS-EDGE-TRIG | 01295 | 8N74L874N |  |
| $U_{30}$ | 1820-1730 | 6 |  | IE FF TTL LS D-TYPE POS-EDOE-TRIG COMIC SFR TTL LS INV OCTL $2-I N P$ | 01295 | 8N74L8273N |  |
| 431 | $1820-1873$ | 8 |  |  | 2701427014 | DMA1LEABN <br> OMBLLE9BN |  |
| 432 | 1820-1873 | 8 |  | IC EFR TTL LS INV OCTL $2=I N P$ |  |  |  |
| 433 | 1820-1730 | 6 |  | IC FF TTL 18 D-TYPE POSEEDEETRIG COM NETWORK-ENOCT MODULE DIPI 16 PINS: 0.100 | $\begin{aligned} & 01295 \\ & 28480 \end{aligned}$ | OMEILEAEN |  |
| 434 | $1810-0309$ $1200-0473$ | 0 | 1 |  |  | $\begin{aligned} & 181000307 \\ & 1200=0493 \end{aligned}$ |  |
| 435 436 | $1820-1730$ $1820-1689$ | 4 | 4 | If FF TTL LS D-TYPE POS-EDGE-TRIG COM | $\begin{aligned} & 01295 \\ & 04713 \end{aligned}$ | 8N74L8273N MC3446 |  |
| 437 | 1820-1689 | 4 | 4 | IC Mise OUAD ie mise ouad | $\begin{aligned} & 04713 \\ & 04713 \end{aligned}$ | $\begin{aligned} & \text { MC34460 } \\ & \text { ME } 3446 \mathrm{P} \end{aligned}$ |  |
| 438 | 1820-1689 | 4 |  | IC MISC OUAD IC MISE OUAD | $\begin{aligned} & 04713 \\ & 04713 \end{aligned}$ | MEJ446P ME3446P |  |
| 439 | 1820-1689 | 4 |  | ic mise ouad |  |  |  |
| UaO | 1820-1144 | 6 |  |  | $01295$ | $8 \mathrm{NT4L802N}$ |  |
|  | $4040-0748$ $4040-0750$ | 3 | 1 | EXYRACTOR-PC BOARD BLK POLYC EXPAACPOREPC EOARD RED POLYE | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 4040=0740 \\ & 4040=0750 \end{aligned}$ |  |
| $\begin{aligned} & \text { MP } 3 B \\ & \text { MP } 3 C \end{aligned}$ | $03582-61613$ $1251-3283$ | 1 | 1 | HP-IB CONNECTOR W/CABLE <br> CONNECTOR 24-PIN F MICRORIBBON | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{gathered} 03582-61613 \\ 1251-3283 \end{gathered}$ |  |

## SERVICE GROUP 9

## PSEUDO RANDOM NOISE

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# PSEUDO RANDOM NOISE SERVICE GROUP 9 

### 8.9.1. INTRODUCTION.

8-9-2. The Pseudo Random Noise (PRN) generator is essentially a pseudo random binary generator that has its output processed by a digital filter (similar to a current output DAC). This signal is then band translated by a four quadrant multiplier, low pass filtered, and buffered before being presented at the front panel BNC connector (NOISE SOURCE OUTPUT). A switch on the NOISE SOURCE LEVEL control selects either a PERIODIC or RANDOM noise source. Random noise is extended periodic noise that is unsyncronized with the data collection time which makes it appear like a white noise source to the device under test and the 3582A.

## 8-9-3. GENERAL INFORMATION.

8-9-4. The PRN requires a clock signal and a sync signal from the Timing board C(A3) and also a cosine word from the Digital Local Oscillator portion of the A4 board (schematic E). Signature Analysis (SA) is the primary troubleshooting tool for the digital circuits. For the analog circuits, use a two channel oscilloscope to check the inputs and outputs of the various operational amplifiers.

Table 8-9-1. Troubleshooting Hints.

1. It is a good idea to check the following things first:
a. U17 pin 6 should be at +5 VDC . This can be adjusted with R33. An incorrect DC level will cause a "spike" at the center of the display in band analysis modes.
b. Set the center frequency to 1 kHz , move J 5 to "test" and check TP5 (L.O. test point) for a 3 Vp -p sin wave centered around zero.
c. Move J5 back to "run'.
2. Use the oscilliscope photos to check the analog circuits (current summer, mixer, low pass filter and buffer).
3. Use signature analysis to check the digital circuits. If a signature analyzer is not available, check for 5 V levels at the shift register outputs.

Table 8-9-2. PRN Signatures.
a. Move the test jumper (PRN J4) to Test.
b. Preset the board by momentarily shorting TP6 and 7.
c. Check U1-4, pins 3-6 and 10-13 for good 5V square waves.
d. Set up the 5004A as follows:

| GND: | $J 5(1)$ |  |
| :--- | :--- | :--- |
| Clock: | $J 5(3)$ | - |
| Start/stop: | $J 5(4,5)$ | $\boxed{ }$ |

3582A: Single channel; $0-25 \mathrm{kHz} \quad+5$ signature 3951
e. Troubleshoot using the following signatures:

| U1 \& 3 pin | 3 | P391 | U2 \& 4 pin | 3 | OOC2 |
| ---: | ---: | ---: | ---: | ---: | ---: |
|  | 4 | U1F8 |  | 4 | A5AO |
|  | 5 | 78P4 |  | 5 | U729 |
|  | 6 | 3F72 |  | 6 | HP6H |
|  | 10 | 9P39 |  | 10 | FAFU |
|  | 11 | FU1F |  | 11 | FO9P |
|  | 12 | P78P |  | 12 | F5C6 |
|  | 13 | 73F7 |  | 13 | F722 |
| U5 pin | 8 | 3551 |  |  |  |
| U5 pin | 3 | FU1F |  |  |  |
| U7 pin | 6 | 3UCO |  |  |  |



## NOTE

The Parts List for Service Group 9 is located in Service Group 3.




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## X-Y RECORDER

## SERVICE GROUP 10

## 8-10-1. INTRODUCTION.

8-10-2. The X-Y Recorder outputs are managed entirely by the Processor F(A7). The Processor latches binary data directly into the $Y$ and $X$ latches from the I/O Bus. The data is converted by DACS to a DC signal which is applied to a buffer driver circuit whose outputs result in the recorder drive signals at the rear panel. The Processor latches data at time intervals which approximate a constant slew rate for the recorder helping to eliminate curved line segments between data points.

8-10-3. A DAC voltage reference source is also located on this portion of the A10 board. Its outputs are also used by the Analog Display Driver DACS (schematic K).

### 8.10-4. GENERAL INFORMATION.

8-10-5. An internal self test is available for checking the DAC output voltages. The test causes the Processor to latch a known bit pattern into the DACS. The outputs can then be checked using a DC voltmeter (see Self-Tests).

## 8-10.6. RECORDER OUTPUT TEST (O00005) AVE \#128.

## 8-10-7. Function.

8-10-8. To test the X-Y recorder DAC's and the pen-lift relay, the X-Y recorder output registers are loaded with a word containing a single 1 bit and all the rest zeroes. Both the $\mathbf{X}$ and $Y$ registers are loaded with the same number, and the 1 bit is shifted each time this test is re-selected with the AVERAGE NUMBER and AVERAGE RESTART keys. Thus, a voltmeter can be used to check each bit of the DAC outputs.

8-10-9. For the X-Y output registers, bits $0-9$ are X-Y output bits, while bit 10 controls the pen-up relay. When the X-Y output word (see "condition code" paragraph 8-10-12) is octal 002000 , the pen-up relay should close, and the X-Y outputs should be zero.

## 8-10-10. Status Code.

8-10-11. CY only. Performs no internal checks for errors.

## 8-10-12. Condition Code.

8-10-13. Condition code 8 displays the octal number loaded into the X-Y output registers.



## NOTE

The Parts List for Service Group 10 is located in Service Group 5.

## SERVICE GROUP 11 POWER SUPPLY

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## POWER SUPPLY <br> SERVICE GROUP 11

## 8-11-1. INTRODUCTION.

8-11-2. The Power Supply Service Group contains information for troubleshooting the power supply control A17 board; the switching supplies A14, A15 and A16 boards; the linear supplies A18 board; the transformer, and the rectifier circuits. The linear supplies are used for low current circuits while the switching supplies power the remainder of the instrument. The power supply control A17 board generates the clock signal and reference voltages used by the switching supplies in addition to a raw +150 V for the display section.

Table 8-11-1. Table of Power Supply Use.

| Volts | Source | Schematic | Use | Volts | Source | Schematic | Use |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| +5 | A16 | T | $\begin{aligned} & \text { A1 } \\ & \text { A2 } \\ & \text { A3 } \end{aligned}$ | -15 | A18 | v | $\begin{aligned} & \text { A4 } \\ & \text { A10 } \\ & \text { A13 } \end{aligned}$ |
|  |  |  | A4 A5 | + 15 Isol | A18 | v | A1 |
|  |  |  | $\begin{aligned} & A 6 \\ & A 7 \\ & A 8 \end{aligned}$ | - 15 Isol | A18 | V | A1 |
|  |  |  | A8 A9 A10 | +150 Raw | A17 | V | A13 |
|  |  |  | $\begin{aligned} & \text { A11 } \\ & \text { A12 } \\ & \text { A13 } \end{aligned}$ | + 5 Ref | A17 | U | $\begin{aligned} & \text { A14 } \\ & \text { A15 } \\ & \text { A16 } \end{aligned}$ |
| + 7 | A15A | S | $\begin{aligned} & \text { A5 } \\ & \text { A7 } \end{aligned}$ | - 5 Ref | A17 | U | $\begin{aligned} & \text { A14 } \\ & \text { A15 } \\ & \text { A16 } \end{aligned}$ |
| +12 | A15B | S | $\begin{aligned} & \text { A2 } \\ & \text { A3 } \\ & \text { A4 } \\ & \text { A5 } \end{aligned}$ | + 18 Ref | A17 | U | $\begin{array}{r} \text { A15 } \\ \text { A16 } \end{array}$ |
|  |  |  | A6 A 7 | - 18 Ref | A17 | U | A14 |
|  |  |  | A8 | +24 Ref | A17 | U | $\begin{aligned} & \text { A14 } \\ & \text { A15 } \\ & \text { A16 } \end{aligned}$ |
| +18 | A15C | S | A4 A5 A13 | - 24 Ref | A17 | U |  |
| + 5 Raw | A18 | $v$ | A1 |  |  |  |  |
| +15 | A18 | v | A4 A10 A13 |  |  |  |  |

## 8-11-3. THEORY (Switching Supplies).

8-11-4. The switching power supply provides a very efficient means for regulating the voltage associated with high current demand. The principal component involved is the switching regulator which, when provided with the proper drive signal, switches between two states. When the switching regulator is turned on, the resistance between the input and output is very low. This low resistance dissipates very little power, even with high current flow. When the switching regulator is turned off, the resistance between the input and output is very high. This results in complete current cutoff and no power is dissipated by the device. With this criteria in mind, it can be easily realized that any prolonged delay in switching between the two states will result in high power dissipation and failure of the device. Therefore, the switching drive current and voltages must be of the proper magnitude to assure complete state change of the switching regulator. The drive signals to the switching regulator are developed from a 27 kHz clock signal modified by the current and voltage sense circuits.

8-11-5. The output from the switching regulator consists of pulses of high voltage and current. These pulses are filtered by a low pass network formed by a series inductor and a parallel capacitor. The voltage output is monitored by the voltage sense circuit which compares the monitored voltage to a known reference. If voltage output is low, the drive pulse remains on for a greater period of time. The current output is monitored across a low resistance series resistor located between the inductor and capacitor. The voltage drop across the resistor signals the current sense detector which turns off the switching hybrid. If the current demand is too great such as in the case of a short circuit, the current detector will signal the current sense latch causing an indicator red (current limit LED) to light and the output current to fold back.

## 8-11-6. TROUBLESHOOTING THE POWER SUPPLY SECTION.


#### Abstract

NOTE

Because damage may occur, boards should not be inserted into or removed from the chassis with power ON.


8-11-7. If supplies are down, remove all load by removing A1 through A10 boards and disconnecting A13J2. This will also eliminate damage to components on these boards. At this point go to the paragraph applying to the appropriate supply.

## 8-11-8. Determining Which Board Is Causing A Supply To Malfunction.

8-11-9. Because the supplies will operate without a load, use the following procedure to identify a malfunctioning supply or board.
a. Install the boards A1 through A10 and A13J2 one at a time until the problem board is found. Use information given in the Table of Power Supply Use.
b. When the affected board is found, the first thing to check is the decoupling capacitors for a short.
c. When all supplies are again working, reinstall A1 through A10 and A13J2.

## 8-11-10. Switching Supply Troubleshooting.

8-11-11. The switching power supplies are somewhat similar in design and operation. The series switching regulator responds to control pulses that vary in width according to output voltage and current variations which are sensed by the associated control circuitry.

8-11-12. If a power supply fails, it usually requires replacement of the switching regulator. This leads to the problem of trying to determine if the switching regulator was at fault or the associated control circuitry. Therefore before replacing the switching regulator, the control circuitry should be checked, otherwise, the new regulator may be immediately damaged upon application of line power to the instrument.

8-11-13. The proper operation of the control circuitry may be determined through the use of the following procedure.
a. Remove circuit boards A1 through A10 and unplug the connector on A13J2 to unload the supplies.
b. Remove the damaged power supply board from the instrument. Then plug an extender board (03582-66533) back into the slot for further troubleshooting use. Measure the output pin to ground to determine if the over voltage protection diode is shorted (see schematic).
c. Remove the two screws which hold down the switching regulator. Then, gently pry the regulator from its socket using a small flat bladed screwdriver.
d. Connect a 1 Kohm resistor (-hp- 0683-1025) between the ( + or - ) 50 V input to the switching regulator and the control input to the switching regulator (use Figure 8-11-1 and the proper schematic as a guide).
e. Place the power supply board on the extender in the 3582A.
f. Turn the LINE switch to ON and check the inputs to the power supply board (use the schematic for voltage references).


Figure 8-11-1. Initial Power Supply Test Setup.
g. Set up an oscilloscope for reading $\pm 80 \mathrm{VDC}$ and set the sweep for 10 usec . Connect the oscilloscope to the control input line of the switching regulator (see Figure 8-11-1).
h. If the power supply is positive, observe that pulses appear on the oscilloscope display and are similar to the ones shown in Figure 8-11-2. If the power supply is negative, the pulses will be inverted and positioned in the negative portion of the oscilloscope display (actual voltage levels may vary between instruments). If no pulses appear, troubleshoot the output transistors of the control circuitry; also check the clock signal for TTL levels. These pulses indicate maximum power output for the switching regulator.


Figure 8-11-2. Control Pulses For Positive Supply.
i. To check for voltage regulation, connect an external power supply with the same polarity between the voltage output test point and ground (for a positive supply, connect the positive output to the VO test point).
j. Increase the voltage on the external power supply until the PC board green LED indicator is on and the pulses on the oscilloscope display start to become narrower. This is the approximate output voltage of the supply under test. Further increase in voltage will cause the pulses to decrease in width, then disappear leaving a DC level (see Figure 8-11-3). If problems occur here, check the voltage sense amplifier. When finished with this portion of the check, disconnect the external power supply, but leave the oscilloscope connected for further checks.


Figure 8-11-3. Voltage Effects On Control Pulses.
k. The current limiting control circuit senses the voltage drop across a low resistance in the output line of the supply. On the +5 volt supply, this is actually a trace on the circuit
board. When the voltage drop exceeds the value associated with an overcurrent condition, the current sense circuit clears a flip-flop. This latches the pulse control circuits in a steady state, removing control pulses from the switching regulator, thereby causing it to shut down. The switching regulator will remain shut down as long as the overcurrent condition exists.

1. To simulate an overcurrent condition requires the use of an external power supply. Before connecting the supply, verify that the output voltage is set to zero. If the power supply under test is a positive supply, connect the negative output of the external supply to the voltage output test point. For negative supplies, connect the positive output from the external supply. Connect the other output from the external supply through a 1 Kohm resistor to the input of the current sense amplifier which as the opposite polarity to the supply under test. For example, if the supply under test is a positive supply, connect the positive output from the external supply to the negative input of the current sense amplifier using a 1 Kohm resistor (see Figure 8-11-4).


Figure 8-11-4. Setup For Current Limit Check.
m. Slowly increase the voltage on the external power supply until the PC board red LED lights, indicating that an overcurrent condition exists. Also notice that the pulses on the oscilloscope display have again returned to a DC level indicating that the switching regulator is turned off. For problems in this area, check devices for TTL logic levels and the current sense amplifier for turn on when both inputs are of equal voltage.

## 8-11-14. Power Supply A18.

8-11-15. For adjustment of -15 Volt isolated supply see Adjustment Procedure. The A18 board has the following supplies:
+15 volt
-15 volt
+15 volt isolated

- 15 volt isolated
+5 volt raw (for +5 volt isolated see A1 board A)

8-11-16. When all supplies are working, replace A1 through A10 and A13J2.

## 8-11-17. Power Supply Control A17.

8-11-18. If a problem seems to afflict more than one power supply, a good place to start troubleshooting is the A17 Power Supply Control board. Perform the following steps:
a. Remove all power supply boards.
b. Turn on the 3582A and verify the following voltages on connector XA17.

| Pin | Voltage |
| :---: | :---: |
| A | +50 Vdc |
| C | -50 Vdc |
| $12, \mathrm{~N}, 14, \mathrm{R}$ | 114 Vac |
| J | 9.2 Vac |
| L | 8.5 Vac |

c. If these voltages are incorrect, troubleshoot the transformer and rectifier circuits as indicated by the problem.
d. If these voltages appear to be good, turn the instrument OFF and plug in the A17 Power Supply Control board using an (03582-66533) extender board.
e. Turn ON the 3582A and measure the following voltages on the output pins.

f. Refer to Adjustments Section V if the $\pm 18 \mathrm{~V}$ or 27 kHz signals are not correct.
g. Reinstall all power supply boards after the reference voltages are restored.

8-11-19. When all supplies are working, replace A1 through A10 and A13J2.

## 8-11-20. Fan Retrofit Kits.

8-11-21. Two retrofit kits have been set up to change the fan in the -hp-3582A.
a. The LO VOL FAN KIT (PN 03582-68702) contains a quieter fan. This fan is recommended for applications where noise is objectionable.
b. The HI VOL FAN KIT (PN 03582-68703) contains a noisier fan. This fan cools the 3582A better and therefore increases its reliability and is recommended for applications where reliability is important.






CHASSIS MOUNTED COMPONENTS


3582-19C



CHASSIS MOUNTED
COMPONENTS

OHMS Readings of Secondary, T1*

| Pins | OHMS |
| ---: | ---: |
| 5 to 4 | 29.3 |
| 1 to 3 | 4.8 |
| 1 to 2 | 2.4 |
| 3 to 2 | 2.4 |
| 15 to 16 | 0.5 |
| 7 to 8 | 0.3 |
| 9 to 11 | 2.6 |
| 9 to 10 | 1.3 |
| 10 to 11 | 1.3 |
| 14 to 13 | 2.7 |
| 6 to all | Open |
| 12 to all | Open |

OHMS Readings of Primary, T1*

| Power plug @ 240v | $7.9 \Omega$ |
| :--- | :--- |
| Power plug @ 220 v | $7.1 \Omega$ |
| Power plug @ 120 v | $2.3 \Omega$ |
| Power plug @ 100 v | $2.2 \Omega$ |
| 0 to 40 | $3.8 \Omega$ |
| O to 3 | $0.8 \Omega$ |
| 50 to 20 | $4.0 \Omega$ |
|  |  |
|  |  |




Figure 8-11-8. Power Supply Control.



Figure 8-11-9. Linear Power Supply.

Table 8-11-2. Replaceable Parts.

| Reference Designation | HP Part Number | C | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 414 | 03582-60514 | 4 | 1 | PC ASSEMBLY, - ISV POWER SUPPLY | 28480 | 03582-66514 |
| $\mathrm{C}_{1}$ | 0180-0309 | 4 | 18 | CAPACITOR-PXD 4.7UF+-20X 10 VDC TA | 56289 | $1500475 \times 001042$ |
| $C_{2}$ | 0180-0309 | , |  | CAPACITOR-FXD 4.7UF*-20x 10 VOC TA | 56289 | 1500475x001042 |
| 63 | 0160-3622 | 8 |  |  | 28480 | 0160-3622 |
| ${ }^{\text {c }}$ | 0180-0116 | 1 | 24 |  | 56289 | 1500685×903502 |
| ${ }^{5}$ | $0160-0300$ | 3 | 2 | CAPAEITOR-PXD 2700PF +610X 200VDC POLYE | 28480 | 0160.0300 |
| 66 | 0160-2204 | 0 | 3 | CAPACITOR-FXD 100PF +65x 300VOC mICA | 28480 | 0160-2204 |
| 67 | 0160-2055 | , | 4 | CAPACITOR-FXD . O1UF +80-20X 100 VOC CER | 28480 | $0160-2055$ |
| ${ }^{\text {cha }}$ | 0160-3622 | 8 |  | CAPACITOR-FXO 1 IUF +80-20X 100 VOC CER | 28480 | 0160.3622 |
| 60 $C 10$ | $0160-3450$ $0160-3456$ | 6 |  | CAPAEITOR-FXD CAPAEITOR | 28480 28480 | $0160-3456$ $0160-3456$ |
| $C_{11}$ | 0180-0309 | 4 |  | CAPACITOR-FXD 4, TUF+-20X 10 VOC TA | 56289 | $1500475 \times 001042$ |
| ${ }^{1} 12$ | 0180-2687 | 5 |  | CAPACITORAPXO 47UF+100-10\% 100 VOC AL | 28480 | 0180-2687 |
| ${ }^{1} 13$ | 0160-3622 | 8 |  | CAPACITOR-FXO - 1UF $+80-20 \mathrm{X}$ 100VDC CER | 28480 | $0160=3622$ |
| $\mathrm{Cl}_{14}$ | 0180-2686 | 4 |  | CAPACITOR-FXO A7OUF+100-10x 25VDC AL | 28480 | $0180-2686$ |
| C15 | 0160-3622 | 8 |  | CAPAEITOR-FXD .1UF +80-20X 100 VOC CER | 28480 | 0160.3622 |
| C16 | 0160-3456 | 6 |  | CAPACITOR-FXD 1000PF +-102 1 KVDE CER | 28480 | 0160-3456 |
| $\mathrm{Caz}_{2}$ | 1901-0040 | 1 |  | OIODESSWITCHING 30V SOMA $2 N 8$ DO-35 | 28480 | 1901-0040 |
| Co3 | 1902-0202 | 9 |  |  | 28480 | 1902.0302 |
| $\mathrm{CR}_{5}$ | 1901-0026 | 3 |  | DIODE-PWR RECT 200 V 750 MA 00-29 | 28480 | 1901-0026 |
| OS DS4 | $\begin{aligned} & 1990=0486 \\ & 1990=0485 \end{aligned}$ | 6 5 | 6 | LEO_VIBIELE LUM-INTEIMCD IF:2OMA_MAX-RED LED-VISIBLE LUM-INT=BOOUCD IF=3OMA-MAX-GRN | 28480 28480 | $\begin{aligned} & 5082=4684 \\ & 5082-4984 \end{aligned}$ |
| $F_{1}$ | $\begin{aligned} & 211000043 \\ & 2110-0269 \end{aligned}$ | $\begin{aligned} & 8 \\ & 0 \end{aligned}$ | 3 | FUSE 1.5A 250 V FASTa8LO 1.25X. 25 UL IEC FUSEMOLOER-CLIP TYPE.2SD.FUSE | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 2110=0043 \\ & 2110=0269 \end{aligned}$ |
| L 1 | 9140.0244 | 1 |  | Inductor 1MH | 28480 | 9140.0244 |
| 01 | 1854-0215 | 1 |  | TRANEISTOR NPN SI PDE350mm Fiz 300 MHZ | 04713 | SPS 3611 |
| 82 | 1854-0215 | 1 |  | TRANSISTOR NPN SI PDU350Mm Fiz 300 MHZ | 04713 | 3 Pa 3611 |
| 03 | 1853-0210 | 4 | 1 | TRANSISTOR PNP SI TO-39 PDEIW FTESOMHZ | 28480 | 1853-0210 |
| $R 1$ $R 2$ | $0683-1505$ $0683-1505$ | 0 | 13 |  | $\begin{array}{lllll}0 & 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1\end{array}$ | ces 505 ces 505 |
| R3 | 0683-1525 | 4 | 15 | RESISTOR 1,5K 5x. 25 W FC TCE=400/4700 | 01121 | CB1525 |
| R4 | 0683-1525 | 4 |  | RESISTOR 1.5K 5X . 25W FE TE $=-400 /+700$ | 01121 | CBI525 |
| R5 | 0683-2725 | 8 | 7 | RESISTOR 2,7K 5\% .25w FC TCa-400/4700 | 01121 | C82725 |
| R6\% | 0683-3915 | 0 |  | RESISTOR 390 5x \% 25 W FC TCM-400/ 4600 | 01121 | C83915 |
| R 7 | 0683-1025 | 9 |  | RESISTOR 1 K 5X, 25 W FC TCE-400/4600 | 01121 | CB1025 |
| Rs | 0683-2725 | 8 |  |  | 01121 | C82725 |
| R9 | 0683-1525 | 4 |  | RESISIOR 1.5K 5X, 25 W FC TCE $=400 / 4700$ | 01121 01121 | 681525 |
| R10 | 0683-1035 | 1 | . 23 | RESISTOR LOK 5x.25W FC TCE=400/4700 | 01121 | C81035 |
| R11 | 0683-1035 | 1 |  | RESISTOR 10 K 5X. 25 W TE TCE=4000 $1+700$ | 01121 | C81035 |
| R12 | 06833.4725 | 2 |  |  | 01121 0 0 | CB4725 CBIO25 |
| R13 R14 R15 | $0683-1025$ $0683-1035$ | 9 |  |  | 01121 01121 | C81025 CE1035 |
| $R_{15}$ | 0683-1035 | 1 |  | RESISTOR IOK SX, 25W FE TE= $04001+700$ | 01121 | C81035 |
| R16 | 0683-1025 | 9 |  | RESISTOR IK 5X, 25W FC TCE=400/4600 | 01121 | C81025 |
| $\mathrm{R}_{17} 7$ | 0683-1015 | 1 |  | RESISTOR 100 5x.25H FC TC $=-400 /+500$ | 01121 | CB1015 |
| R18 | 0683.1035 | 1 |  | RESISTOR LOK 5X. 25W FE TC=-400/+700 | 01121 | CB1035 |
| R19 | 0683-1015 | 7 |  | RESISTOR 100 5x, 25W FC TC= $=400 / \$ 500$ | 01121 | C81015 |
| R20 | 0683-1505 | 0 |  | RESISTOR 15 5x, 25W FC TC=0400/4500 | 01121 | ceisos |
| R21 | 0683-1505 | 0 |  | RESISTOR 15 5x, 25w FC TCE-400/4500 | 01121 | CB1505 |
| R22 | 0683-1035 | 1 |  | RESISTOR 10K 5X. 25w Fe TCE=400/*700 | 01121 | CB1035 |
| R23 | 0757-0442 | 9 |  | RESISTOR 10K $1 \times .125 \mathrm{WF}$ TC=0¢-100 | 24546 | C4-1/8-T0-1002-F |
| R24 | 0683-1035 | 1 |  | RESISTOR 10K 5\% . 25w FE TCE-400/*700 | 01121 | C81035 |
| R25 | 0683-4715 | 0 |  | RESISTOR QT0 5x. 25 W FC TCE-400/\$600 | 01121 | c84715 |
| R26 R27 | $0683-4705$ 0698.3582 | 8 |  |  | 01121 24546 | $\begin{aligned} & \text { CB4705 } \\ & \text { Ca-1/8-T0-4122-F } \end{aligned}$ |
| Res | 0757-0404 | 3 | 1 |  | 24546 | C4-1/8-T0-131-F |
| R29 | 0811-1826 | 1 |  | RESISTOR .05 10X 3W PW TCa04-200 | 28480 | 0811-1826 |
| R30 | 0687-1021 | 3 |  | RESISTOR iK 10X.5W CC TCEO\$647 | 01121 | EB1021 |
| 42 | $1826=0026$ | 3 |  | IC 311 COMPARATOR TO-99 | 04713 | mLM316 |
| U4 | 182600026 | 3 |  | IC 311 COMPARATOR T0-99 | 04713 | MLM31i6 |
| US | $\begin{aligned} & 1813=0084 \\ & 1205=0247 \end{aligned}$ | 4 | 1 | IC $10-66$ SW-REG <br> HEAT 日INK TO-6b-PKG | 12969 28480 | PIC611 12050247 |
|  | 03582-01103 | 1 | 1 | heat bink | 28480 | 03582-01103 |
|  |  |  |  | MISCELGANEDUS PARTA |  |  |
|  | $\begin{aligned} & 4040-0749 \\ & 4040=0752 \end{aligned}$ | 4 | 1 | EXTRAETOR-PE BOARD GRN POLYE EXTRACTOR-PC BDARD YEL POLYC | $\begin{aligned} & 28480 \\ & 28460 \end{aligned}$ | $\begin{aligned} & 4040=0749 \\ & 4040-0752 \end{aligned}$ |
|  |  |  |  | NOTE: THE SOLDER BUCKET 1251-2551 IS NO LONGER USED ON THE SWITCHING REGULATOR, U1. |  |  |

Table 8-11-2. Replaceable Parts (Cont'd).


Table 8-11-2. Replaceable Parts (Cont'd).


Table 8－11－2．Replaceable Parts（Cont＇d）．

| Reference Designation | HP Part Number | c | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 116 | 03582066516 | － | 1 | －C ASEEMELY，＋5V PONER SUPPLY | 20480 | 03582－06516 |
| C1 | 018002687 $0160-3622$ |  |  |  | 28480 28480 | －1180－20097 |
|  |  | 5 | ！ |  |  |  |
|  |  | 5 | 1 |  | 28480 56289 | 110000154 $150045 \times 0010 \wedge 2$ |
| ${ }^{\text {cos }}$ | 018000309 01800 01800 0 | 4 |  |  | 56280 <br> 56280 | $1500497 \times 001012$ 1500475001012 |
| ${ }^{\text {ch }}$ |  |  |  |  | （362809 | （150945x ${ }^{\text {a }}$ |
| ${ }_{\text {cid }}$ | 0116002055 $0160-3622$ | ！ |  |  | 283808 28480 |  |
| ${ }_{\text {c }}^{1}$ | －0．160－3622 ${ }_{0}^{160-3456}$ | ． |  |  | 28880 28480 2800 | $01100-3622$ 0 0 |
|  |  | － |  |  |  |  |
| $\begin{aligned} & \text { CRR } \\ & \text { CRR } \\ & \text { Ras } \end{aligned}$ |  | 3 | 3 |  <br>  |  |  |
| 2083 | 199000485 | 5 |  | LEDDISIBLE LUM－INTEBOOUED IFEJOMA－MAX－GRN LDDVISIGLE LUM－INTEIMCD IFEZOMA－MAX－RED | $\begin{aligned} & 28480 \\ & 2800 \end{aligned}$ | S082－49894 |
| $\ldots$ | $\begin{aligned} & 2110-0043 \\ & 211000269 \end{aligned}$ | ： |  |  | $\begin{aligned} & 28400 \\ & 2480 \end{aligned}$ | 211000043 211000269 |
| 4 | 914000243 | － | 1 | INDUCTOR 150．84 | 28480 | 914000243 |
|  |  | － |  |  Transistor pap si ponsion ptiainhz |  |  |
| ${ }_{\text {Ras }}$ | 年083－16015 |  | $10^{1}$ |  | O1121 |  |
| ${ }_{\text {Rog }}^{\text {Rob }}$ |  |  |  |  | Sill | citisios |
| ${ }_{88}^{89}$ |  | 。 |  |  | － 01121 | ctisos |
| ${ }^{\text {R9 }}$ | 0663－1023 |  |  |  | 01121 | ${ }^{6} 810205$ |
| R210 | － 06033 O6095 |  | 1 |  | － 01121 | cotios |
|  |  |  |  |  | －01121 |  |
| R19 | － 0683 －6823 |  | 2 |  | 01121 01121 |  |
| SR16 |  |  |  |  | 0121 | ${ }_{\text {coid }}$ |
| R18 |  | 2 |  |  | （ 01121 | ciliols |
| R19 | 2100－3273 |  |  |  | 28400 | 21000323 |
|  | － |  |  |  | 21121 | cisos |
| ${ }^{\text {R22 }}$ | － 0 06331015 | ？ |  |  | 01121 0121 |  |
| R284 | － $0083-1025$ |  |  |  | －01121 |  |
|  | － |  |  |  | （01121 |  |
| R28 | $0757-0442$ | ！ |  |  | 24546 | C4－1／8－T0－1002．F |
|  | － $\begin{aligned} & \text { 0683－1025 } \\ & 069894480\end{aligned}$ |  |  |  | 01121 24546 |  |
|  |  | $\stackrel{1}{5}$ | ： |  |  | 边 |
| ${ }_{\text {R33 }}$ |  | ！ | 1 |  | cis |  |
| ${ }^{2385}$ | 年0633－1035 | ， | 1 |  <br>  | － 01121 | ceioss |
| $\begin{aligned} & u_{1}{ }_{2}^{2} \\ & u_{2}^{2} \\ & u_{3} \\ & u_{5} \end{aligned}$ | 826－0026 <br> $1826+002$ <br> $1820-1199$ $1820-1112$ <br> 182001112 <br> $1251-1636$ <br> $03582-01101$ |  | － | IE 311 companator To－90 <br> It INV THL LS MEX <br>  <br>  | $\begin{aligned} & 04713 \\ & 04713 \\ & 01295 \\ & 01295 \\ & 12968 \\ & 28080 \\ & 28480 \end{aligned}$ | MLM3116 <br>  ontalatan 1251－1636 |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  | $3_{1}^{3}$ |  |  |  |
|  |  |  |  | iscellaneous |  |  |
|  | 200000749 | ${ }_{1}$ | 2 |  | 28880 | 90900749 |

See introduction to this section for ordering information

Table 8-11-2. Replaceable Parts (Cont'd).


Table 8-11-2. Replaceable Parts (Cont'd).


Table 8-11-2. Replaceable Parts (Cont'd).


Table 8-11-2. Replaceable Parts (Cont'd).


Table 8-11-2. Replaceable Parts (Cont'd).


SERVICE GROUP 12
CHASSIS MOUNTED COMPONENTS

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## CHASSIS MOUNTED COMPONENTS SERVICE GROUP 12

## 8-12.1. INTRODUCTION.

8-12-2. This service group contains information concerning the replacement of the CRT, Mother board diagram, and chassis mounted components not covered in other service groups.

## 8-12-3. CHASSIS MOUNTED COMPONENTS CROSS REFERENCE.

8-12-4. Use the following cross reference to determine the service group which contains the part numbers for a particular part grouping.

| Part Group | Service Group |
| :--- | :---: |
| Cables | 12 |
| CRT | 12 |
| Fan | 11 |
| Frame Parts | 12 |
| Front Panel | 7 |
| Power Supply | 11 |
| Miscellaneous Parts | 12 |
| Rear Panel | 11 |

## 8-12-5. REPLACING THE CRT.



The CRT and associated circuits may retain lethal voltages (up to 18 kV ) even when the instrument power is off.

## 8-12-6. General Information.

8-12-7. Before removing CRT, be sure that instrument power is off and allow sufficient time for circuits to discharge. Handle the CRT with care!

8-12-8. Perform the following steps:
a. Remove the top and bottom instrument covers.
b. From the bottom of the instrument, remove the screw retaining the CRT shield ground lug.
c. Unplug the post accelerator cable (red) and ground the CRT end to the chassis. Then connect clip lead between the HV lead and ground. Be careful of the high voltage hazards!
d. Remove the plastic shield over the A13 board.
e. Unplug the two Molex connectors in the center of the A13 board (that have wires leading to the pin connectors).
f. Remove the remaining screws (standoffs) holding the A13 board to the chassis. The A13 board may be swung up leaving other cables attached.
g. Using a flat-bladed screwdriver, carefully pry off the connector at the rear of the CRT.
h. Remove the retaining band that clamps the CRT shield to the chassis.
i. With the A13 board swung aside, the CRT may be pulled upward and backward away from the instrument chassis.
j. To remove the CRT from the shield, perform the following steps:

1. Disconnect the wires at the pin connectors at the side of the CRT.
2. Loosen the screws of the alignment coils (2 each).
3. Place the CRT face on a soft surface. Then while holding the shield with both hands, press on the rear of the tube with the thumbs forcing the tube forward and out of the shield.
4. Remove the foam ring from the rear of the CRT shield.
k. Reinstall the CRT using the general procedure for removal in reverse order. Be careful that the following points are observed.
5. Slide the CRT into the shield so that the neck and connectors line up with the slots.
6. Press forward on the alignment coils screws (at the side) to secure the coil against the CRT neck before tightening.
7. Replace the foam ring at the rear of the CRT shield, sliding it just far enough on the CRT neck so that there is no interferrence to the rear connector.
8. Perform high voltage section adjustment and alignment.


Figure 8-12-1. Mother Board (Bottom Side).



Figure 8-12-3. CRT Assy Exploded View.

## CATHODE-RAY TUBE FAILURE REPORT

(This form must accompany all warranty claims and MFR/HEART credit claims.)

## Date

Submitted By (Name) $\qquad$
Name of Company $\qquad$
Address $\qquad$

1. Hewlett-Packard Instrument Model No. $\qquad$
2. Hewlett-Packard Instrument Serial No. $\qquad$
3. Defective CRT Serial No. $\qquad$ Part No. $\qquad$
4. Replacement (New) CRT Serial No.
5. Please describe the failure and, if possible, show the trouble on the appropriate CRT face below.
$\qquad$
$\qquad$
$\qquad$
$\qquad$
$\qquad$
$\qquad$

6. Is a warranty claim being made?
7. Hewlett-Packard Sales/Service Office $\qquad$
8. MFR, HEART or Customer Service Order Number $\qquad$

Table 8-12-1. Replaceable Parts.


Table 8-12-1. Replaceable Parts (Cont'd).

| Reference Designation | HP Part <br> Number | $\begin{aligned} & \mathbf{C} \\ & \mathbf{D} \end{aligned}$ | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Chassis mounted components |  |  |
| "EPP1 |  |  |  |  | 28480 |  |
| ER2 | $01332-66001$ | 8 | 1 | COIL. ORTHO | $28480$ | $01332=66001$ |
| EP3 | 01701-66001 | 5 | 1 | COIL, X -AXIS |  |  |
| MP5 | 03582.04104 | 8 |  | GUARD, FAN SWITCH | 28480 | 03582-04104 |
| MPQ | 03582-00201 | 8 <br> 4 | 1 | PANEL, LEFT | 28480 28480 | $03582-00201$ 0358200215 |
| MP10 | $03582-00215$ $03582-00222$ | 4 | 1 | Plate, CUTOUT | 28480 28480 | 03582-00215 |
| mpit | 03582-20601 | 4 |  | SHIELD, TERM | 28480 | 03582-20001 |
| MP 13 | 03582-00601 | 2 | 2 | SHIELD, INPUT | 28480 | 03582-00601 |
| MP 14 | 03582-00602 | 3 | 1 | SHIELD, DISPLAY | 28480 | 03582-00602 |
| MP 15 | 03582-00603 | 4 | 1 | COVER, CARD NEST | 28480 | 03582-00603 |
| MP 16 | $03582=00605$ $03582=01201$ | 6 0 | 1 | SHIELO, TRANSFORMER BRACKEF, TRANSFORMER | 28480 28480 | $03582=00605$ $03582-01201$ |
|  | 03582-01201 | 0 | 1 | BRACKEY, TRANSFORMER |  |  |
| MPI 18 | 03582-01202 | 1 | , | SRACKET, RECT. | 28480 | 03582001202 |
| MPI MP 20 | 03562001209 0358201210 | $\cdots$ | 1 | GRACKET, H.V.P.S. | 28480 28480 | $03562-01209$ 03582001210 |
| mpzo Mp 21 | $03582-01210$ $03582-01211$ | 1 | 1 | GRACKET, CAP. | 28480 28480 | $03582=01210$ $03582=01211$ |
| MP 21 MP 22 | $03582-01211$ $03582-01216$ | $\frac{2}{7}$ | 1 | CARD GUIDE, REAR | 28480 28480 | $03562-01211$ $03582-01216$ |
| MP 23 | 03582-01219 | 0 | 1 | BRACKET, CARD NEST | 28480 | 03582-01210 |
| MP24 | $03582-01225$ 03582004101 | 8 | 1 | SRACKET, TRANSFORMER SHIELO | 28480 28480 | 03582.01225 03582004101 |
| MP 25 | $03582-04101$ $03582-04103$ | 5 | 1 | INSULATOR, CAP | 28480 28480 | $03582-04101$ $03582-04103$ |
| MP 26 MP 21 | $03582-04103$ $03582-04105$ | 9 | 1 |  | 28480 28480 | $03582-04103$ 03582004105 |
| MP 28 | 03582-04106 | 0 |  | INSULATOR, AMPLIFIER BOARD | 28480 | 03582004106 |
| MP29 | 03582-22701 | 9 | $\frac{1}{3}$ | FILTER, GRAY | 28480 | 03582-22701 |
| MP 30 | 03582-24702 | 4 | 3 | SPACER, AMPLIFIER BOARD A13 ASSY | 28480 | 03582-24702 |
| MP 31 | 03582-24703 | 5 | 3 | SPACER, CUTOUT AI3 ASSY | 28480 | 03582-24703 |
| MP 32 | 03582-60101 | 3 | 1 | CHASSIS ASSEMBLY | 28480 | 03562-60101 |
| MP33 | 03582-60103 | 5 | 1 | SHIELO, CRT | 28480 | 03582-60103 |
| MP34 | 03582060201 | 4 | 1 | SHIELO ASEEMBLY | 28480 | $03582=60201$ |
| MP 35 | 0905-0573 | 2 | 1 | GASKET, ROUND, NPRN | 28480 | ${ }^{0905050573}$ |
| MP 36 MP 37 | $1400-0906$ $1960-1345$ | 6 5 | 1 2 |  | 08484 28480 | $08200-\mathrm{M} 40 \mathrm{H}$ $1400=1345$ |
| MP 38 | 5001-0440 | 1 | 2 | YRIM, SIDE | 28480 | 5001-0440 |
| MP 39 | $5020-8805$ | 8 | 1 | FRAME: FRONT | 28480 | 5020-8805 |
| MPaO | 5020-8806 | 9 | 1 | FRAME: REAR | 28480 | 5020-8806 |
| MP41 | $5020-8837$ | 6 | 4 | STRUT: CORNER | 28480 | $5020-8837$ |
| MP42 | 5040-1023 | 2 | 1 | Pushrod | 28480 | 5040-7023 |
| Mp43 | 5040-1201 | 8 | 4 | FODT(STANOARD) | 28480 | 5040-7201 |
| MPu4 | 5040-1202 | $\stackrel{ }{ } \cdot$ | 1 | TRIM, POP | 28480 | 5040-7202 |
| MP45 | 5040-7219 | 8 | 2 | STRAP, HANDLE, CAP-FRONT | 28480 | 5040-7219 |
| MP40 | $5040=1220$ $5040-8393$ | 1 | 2 1 | STRAP, HANDLE, CAPGREAR SUPPORT, CARD | 28480 28480 | $5040-7220$ $5040-8393$ |
| mpas | 5040-8304 | 2 |  | caro guide, front | 28480 | 5040-0394 |
| MP49 | 5040-8309 | 7 | 1 | BEZEL, CRT | 28480 | 5040-8309 |
| MP50 | 5060-1474 | 9 | 1 | BEREL, FRAME | 28480 | 5060-7474 |
| MPS 1 | 5060-9804 | 3 | 2 | STRAP HANDLE, 18 IN. | 28480 | 5060.9804 |
| MP52 | 5060-9835 | 0 | 1 | TOP COVER | 28480 | 5060-9835 |
| MP5 3 MP5 | 5060-9847 | 4 | $\frac{1}{2}$ | BDTTOM COVER | 28480 28480 | 506009847 5060099 |
| MP54 MPS5 MP | $5060-9942$ 506102009 | 0 | 2 | SIDE COVER | 28480 28480 | $5060-9942$ 506102009 |
| MP5 6 | 5061-2033 | 8 | 1 | CARO HOLOER | 28480 | 5061-2033 |
| MP5 7 | 9320-3885 | 4 | 1 | SNSTRUCTION CARD | 28480 | 9320-3885 |
| MP58 MPS M | $9320-3886$ 032400094 | 5 | 1 | HPOIB INBTRUETION CARD ISOLATOR CRT | 28480 28480 | $\begin{aligned} & 9320=3886 \\ & 4324=0094 \end{aligned}$ |
| MP60 | $4320-0325$ | 6 | 2 | POMM. PDWER SUPPLY SUPPDRT | 28480 | 4320-0325 |
| MP6 12 MP6 2 | $\begin{aligned} & 4324-0095 \\ & 03582-00204 \end{aligned}$ | 5 1 | 2 | POAM, CARD NEST IUPPORT FRONT CARD NEST SUPPORT | 28480 28480 | $\begin{aligned} & 4324.0095 \\ & 03582-00204 \end{aligned}$ |
| 32 | 3101-2216 | 3 |  | SWITCM-PB DPD altng an zsovac line sw | 28480 | 3101-2226 |
| 11 | -100-4063 | 6 | 1 | TRANSFDRMER, LINE | 28480 | -100-6063 |
| W23 | 8120-1521 | 6 | 1 | CABLE ASBY IBAWG J-CNDCT JGK-JKT (AC PWR CRD) | 28480 | 8120-1521 |
|  |  |  |  | = \%FOR INSTRUMENTS WITH CRT SERIAL NUMBER 5083-5788, THIS IS A DIRECT REPLACEMENT TUBE AND DOES NOT REQUIRE CIRCUIT MODIFICATION. |  | - |

Table 8-12-1. Replaceable Parts (Cont'd).

| Reference Designation | HP Part Number | Oty | Description | $\mathrm{Mfr}$ Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\text { [ } \begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ |  |  |  |

## CATHODE-RAY TUBE FAILURE REPORT

(This form must accompany all warranty claims and MFR/HEART credit claims.)

Date $\qquad$
Submitted By (Name) $\qquad$
Name of Company $\qquad$
Address $\qquad$

1. Hewlett-Packard Instrument Model No $\qquad$
2. Hewlett-Packard Instrument Serial No. $\qquad$
3. Defective CRT Serial No $\qquad$ Part No $\qquad$
4. Replacement (New) CRT Serial No.
5. Please describe the failure and, if possible, show the trouble on the appropriate CRT face below.
$\qquad$
$\qquad$
$\qquad$
$\qquad$
$\qquad$
$\qquad$

6. Is a warranty claim being made? $\qquad$
7. Hewlett-Packard Sales/Service Office
8. MFR, HEART or Customer Service Order Number

# (hp) MANUAL CHANGES 

hp- MODEL 3582A

## SPECTRUM ANALYZER

Manual Part Number 03582-90004

1All New Items
This supplement contains important information for correcting manual errors and for adapting the manual to instruments containing improvements made after the printing of the manual.

To use this supplement:

1. Make all Manual ERRATA changes.
2. Make all additional changes that pertain to your instrument serial number only.

## errata

Page 7-A-5/7-A-6, Figure 7-A-2. Change the Figure number to 8-1-12. Change the page number to 8-1-15/8-1-16. Add REV $F$ to the Figure title. Add the component locator in Figure 1. Move the page to section $8-1$.

Page 8-1-15/8-1-16, Figure 8-1-12. Change the Figure number to 7-A-2. Change the page number to 7-A-5/7-A-6. Move the page to section 7-A.

## CHANGE NUMBER 1 for all Serial Numbers.

Pages 8-1-3/8-1-4, 8-1-5/8-1-6, 8-1-7/8-1-8, and 8-1-13/8-1-14. Update the component locator according to Figure 1.

Page 8-3-20, Table 8-3-2. Change the part number and description of U16 and U18 to 1826-0111 OPAMPL MC1458G. Change the part number of U17 to 1826-0866.

Page 8-6-15/8-6-16, Table 8-6-1. Change the part number and description of A3 to 0960-0491 MULT HI VOLT.

Page 8-7-3/8-7-4, Figure 8-7-2. Add SEE NOTE to part numbers 0370-1006 and 0370-3013. Add the following note:

## NOTE

For instruments with Serial Numbers through 1809A03324, if the potientometer is replaced with part number 2100-3737, replace knob 0370-1006 with 0370-3048 and 0370-3013 with 0370-3049.

For instruments with Serial Numbers 1809A03325 and greater, use part number 0370-3048 instead of 0370-1006 and 0370-3049 instead of 0370-3013.

Page 8-7-7; Table 8-7-1. Change the part number for R17 to 2100-3983. Change R17 to **R17. Add "*For instruments with Serial Numbers through 1809A03324, if the potientometer is replaced with part number 2100-3737, replace knob 0370-1006 with 0370-3048 and 0370-3013 with 0370-3049.


Figure 1.

Page 8-7-9, Table 8-7-1. Add SEE NOTE to part numbers 0370-1006 and 0370-3013. Add the following note:

## NOTE

For instruments with Serial Numbers through 1809A03324, if the potientometer is replaced with part number 2100-3737, replace knob 0370-1006 with 0370-3048 and 0370-3013 with 0370-3049.

For instruments with Serial Numbers 1809A03325 and greater, use part number 0370-3048 instead of 0370-1006 and 0370-3049 instead of 0370-3013.

Page 8-7-10, Table 8-7-1. Add 1460-1581 HOLD DOWN SPRING.
Page 8-11-15/8-11-16, Figure 8-11-8. At the left end of the A17 schematic, change the voltage value of A17CR11 and A17CR12 to 24 V .

Page 8-12-9, Table 8-7-1. Add 1460-1581 HOLD DOWN SPRING.
Page 8-12-10, Table 8-12-1. Change the following part numbers and descriptions:

MP30 0380-1228 SPACER-AMPL
MP31 0380-1227 SPACER-CUTOUT
Add 0380-1229 SPACER RPG BD to the parts list.

CHANGE NUMBER 2 for Serial Numbers 1809A02186 and greater.

Page 8-4-26, Table 8-4-3. Add R43 0683-1335 RESISTOR FXD $13 \mathrm{~K} 5 \% .25 \mathrm{~W}$ to the parts list. Change the part number and description of R16 to 0683-5625 RESISTOR FXD 5.6K $5 \%$.

CHANGE NUMBER 3 for Serial Numbers 1809A02336 and greater.

Page 8-5-24, Table 8-5-3. Change the part number of U15 and U17 to 1826-0582.

Page 8-8-15, Table 8-8-12. Change the part number and description of C5 to 0180-0374 CAPACITOR FXD 10 UF 20V.

CHANGE NUMBER 4 for Serial Numbers 1809A02406 and greater.

Page 8-8-13/8-8-14, Figure 8-8-1. In the lower left corner of the schematic, add a resistor ( R 17 , value 10) in parallel with the coil of L1 that is connected to ground.

Page 8-8-15, Table 8-8-12. Add R17 0683-1005 RESISTOR 10 5\%.

CHANGE NUMBER 5 for Serial Numbers 1809A02436 and greater.

Page 8-3-19, Table 8-3-2. Delete C7, C8, and C9.
Change the following parts:

```
C2 0160-0134 CAPACITOR FXD 220PF 300V
R33 2100-3350 RESISTOR VAR 200
R34 0757-0430 RESISTOR FXD 2210
R35 0698-3152 RESISTOR FXD 3480 1%
```

Add the following parts:

```
CR1, CR2 1901-0518 DIODE - SI
CR3, CR4 1091-0025 DIODE - HOT CARRIER
```

Page 8-3-20, Table 8-3-2.
Delete R37 through R45, R52 through R55, R57, R59,R62, R63, and U15

Change the following parts:
U14 1826-0356 CNVTR AD 7530AD
R56 0698-4435 RESISTOR FXD 2490 1\%
Add the following parts:

| R69, R70 0699-0059 RESISTOR FXD 5K |  |  |
| :--- | :--- | :--- |
| R71 | $0698-4436$ RESISTOR FXD 2800 | $1 \%$ |
| R72 | $0757-0283$ RESISTOR FXD 2000 | $1 \%$ |
| R73 | $0688-5115$ | RESISTOR FXD $510 \quad 5 \%$ |

CHANGE NUMBER 6 for Serial Numbers 1809A02465 and greater.

Page 8-5-19/8-5-20, Figure 8-5-6. In the center top portion of the schematic, change the values of R12 to $1.24 \mathrm{~K}, \mathrm{R} 13$ to 1.91 K , and R10 to 1 K .

Page 8-5-23, Table 8-5-3. Change the part numbers and descriptions of the following parts:

Q4 1854-0094 TRANSISTOR - 2 N3646
R12 0698-3223 RESISTOR 1.24K $1 \%$. 125 W
R13 0698-4430 RESISTOR 1.91K $1 \%$. 125 W
Delete the entries for R10** and add R10 0683-1025 RESISTOR 1000 5\% .125W.

CHANGE NUMBER 7 for Serial Numbers 1809A02976 and greater.

Page 7-H-1/7-H-2. Change "REV A\&B" TO "REV A\&B 3582-66508."
CHANGE "Rev C board" to $3582-66508$ Rev C board."
Add
REV C 3582-66508
Schematic
Use the schematic provided in this section.
Troubleshooting
Use the trouble shooting procedures provided in this section.

Page 8-4-17, Paragraph 8-4-34. Change the heading to "TROUBLESHOOTING THE 03582-66508 RAM ASSEMBLY."

Pages 8-4-17 through 8-4-24. Renumber the pages to $7 \cdot H-3$ through $7 \cdot \mathrm{H}-11$. Renumber Figure $8-4-5$ to $7 \cdot \mathrm{H} \cdot 1$. Resequence the paragraph numbers starting with $7-\mathrm{H}-1$. Move these pages to section 7-H. Insert the attached pages 8-4-17 through 8-4-24 into section 8-4.

Page 8-4-29/8-4-30, Table 8-4-3. Add the following Table:

| A8 | 1 | 03582-66528 | PC ASSEMBLY, RAM |
| :---: | :---: | :---: | :---: |
| C1-4, C6-10 | 9 | 0160-4571 | CAPACITOR-FXD . 1 UF . 20 |
| C12-C14 | 3 | 0180-0228 | CAPACITOR-FXD 22 UF 15V |
| R1 | 1 | 0683-1025 | RESISTOR-FXD 1000 5\% |
| R2 | 1 | 0683-5125 | RESISTOR-FXD 5100 5\% |
| U1, U3, U5 | 3 | 1820-1445 | TTL-74LS375 |
| U2, U4, U6 | 3 | 1820-1470 | IC-SN74LS157N |
| U17, U10 | 4 | 1818-1611 | IC MEMORY |
| U11, U14 | 2 | 1820-1794 | TTL-BUF 81LS95N |
| U12, 15-17 | 4 | 1820-1872 | TTL-BUF 81LS96N |
| U13, U19 | 2 | 1820-1199 | IC SN74LS04N |
| U18 | 1 | 1820-1430 | IC SN74LS161AN |
| U20 | 1 | 1820-1491 | IC SN74LS367N |
| U21, U22 | 2 | 1820-1197 | IC SN74LSOON |
| MISC. PARTS |  |  |  |
|  |  | $\begin{aligned} & 4040-0747 \\ & 4040-0748 \end{aligned}$ | EXTR-GREY PC BD EXTR-BLACK PC BD |

CHANGE NUMBER 8 for Serial Numbers 1809A03088 and greater.

Page 8-5-19/8-5-20, Figure 8-5-6. At the top center of the schematic, delete A10C13.

Page 8-5-22, Table 8-5-3. Delete C13.
CHANGE NUMBER 9 for Serial Numbers 1809A03091 and greater.

Page 8-11-9/8-11-10, Figure 8-11-5. In the top right corner of the schematic, add R31 (value 470) between R30 and the horizontal line. Change the values of A14C3, A14C8, A14C13, and A14C15 to 1UF. Change the value of A14R30 to 470. Replace the component locater with the attached Figure 2.

Page 8-11-19, Table 8-11-2. Add R31 0683-4715 RESISTOR FXD $4705 \%$. Change the following components:

| C3, C8, | $0160-4577$ | CAPACITOR-FXD 1UF 50V |
| :--- | :--- | :--- |
| C13, C15 |  |  |
| C6 | $0160-4801$ | CAPACITOR-FXD 100PF |
| C7 | $0160-4832$ | CAPACITOR-FXD .01UF |
| C9, C10, C16 | $0160-4822$ | CAPACITOR-FXD 1000 PF |
| R30 | $0683-4715$ | RESISTOR-FXD 470 5\% |

CHANGE NUMBER 10 for Serial Numbers 1809A03161 and greater.

Page 8-11-11/8-11-12, Figure 8-11-6. Replace the component locator with the attached Figure 3. In the top right corner of the schematic, delete R3 and add R33 ( 470 OHM) and R34 ( 470 OHM) in series with DS3 on the anode side of DS3. Change the A15U4 designators and pins according to the following table:

| OLD REF | NEW REF | INPUT | OUTPUT |
| :---: | :---: | :---: | :---: |
| DESIGNATOR | DESIGNATOR | PIN | PIN |
| U4F | U4B | 3 | 4 |
| U4E | U4C | 5 | 6 |
| U4D | U4E | 11 | 10 |
| U4C | U4F | 13 | 12 |
| U4B | U4D | 9 | 8 |

Page 8-11-20, Table 8-11-2. Delete C16 and R3. Add C15 0160-4571 CAPACITOR-FXD . 1 UF 50V and R33, R34 0683-4715


Figure 2.
RESISTOR 470 5\%. Change the part number and description of the following parts:

$$
\begin{array}{lll}
\mathrm{C} 2, \mathrm{C}, \mathrm{C} 13 & 0160-4571 & \text { CAPACITOR-FXD .1UF 50V } \\
\mathrm{C4}, \mathrm{C} 12, \mathrm{C} 14 & 0160-4822 & \text { CAPACITOR-FXD 1000 PF } \\
\text { C11 } & 0160-4832 & \text { CAPACITOR-FXD .01 UF }
\end{array}
$$



Figure 3.

CHANGE NUMBER 11 for Serial Numbers 1809A03266 and greater.

Page 8-11-26, Table 8-11-2. Delete MP5. Change B1 to 3160-0394 FAN-TUBEAXIEL. Add 03582-24704 SPACER FAN and 3160-0092 FINGER GUARD.

Page 8-12-10, Table 8-12-1. Delete MP5.

CHANGE NUMBER 12 for Serial Numbes 1809A03306 and greater.

Page 8-9-3/8-9-4, Figure 8-9-1. In the right center portion of the schematic, change the value of A4R74 to 13.3 K .

Page 8-3-20, Table 8-3-2. Add R74 0757-0289 RESISTOR-FXD 13.3K 1\%.

CHANGE NUMBER 13 for Serial Numbers 1809A03401 and greater.

Page 8-1-7/8-1-8. Figure 8-1-4. Change the EXTERNAL TRIGGER CIRCUIT as illustrated in Figure 4.

Page 8-1-18, Table 8-1-4. Add the following parts: 0690-1211 RESISTOR 120 10\%
1902-0579 DIODE BKDN 5.11\%
CHANGE NUMBER 14 for Serial Numbers 1809A03421 and greater.

Page 1-3, Table 1-1. Delete option 001.
Page 1-7, Table 1-5. Delete the specifications for TRANSFER FUNCTION ACCURACY (STANDARD). Change TRANSFER FUNCTION ACCURACY (OPTION 001): to TRANSFER FUNCTION ACCURACY:

Page 4-11, Paragraph 4-63. In step d., delete " + + 2 degrees, Option 001), and chañge +-5 degrees to +-2 degrees.

CHANGE NUMBER 15 for Serial Numbers $1809 A 03516$ and greater.

Page 8-11-15/8-11-16, Figure 8-11-8. Change the value of A19R13 to 29.4K.

Page 8-11-25, Table 8-11-2. Change the part number and description of Q1 to 1884-0306 SIL BILATERAL and R3 to 0698-4490 RESISTOR 29.4K $1 \%$.


Figure 4.

CHANGE NUMBER 16 for Serial Numbers 1809A03791 and greater.

Page 8-1-7/8-1-8, Figure 8-1-4. Change A1R12 near the left center of the schematic to *R12 and change the value of A1R11 to 422.

Page 8-1-18, Table 8-1-4. Change the part number and description of R11 to 0698-3447 RESISTOR $4221 \%$. Change R12 to *R12. Add the following components for *R12:

> 0698-3516 RESISTOR $63401 \%$ 0698-3226 RESISTOR $64901 \%$ 0698-3486 RESISTOR $66501 \%$ 0757-3439 RESISTOR $68101 \%$ 0698-4471 RESISTOR $7.15 \mathrm{~K} 1 \%$ 0698-3518 RESISTOR $73201 \%$ 0757-0440 RESISTOR $7.5 \mathrm{~K} 1 \%$ 0698-4472 RESISTOR $67801 \%$

Page 8-7-11, Table 8-7-1. Change the part number of FPR7 to 2100-3686.

CHANGE NUMBER 17 for Serial Numbers $1809 A 03816$ and greater.

Page 8-5-15/8-5-16, Figure 8-5-4. Change the page number to 7-1-1/7-1-2. Change the figure number to $7-1-1$. Add

I(A9) DIGITAL DISPLAY CONTROLLER BACKDATING
REVISION A, B, C, AND D
Schematic
Use backdating schematic $I(A 9)$ for Revision $A, B, C$, and $D$.
Component Locator

Use component locator on backdating Schematic I (A9)
Parts List
Use the current parts list except for the following parts:

| C2 | 0160-3046 | CAPACITOR-FXD 250 PF + - 1\% 100VDC MICA |
| :---: | :---: | :---: |
| C3 | 0160-2199 | CAPACITOR-FXD 30 PF + - 5\% 300VDC MICA |
| C6 | 0140-0193 | CAPACITOR-FXD 82 PF $+-.5 \%$ 300VDC MICA |
| J1 | 1200-0458 | SOCKET-XSTR 3-CONT TO-5 DIP-SLDR |
| $\begin{aligned} & \text { R2, R3, } \\ & \text { R10, R11 } \end{aligned}$ | 0683-5125 | RESISTOR 5.1K 5\% .25W $T C=400 /+700$ |
| - | 6960-0080 | HOLE PLUG |
| DELETE |  |  |
| C14 | 0160-3847 | CAPACITOR-FXD .01UF 50V |
| JR1 | 1258-0141 | JUMPER-REMOVABLE |
| U32-U35 | 1820-1208 | IC DIG SN74LS32N |

Move page to section 7-I. Insert attached page 8-5-15/8-5-16.

Page 8-5-17/8-5-18, Figure 8-5-5. Change the page number to 7-J-3/7-J-4. Change the figure title to "Figure 7-J-1. P/O A9 Digital Display Driver. REV C, D." Add

J(A9) DIGITAL DISPLAY CONTROLLER BACKDATING

REVISION C AND D
Schematic

Use backdating schematic J(A9) for Revision C and D.
Component Locator
Use component locator on backdating Schematic J(A9)
Revision C and D.
Parts List
Use the current parts list for J(A9).
Move page to section 7-J. Insert attached page 8-5-17/8-5-18.
Page 8-5-21, Table 8-5-3. Change the following components:

| C2 | $0160-4811$ | CAPACITOR-FXD 270 PF |
| :--- | :--- | :--- |
| C3 | $0160-4807$ | CAPACITOR-FXD 33 PF 110V |
| C6 | $0160-4802$ | CAPACITOR-FXD 82 PF .5 100V |
| J1 | $1251-5501$ | CONNECTOR |
| R2, R3 | $0698-3155$ | RESISTOR-FXD $46401 \% .125 \mathrm{~W}$ |
| R10, R11 |  |  |
| ADD |  |  |
| C14 | $0160-3847$ | CAPACITOR-FXD .01UF 50V |
| JR1 | $1258-0141$ | JUMPER-REMOVABLE <br> U32-U35 <br> $1820-1208$ |
| IC DIG SN74LS32N |  |  |

Page 8-11-19, Table 8-11-2. Change the part number and description of L1 to $9140-0649$ INDUCTOR-FXD.

Page 8-11-20, Table 8-11-2. Change the part number and description of L1 to $9140-0649$ INDUCTOR-FXD.

CHANGE NUMBER 19 for Serlal Numbers 1809A03936 and greater.

Page 8-11-13/8-11-14, Figure 8-11-7. Replace the component locator in the upper right corner with the attached Figure 5.

Page 8-11-22, Table 8-11-2. Change the fuse holder part number and description to FH1 2110-0643 FUHLR-CL 15A. Change the following component part numbers and descriptions:

| C2, C10, | 0160-4835 | CAPACITOR-FXD .1UF 50V |
| :--- | :--- | :--- |
| C11 |  |  |
| C9 | $0160-3847$ | CAPACITOR-FXD .01 UF |
| C12, C14 | $0160-4822$ | CAPACITOR-FXD 1000 PF |


[^0]:    *Actually on the 10 kHz span, the sample rate is dropped to 81.92 kHz to take advantage of the digital filter structure.

[^1]:    * HP-IB is Hewlett-Packard's implementation of IEEE Std. 488-

    1975, "Standard Digital Interface for Programmable Instrumentation."

