Tektronix®
COMMITTED TO EXCELLENCE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

7912AD PROGRAMMABLE DIGITIZER SERVICE VOL. 1

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

070-2407-00
Product Group 45

Serial Number _____

First Printing APR 1979
Revised APR 1984

Scans
By
Artek Media

Artek Media
1042 Plummer Cir. SW
Rochester, MN 55902

www.artekmedia.com

"High resolution scans of obsolete technical manuals"

If your looking for a quality scanned technical manual in PDF format please visit our WEB site at www.artekmedia.com or drop us an email at manuals@artekmedia.com and we will be happy to email you a current list of the manuals we have available.

If you don't see the manual you need on the list drop us a line anyway we may still be able to point you to other sources. If you have an existing manual you would like scanned please write for details, This can often be done very reasonably in consideration for adding your manual to our library.

Typically the scans in our manuals are done as follows;

1) Typed text pages are typically scanned in black and white at 300 dpi.
2) Photo pages are typically scanned in gray scale mode at 600 dpi
3) Schematic diagram pages are typically scanned in black and white at 600 dpi unless the original manual had colored high lighting (as is the case for some 70's vintage Tektronix manuals).

If you purchased this manual from us (typically through our Ebay name of ArtekMedia) thank you very much. If you received this from a well-meaning "friend" for free we would appreciate your treating this much like you would "share ware". By that we mean a donation of at least $5-10 per manual is appreciated in recognition of the time (a manual can take as much as 40 hours to reproduce, book, link etc.), energy and quality of effort that went into preserving this manual. Donations via PayPal go to: manuals@artekmedia.com or can be mailed to us the address above.

Thanks

Dave & Lynn Henderson
Artek Media

Products of Tektronix, Inc. and its subsidiaries are covered by U.S. and foreign patents and/or pending patents.

TEKTRONIX, TEK, SCOPE-MOBILE, and  are registered trademarks of Tektronix, Inc. TELEQUIPMENT is a registered trademark of Tektronix U.K. Limited.

INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektronix, Japan
700000	Tektronix Holland, NV, Heerenveen, The Netherlands

TABLE OF CONTENTS

VOL. I

@

VOL. II

SAFETY SUMMARY

This manual contains safety information which the user must follow to ensure safe operation of the instrument. The following safety information and precautions must be observed during all phases of operation and maintenance.

Terms and Symbols

WARNING statements identify conditions or practices that could result in damage to the equipment or property.

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

DANGER, as it appears on equipment, identifies areas of immediate hazard that could result in personal injury or loss of life.

 DANGER - High Voltage

 Protective ground (earth) terminal.

Power Source

The 7912AD is entended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective-ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Ground the Instrument

The 7912AD is grounded through the grounding conductor of the power cord. To avoid electric shock, plug the power cord into a properly wired receptacle before connecting to 7912AD inputs or outputs.

Use the Proper Power Cord

Use only the power cord and connector specified in the parts list. Use only a power cord that is in good condition.

Use the Proper Fuse

To avoid fire hazard, use only the fuse that is specified in the parts list for your instrument and that is identical in type, voltage rating, and current rating.

Do Not Operate in an Explosive Atmosphere

To avoid explosion, do not operate this instrument in an atmosphere of explosive gases unless it has been specifically certified for such operation.

Do Not Service Alone

Do not perform internal service or adjustment of this instrument unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

Dangerous voltages exist at several points in this instrument. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

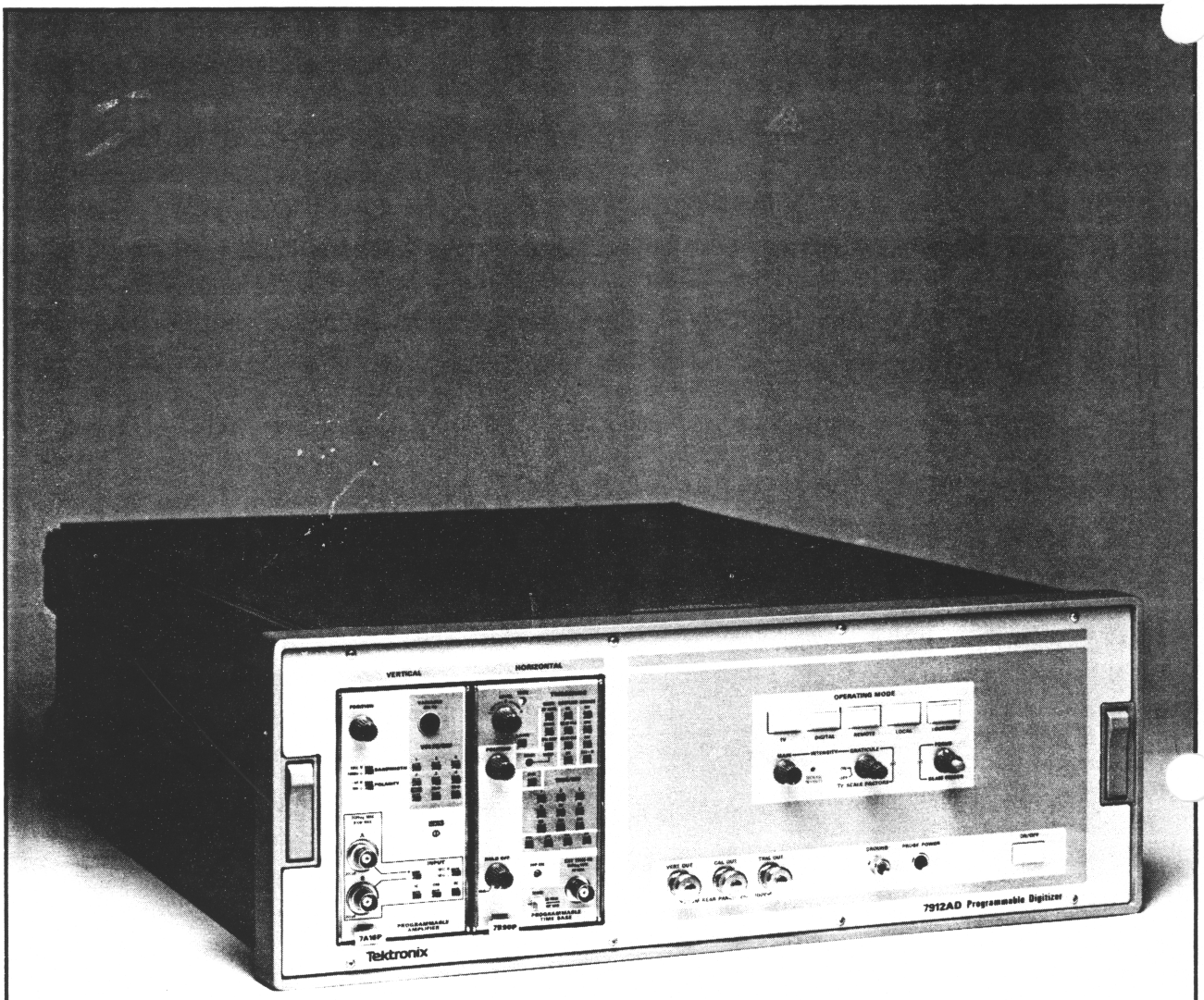
PREFACE

This service manual is provided to assist in the service and repair of the 7912AD Programmable Digitizer. It is intended for qualified service personnel only.

Volume I contains an introduction to the 7912AD and operating and programming information to help the service person understand and operate the instrument. A block diagram and detailed circuit description follow.

Volume II contains maintenance information and a calibration procedure. At the rear are electrical and mechanical parts lists and electrical and mechanical diagrams.

For more operating and programming information, see the 7912AD Operators Manual. For a full discussion of the IEEE 488 bus to which this instrument can be interfaced, see IEEE Standard 488-1975, the IEEE Standard Digital Interface for Programmable Instrumentation.



The 7912AD Programmable Digitizer with programmable plug-ins.

SECTION 1

INTRODUCTION

The TEKTRONIX 7912AD Programmable Digitizer is a wide-bandwidth waveform acquisition instrument with both analog and digital outputs. Programming is accomplished over the bus specified in IEEE Standard 488-1975.

Two operating modes are provided. In the digital mode, the 7912AD digitizes either a single-shot or repetitive waveform and stores it for internal processing or for output on the IEEE 488 bus. Analog outputs are also provided to display the waveform data on an X-Y-Z monitor. In the TV mode, the 7912AD converts a waveform to a composite video output. This allows the input waveform to be displayed on a TV monitor such as the TEKTRONIX 634 Monitor, one of the 650- and 670-series of color Picture Monitors.

In either the TV or digital mode, the 7912AD can acquire waveforms with high bandwidths: up to 500 MHz with the TEKTRONIX 7A19 Amplifier plug-in, for instance, or 1 GHz with the TEKTRONIX 7A21N Direct Access plug-in. The time window can be selected between 10 milliseconds and 5 nanoseconds using a TEKTRONIX 7000-series time base plug-in. This is equivalent to sampling rates (in digital mode) from 50 kHz to 100 GHz.

Remote control and data output via the IEEE 488 bus is simplified by two microprocessor systems in the 7912AD. The firmware operating systems for these microprocessors is designed to let the programmer talk to the 7912AD in as simple and obvious a manner as possible.

Design of the firmware that controls the IEEE 488 interface is consistent with the IEEE 488-1975 standard. Extended addresses are used so that the 7912AD can act as a transparent interface for programmable plug-ins (if installed). These plug-ins include the 7A16P Programmable Amplifier and the 7B90P Programmable Time Base.

The 7912AD operates in many respects like an oscilloscope such as those in the TEKTRONIX 7000-series. The input signal is connected to a vertical plug-in to drive the vertical deflection amplifer. A number of 7000-series plug-ins are available to tailor the 7912AD for bandwidth, input impedance, differential or single-ended input, and input voltage. On most vertical plug-ins, a wide range of deflection factors

(amplification) can be selected on the front panel. A number of 7000-series time base plug-ins are available to drive the horizontal deflection amplifier at calibrated sweep rates.

Although the vertical and horizontal deflection systems of the 7912AD are similar to those of an oscilloscope, the similarity ends there. In place of the oscilloscope CRT, there is a scan converter tube. Instead of displaying the input waveform as a trace on the phosphor-coated face of a CRT, the input waveform is written on a silicon diode matrix and read from this target as in a vidicon TV camera.

The Scan Converter

Because of the high writing rate of the scan converter, the 7912AD performs at high bandwidths and sampling rates not usually obtained with other digitizing techniques. The high writing rate stems from several factors that can be understood only by considering the design of the scan converter. The scan converter is an electron tube with dual electron guns, one at each end of the tube. Between the two guns is the target (Fig. 1-1).

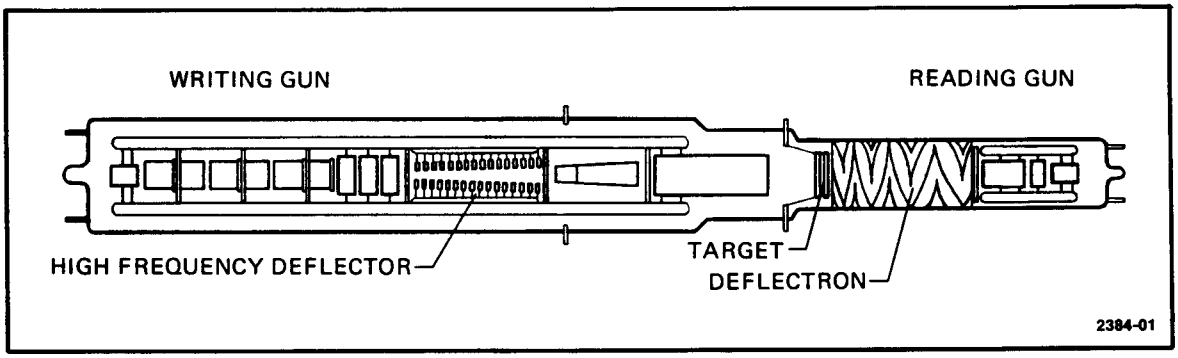


Fig. 1-1. The 7912AD scan converter tube.

The target is an array of diodes formed on an n-type silicon wafer by integrated circuit techniques (Fig. 1-2). In operation, the target substrate is held positive with respect to the reading gun cathode by the target lead. The target is scanned continuously by the reading beam, charging each diode toward the more negative cathode potential to reverse-bias it.

When the time base is triggered, it unblanks the writing gun and applies a ramp to the horizontal deflection plates of the writing gun to write a trace across the target. At the same time, the input signal is

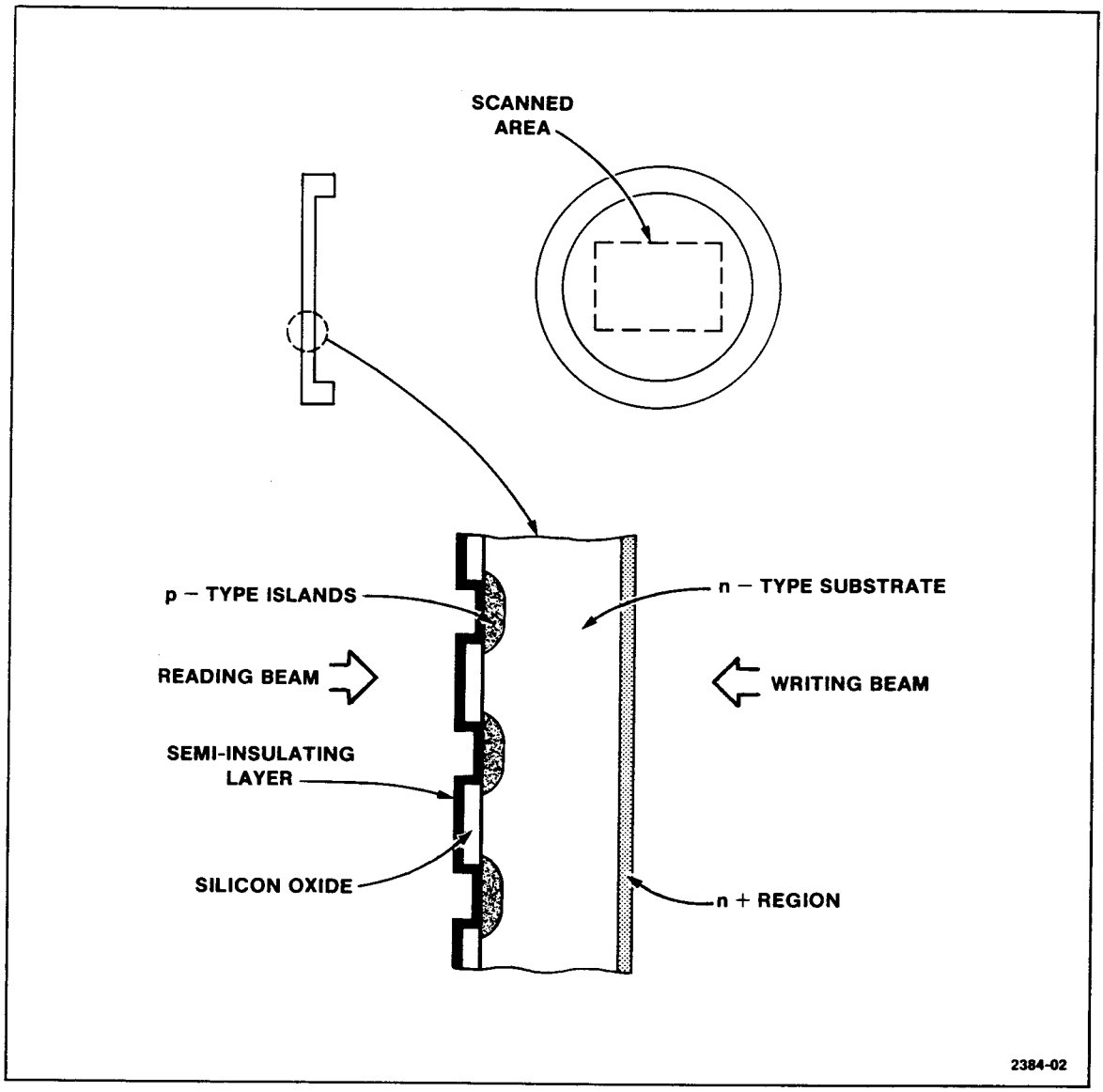


Fig. 1-2. The 7912AD scan converter target. The area scanned is approximately 1.3 X 0.95 centimeters with a diode density of about 800 per centimeter.

applied to the vertical deflection plates to vary the height of the trace according to the amplitude of the input signal.

The writing gun electrons, accelerated by the 10-kilovolt potential between the gun and target, bombard the target (Fig. 1-3). Each electron creates many electron-hole pairs near the surface. The holes diffuse through the target and drift across the depletion region at the p-n junction, causing the adjacent diodes to conduct and discharge. When the reading beam next scans the target, little or no current flows at points that were not written. Where the target was written, however, the diodes are recharged and a signal current can be detected in the target lead. This output signal is amplified for further processing.

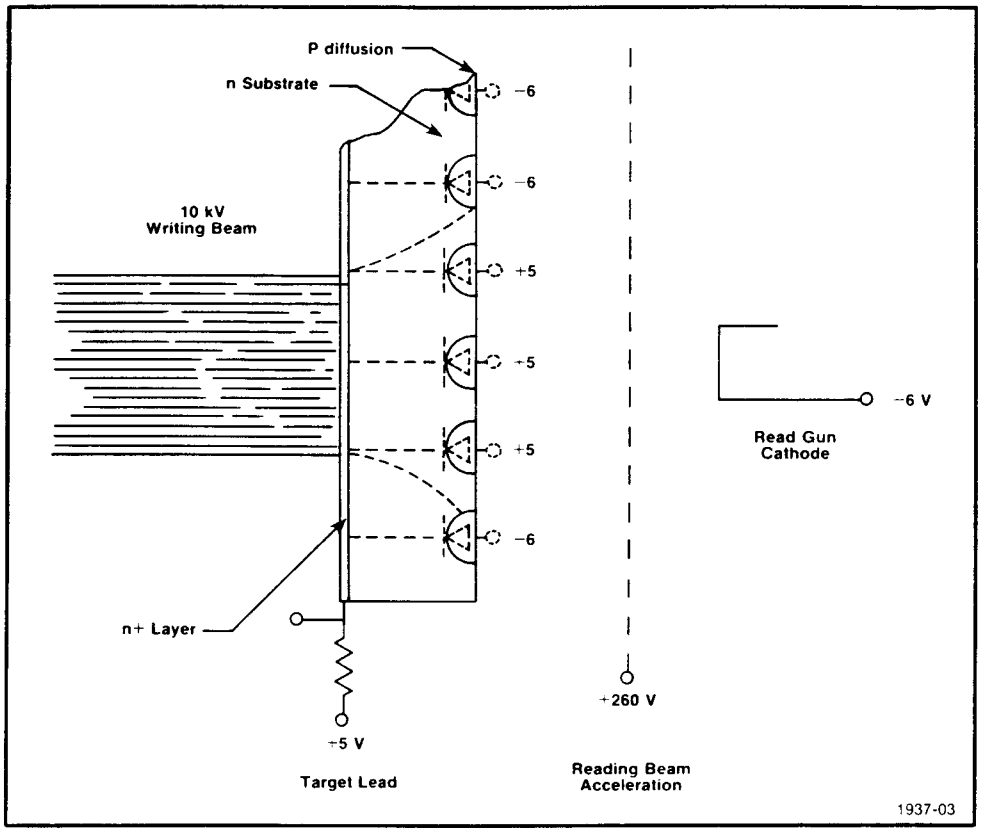


Fig. 1-3. The scan converter tube in operation showing the effect of the reading beam.

Since the energy required to create an electron-hole pair in silicon is about 3.6 electron volts, roughly 2,780 electron-hole pairs are created by each 10-kV electron that strikes the target. Accounting for certain losses, the effective charge gain in the target is about 2,000. This gain is responsible for the high-speed performance of the scan converter because few electrons need to strike the target to record a waveform, allowing the writing trace to be deflected at high speeds.

Other advantages stem from writing and reading the waveform on the target. Because the target is small, the writing beam need only be deflected over a small area (about 1.3 X 0.95 centimeters). Only the writing beam need be high-velocity; the reading beam can be scanned more slowly.

TV Mode

In TV mode, the target is scanned horizontally by the reading beam in a conventional television format with a 525-line (625-lines with option 13) raster. This scan mode is shown in Fig. 1-4. The output signal is amplified, a sync waveform is added, and the composite video signal is provided to two output connectors on the 7912AD rear panel.

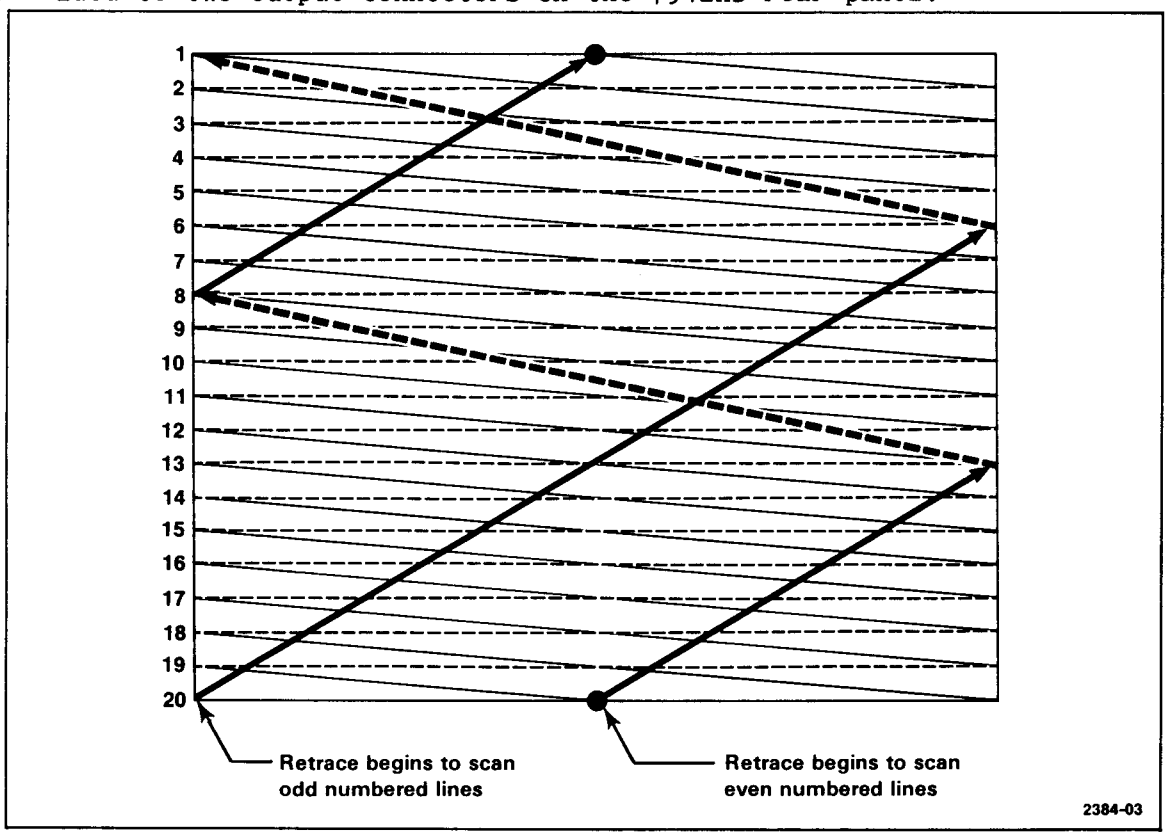


Fig. 1-4. A small-scale example of an interlaced horizontal scan such as is used in the 7912AD TV mode.

One output, LINEAR, is a replica of the output of the target lead. The signal goes positive (white) whenever the reading beam crosses a portion of the target that is written; its amplitude varies with the intensity with which that portion of the target was written.

The other output, BINARY, is a two-level output derived from the LINEAR signal. A comparator sets the video level high when it detects that the writing beam crosses a portion of the target that is written. The comparator sets the video level low at all other times during the scan.

To provide the waveform scale factors as part of the monitor display, a character generator adds the readout from the plug-ins to the composite video outputs.

The TV mode provides several advantages over a conventional oscilloscope display. The monitor can be larger and it can be located some distance from the 7912AD. The TV monitor can be used to set up the 7912AD and plug-in controls for data acquisition. The effect of the intensity controls can be observed, for instance. If the BINARY output is used, the output of the comparators can be displayed to assure that all parts of the waveform will be digitized in the digital mode at a particular intensity setting.

Digital Mode

In the digital mode, the target is scanned vertically by the reading beam in a 512 X 512 point format (Fig. 1-5). The signal from the target lead is amplified and fed to a comparator. If the signal is above the comparator threshold, the comparator switches to a high state to indicate that the reading beam is crossing a portion of the target that is written. If the signal is below the threshold, the comparator switches low to indicate that no trace is detected.

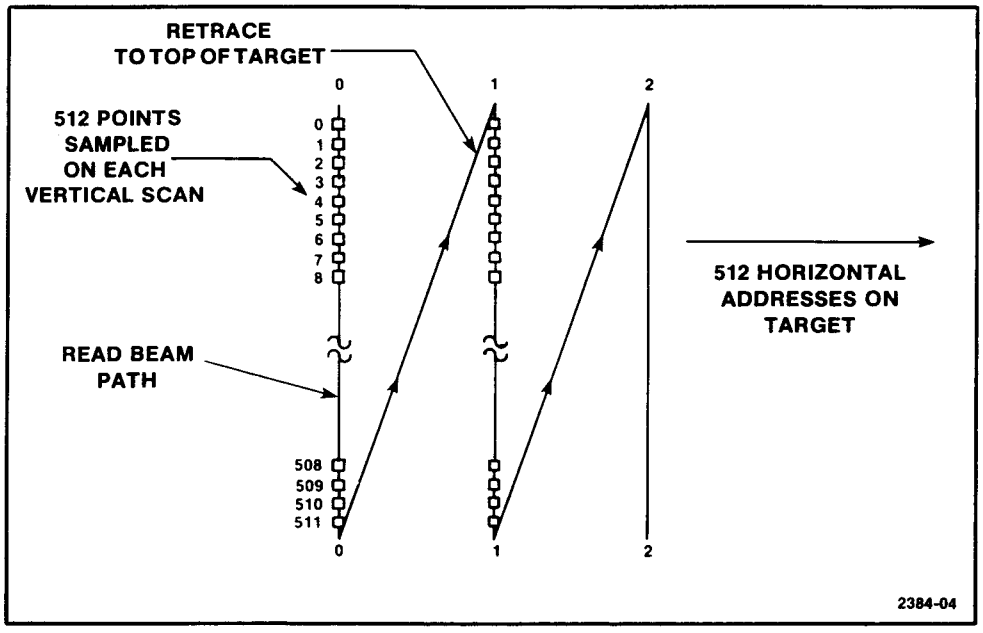


Fig. 1-5. In digital mode, the target is scanned along 512 vertical lines from left to right.

The 7912AD begins to store data on the next time base trigger after either the DIGITAL button is pressed (local mode) or a digitize command is received (remote mode). Two counters are the source of the data. One counter is incremented from 0 to 511 as the reading sweeps down the target. Each time the counter is incremented, the output of the

comparator is sampled. If the comparator has changed state since the last sample, the count is complemented and stored in memory in the Y (vertical) array.

As a result, two data values are usually stored during each vertical scan, one for the top of the trace and one for the bottom of the trace. Data are always stored in pairs. If the top of a written portion of the target is detected, the bottom will be detected as well. Up to 30 data can be stored to handle graticule and dual traces. The data are complemented so 511 corresponds to the top of the target and zero to the bottom.

Meanwhile, another counter is incremented each time the reading beam begins another vertical scan. The value of the counter is used to address a location in an X (horizontal) array where the number of data points detected by that vertical scan is stored. When read, the X and Y arrays are used by 7912AD microprocessor routines or external data processing to recover the X and Y coordinates of all points detected as data on the target.

Options

The following options are available for the 7912AD. They are not field-installable; instructions are not provided in the 7912AD manuals to modify the 7912AD for these options. Changes to the replaceable parts lists are detailed in the service manual for the 7912AD.

Option 4. Change to fast digitize mode. The scan time to read a waveform from the target and into local memory is reduced by compressing the scan. The target is written on and read from a 256 X 256 point matrix with a maximum of 14 points stored per vertical scan. However, the data are normalized to a 512 by 512 point matrix before further processing or output. Vertical values are multiplied by two and the data are blown up to 512 points horizontally by treating every other point as if it is empty.

Graticule resolution is cut by one-half; every other major division is marked in digital mode, and every other major and minor division is marked in TV mode. Both the TV and XYZ displays are restored to the same size as the non-option 4 displays.

This option changes the minimum sweep rate to 200 microseconds/division. This is the lower limit on sweep rate for digitizing reliable data in fast-digitize mode.

Option 9. Set instrument for 230 VAC operation; substitute a 230 volt power cord.

Option 13. Change TV scan rate. The TV mode reading scan of the target is changed to 625 lines per frame with a 50 hertz field rate. The composite video outputs, sync input, and sync output are changed to match this scan rate.

Option 30. Delete cable. The IEEE 488 bus cable that is a standard accessory is deleted.

Specifications

Electrical characteristics of the 7912AD are listed in Table 1-1, Table 1-2, and Table 1-3. To be valid, the following conditions apply:

1) The 7912AD and plug-ins must be calibrated at an ambient temperature between +20 and +30 degrees C.

2) The 7912AD and plug-ins must be allowed to warm up for at least 20 minutes with all covers installed.

3) The calibration of the 7912AD must be checked according to the calibration procedure within each 1000 hours of operation or every six months if operated infrequently. Any adjustments that cause performance outside the limits allowed by the calibration procedure must be readjusted. The plug-ins must also be operated within their calibration intervals.

4) The 7912AD and plug-ins must be operated within their specified environmental limits (Table 1-4). In some cases, an electrical characteristic applies only to a limited temperature range or must be derated to apply to the entire temperature range. These cases are noted.

Statements in the Performance Requirements column are verified by the steps marked with a in the calibration procedure, Section 5 (Vol. II). Statements listed in the Supplemental Information column are not verified in the calibration procedure and are not to be construed as performance requirements of the 7912AD.

Physical characteristics are listed in Table 1-5.

TABLE 1-1

ELECTRICAL SPECIFICATIONS

Characteristics	Performance Requirements	Supplemental Information
VERTICAL DEFLECTION SYSTEM		
Deflection factor	Compatible with all 7000-Series amplifier plug-in units.	Full-scale deflection is ±4 divisions.
Relative accuracy	See Table 1-2.	
Centering	Zero-volt input can be centered by plug-in position control.	Within 0.5 division of electronic graticule center with no plug-in (1 division, option 4).
Low-frequency linearity	0.1 division or less compression or expansion of a centered, two-division waveform. This limit is not exceeded if the waveform is positioned anywhere within the electronic graticule area.	
Bandwidth	See Table 1-2.	
Rise time	See Table 1-2.	
Isolation, signal to graticule	At least 100:1 up to 250 MHz; at least 40:1 from 250 MHz to 500 MHz.	

TABLE 1-1 (cont.)

Characteristics	Performance Requirements	Supplemental Information
Delay line	Adds approximately 60-nanosecond delay in vertical signal path to permit viewing or digitizing of leading edge of triggering waveform.	
GRATICULE		
Format	8 vertical divisions X 10 horizontal divisions.	
TV mode	Both major and minor divisions marked, five minor divisions per major division.	
Digital mode	Only major divisions marked.	
TV mode, option 4	Only every other major and minor division marked.	
Digital mode, option 4	Only every other major division marked.	
Writing time		Requires 3 milliseconds, gated immediately after waveform is acquired. Locks out vertical signal and main sweep and disables Z-axis.

TABLE 1-1 (cont.)

Characteristics	Performance Requirements	Supplemental Information
Position		Adjustable horizontally and vertically ±5%.
Amplitude		Adjustable horizontally and vertically ±5%.
Intensity	Controlled from front panel or by programmed command separately from main intensity.	
Stability		
0 to +40 degrees C		0.5%.
+20 to +30 deg. C		0.1%.

HORIZONTAL DEFLECTION SYSTEM

Deflection factor	Compatible with all 7000-Series plug-in units. See Table 1-3 for recommended time base plug-ins.	Full scale deflection is ±5 divisions.
DC linearity	0.05 division or less error at each graticule line after adjusting for no error at the second and tenth graticule lines (0.1 division, option 4).	

TABLE 1-1 (cont.)

Characteristics	Performance Requirements	Supplemental Information
Fastest calibrated sweep rate (with 7B90P, 7B92A, or 7B80GB Time Base)	0.5 nanosecond/division.	
Slowest sweep rate	1 millisecond/division (200 microseconds/division, option 4).	
Centering	Center of sweep can be centered in graticule by time base Position control.	
Bandwidth, 10 division reference	DC to at least 1 megahertz.	
EXTERNAL Z-AXIS INPUT		
Polarity	Positive-going signal decreases trace intensity of writing gun; negative-going signal increases trace intensity. Zero-volt (approximate) input produces no intensity change.	
Sensitivity	Two volts peak-to-peak provides trace modulation over full intensity range.	
Low-frequency limit		DC

TABLE 1-1 (cont.)

Characteristics	Performance Requirements	Supplemental Information
DC input resistance		550 ohms, ±10%.
Maximum Input voltage		15 volts (DC + peak AC).

CRT TARGET AND WRITING GUN

Gun type	Monoaccelerator.	
Light defects		
Distribution	No more than six points digitized or displayed other than those written by input waveform. No two light defects on same vertical line.	
Size	No light defects larger than six TV lines.	
Geometry	A straight-line input is read from the target as a straight line within 0.1 division.	

TABLE 1-1 (cont.)

Characteristics	Performance Requirements	Supplemental Information
Writing Rate (+10 to +40 degrees C)		
TV mode	Writes an 8-division sine wave of at least 500 MHz in a single sweep.	At least 12.5 divisions per nanosecond; 30 divisions per nanosecond, typical.
Digital mode	Writes a single 8-division pulse with a rise time of 1 nanosecond or less (2 nanoseconds or less from 0 to +10 degrees C).	At least 8 divisions per nanosecond, typical.
Option 4		
TV mode	Writes an 8-division sine wave of at least 1 GHz in a single sweep.	At least 25 divisions per nanosecond; 60 divisions per nanosecond, typical.
Digital mode	Writes a single 10-division pulse with a risetime of 0.5 nanosecond or less (1 nanosecond or less from 0 to +10 degrees C.)	At least 20 divisions per nanosecond, typical.

TABLE 1-1 (cont.)

Characteristics	Performance Requirements	Supplemental Information
READING GUN		
Type	Monoaccelerator	
RAMP GENERATOR AND SCAN AMPLIFIER		
Scan time, digital mode		Approximately 16.4 milliseconds per waveform to read waveform and store in memory (approximately 4.5 milliseconds, option 4).
VIDEO SYSTEM		
Resolution TV mode		At least 400 TV lines per picture width. Video signal is down less than 50% at linear output.
Ultimate resolution, TV mode		At least 500 TV lines when viewed on a TEKTRONIX 632 Monitor or equivalent.

TABLE 1-1 (cont.)

Characteristics	Performance Requirements	Supplemental Information
Digital mode		
Horizontal	Two signals, each including a step with a risetime of 10 nanoseconds, are digitized separately at a sweep speed of 50 nanoseconds/division if the steps are delayed 1.25 nanoseconds with respect to each other.	400 lines.
Vertical	A 50 milivolt square wave is resolved at 2 volts/division.	320 lines.
VIDEO OUTPUTS		
Composite video		
Linear	1 volt into 75 ohms for full white signal. Conforms to EIA RS-170.	
Binary		
Low level	0 to +0.3 volts into 75 ohms.	
High level	+1 volt ±0.1 volt into 75 ohms.	
Sync out	At least +4 volts into 75 ohms. Conforms to EIA RS-170.	

TABLE 1-1 (cont.)

Characteristics	Performance Requirements	Supplemental Information
Scan rate		
Standard		525 lines/frame, 60 Hz field rate (interlaced).
Option 13		625 lines/frame, 50 Hz field rate (interlaced).
Scale factor readout	Up to eight characters per channel.	
VERTICAL plug-in	Channel 1 appears in upper left corner of graticule, channel 2 in lower left corner of graticule.	
HORIZONTAL plug-in	Channel 1 appears in upper right corner of graticule, channel 2 in lower right corner.	
Return losses, sync loop		At least 40 dB to 4 megahertz.
IEEE 488 Interface		
Data connector	Conforms to IEEE Standard 488-1975.	
Signal levels		Conform to IEEE Standard 488-1975.
Signal timing		Conforms to IEEE Standard 488-1975.

TABLE 1-1 (cont.)

Characteristics	Performance Requirements	Supplemental Information
Data transfer rate, max.		710 kilobytes/second.
Waveform transfer time, min.		9 milliseconds for 1024 vertical and 512 pointer data.
Waveform acquisition and transfer rate, max.		40 waveforms/second.
Typical		6-20 waveforms/second, depending on characteristics of input signal.
X-Y-Z analog display outputs of waveform data		
X and Y	1 volt peak-to-peak into 100 kilohms or greater; adjustable from 0.75 to 1.3 volts.	8-bit resolution.
Z	Zero volts (blanked), 1 volt (unblanked) into 100 kilohms or greater. Blanked between data points.	
Z_{out}, X and Y		50 ohms, +5%.

FEEDTHROUGH CONNECTORS

VERT IN, CAL IN, TRIG IN (rear-panel connectors)	Connect to front panel connectors through coaxial cable.	

TABLE 1-1 (cont.)

Characteristics	Performance Requirements	Supplemental Information
Z_0		50 ohms, ±2%.
Attenuation of VERT IN/OUT and CAL IN/OUT signal paths		0.33 dB at 400 MHz; 0.54 dB at 1 GHz.
POWER SUPPLY		
Remote control		
ACUTATE	TTL low level (<0.8V) applied between center conductor and outer conductor turns on power supply. A return to a TTL high level (>2V) turns off power supply. Outer conductor is isolated from chassis by approximately 100 ohms.	
ENABLE	Provides TTL low level (<0.4V) between center conductor and outer conductor approximately 150 milliseconds after power-up. Maximum sink current is 16 milliamps. Goes to TTL high level after power supply is turned off.	

TABLE 1-1 (cont.)

Characteristics	Performance Requirements	Supplemental Information
POWER INPUT		
Line voltage		
115, nominal		90 to 132 volts AC.
230, nominal		180 to 250 volts AC.
Line frequency		48 to 440 Hz.
Power consumption		
Typical, not including plug-ins		250 watts
Maximum, including plug-ins		360 watts
Line current, max		5.2 amps (90 VAC)
SAFETY		
Power line fuse	6 amps, 250 volt, fast-blow.	

TABLE 1-2

7912AD SYSTEM ELECTRICAL CHARACTERISTICS

Plug-in Amplifier	Performance Feature	Minimum Deflection Factor	Bandwidth	Rise Time (Calculated)	Relative Accuracy*
7A11	Low-capacitance FET probe built-in	5 mV/div	250 MHz (225 MHz, +30 to +40 degrees C)	1.4 ns (1.6 ns, +30 to +40 degrees C)	2%
7A13	Differential input; DC offset	1 mV/div	105 MHz	3.4 ns	1.5%
7A16A	1-megohm input	5 mV/div	225 MHz	1.6 ns	2%
7A16P	Programmable	10 mV/div	200 MHz	1.8 ns	2%
7A18	Dual-channel, 1-megohm input	5 mV/div	75 MHz	4.7 ns	2%
7A19	Wide bandwidth, 50-ohm input	10 mV/div	500 MHz (400 MHz, +30 to +40 degrees C)	0.8 ns (0.9 ns +30 to +40 degrees C)	3%
7A24	Dual-channel, wide bandwidth, 50-ohm input	5 mV/div	350 MHz (300 MHz, +30 to +40 degrees C)	1.0 ns (1.2 ns, +30 to +40 degrees C)	2%
7A21N	Direct access, 50-ohm input	Less than 4 V/div	1 GHz	0.35 ns	--
7A26	Dual-channel 1-megohm input	5 mV/div	200 MHz (160 MHz, +30 to +40 degrees C)	1.8 ns (2.2 ns, +30 to +40 degrees C)	2%

*Applies to all deflection factors when the plug-in gain is set at the

deflection factor designated on each plug-in. The calibration signal must be supplied by an external calibrator whose accuracy is within 0.25%.

TABLE 1-3

RECOMMENDED TIME BASE PLUG-IN

Plug-in	Maximum Sweep Rate	Triggering Frequency Range	Notes
7B80	1 ns/div	400 MHz	
7B80 MOD GB	500 ps/div	400 MHz	Slowest sweep rate is 10 us/div
7B90P	500 ps/div	400 MHz	Programmable
7B92A	500 ps/div	500 MHz	Both normal and delayed sweep; set intensity carefully in alternate mode

TABLE 1-4

ENVIRONMENTAL CHARACTERISTICS

Characteristics	Description
Temperature	
Operating	0 to +40 degrees C.
Nonoperating	-55 to +75 degrees C.
Altitude	
Operating	Up to 4570 meters (15,000 feet).
Nonoperating	Up to 15,200 meters (50,000 feet).
Electromagnetic compatibility (EMC) with plug-ins or EMC-shielded blank plug-ins installed	Meets all applicable parts of MIL-STD-461A when tests are performed according to MIL-STD-462 for radiated and conducted electromagnetic emissions and susceptibility from 30 hertz to 1 gigahertz.

TABLE 1-5

PHYSICAL CHARACTERISTICS

Characteristics	Description
Size	Can be mounted in standard 19-inch rack. See Fig. 1-6.
Weight (no plug-ins)	Approximately 24.7 kilograms (54.6 pounds).
Air intake at fan	2.83 meters^3/min. (100 feet^3/min), max; typically 2.40 meters^3/min. (85 feet^3/min).

Accessories

The following accessories are supplied with the 7912AD; for part numbers, see the Accessories page in the back of Vol. II.

1 power cord, 2.4 meters (8 feet)

1 set of rack slides with hardware

1 IEEE 488 bus cable, 2 meters (6.6 feet)

1 operators manual

1 service manual (two volumes)

Checkout software with manual

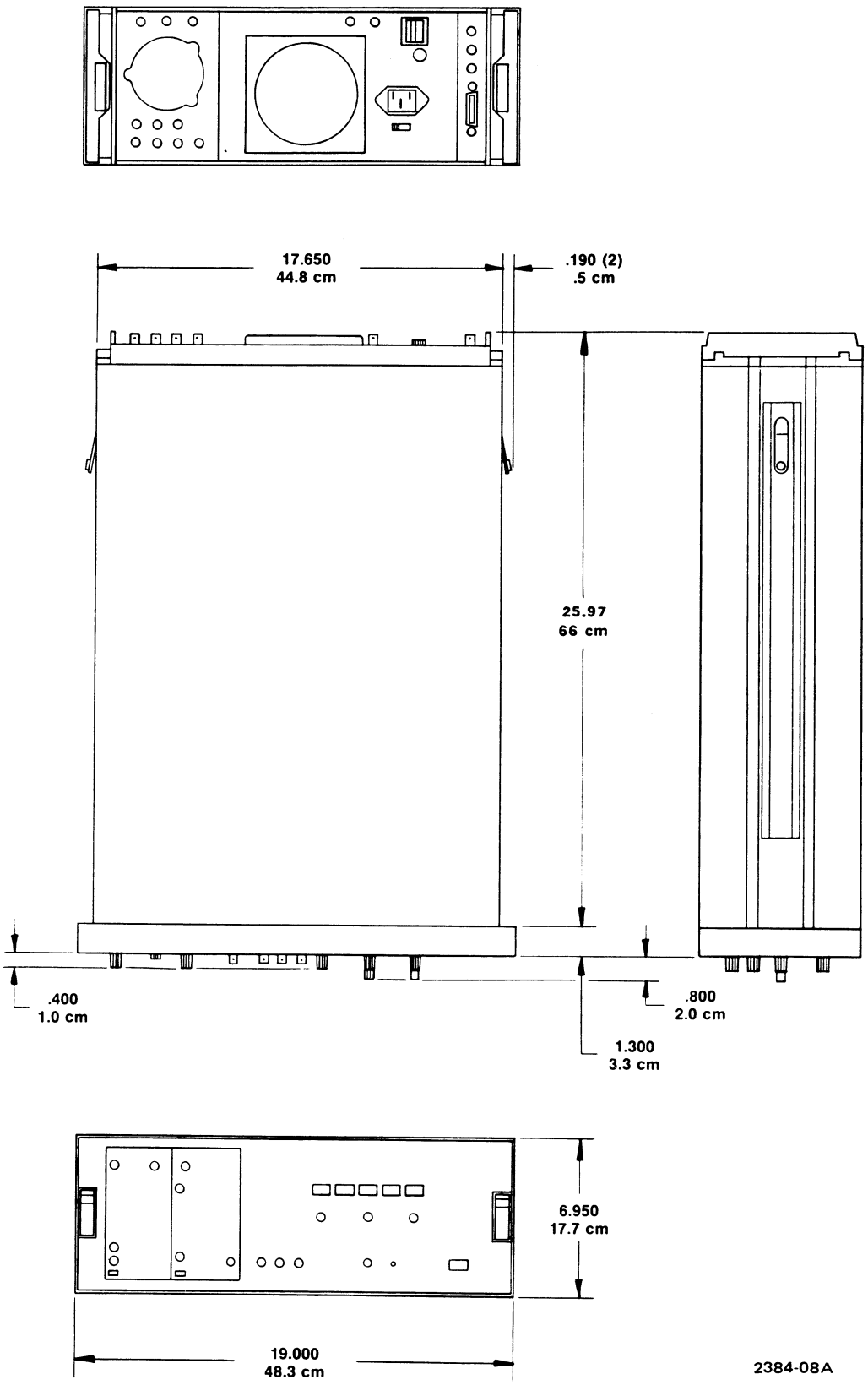


FIG. 1-6. 7912AD outside dimensions shown in both inches and centimeters.

SECTION 2

OPERATION

This section contains a description of 7912AD controls and connectors and instructions for local (operator) control of the instrument. For more complete operating and programming instructions, refer to the 7912AD Operator's manual.

The 7912AD is based on the TEKTRONIX 7000-series plug-in concept. Signal-conditioning plug-ins are used. These have their own operating controls; see the plug-in operators manuals for a description of the controls and instructions for operating the plug-ins. Although some of the plug-in controls are referenced in this manual, they are not fully described, nor are full instructions for their use provided.

Controls and Connectors

Front Panel

The front panel controls and connectors are shown in Fig. 2-1. The numbers in the following descriptions refer to Fig. 2-1.

OPERATING MODE

(1) TV: Sets the 7912AD to TV mode. Lights when in TV mode. If, when the TV button is pressed, the 7912AD is performing a digitize operation, it waits until completed before switching to TV mode.

(2) DIGITAL: Sets the 7912AD to digital mode and initiates a digitize operation. Lights when in digital mode. There is a two-second delay for set-up when switching from TV to digital mode. Once DIGITAL is pressed, the 7912AD is readied to digitize but waits for a sweep gate from the time base to store data detected on the target. To be detected, the input waveform and/or graticule must have been written on the target with sufficient intensity (set by the INTENSITY controls).

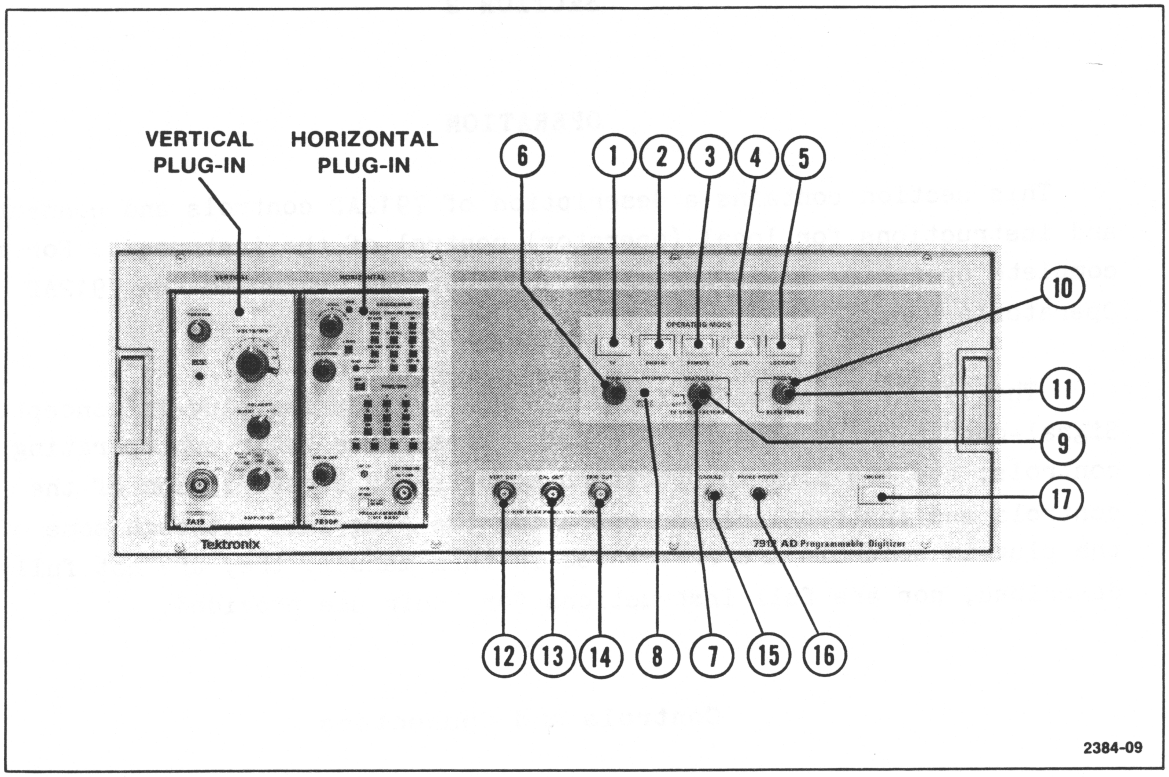


Fig. 2-1. Front panel controls and connectors. The numbers refer to descriptions in the text of the controls and connectors.

(3) REMOTE: Lights to indicate when the 7912AD is set to remote mode by the IEEE 488 bus system controller. When REMOTE is pressed, the 7912AD requests service from the IEEE 488 bus controller if the interrupt is enabled.

(4) LOCAL: Returns the 7912AD from remote mode to local control if not in remote with lockout state (see LOCKOUT). Lights when in local mode. If the instrument is executing a remote command or performing a digitize operation, it waits until finished to return to local.

(5) LOCKOUT: Lights to indicate the 7912AD is set to either local with lockout state or remote with lockout state by the IEEE 488 bus system controller. In remote with lockout state (both REMOTE and LOCKOUT are lighted), the LOCAL button does not return the instrument from remote to local control.

INTENSITY

(6) MAIN: Sets writing beam intensity to control input waveform definition on the converter tube target.

(7) GRATICULE: Sets writing beam intensity when the graticule is written on the converter tube target (outer knob). When set to minimum, the graticule is not written, so it is not displayed (TV mode) or digitized (digital mode).

DECREASE INTENSITY

(8) Lights to warn that the 6800 MPU is automatically limiting beam current because either or both intensity controls are set too high. Also lights when the MPU turns off the writing beam because it detects an invalid sweep rate. Blinks when a hardware protection circuit becomes active; in this condition, the beam is automatically deflected outside the graticule area.

(9) TV SCALE FACTORS

Turns on or off the display of scale factors when in TV mode (inner knob).

(10) FOCUS

Sets focus of writing beam to affect trace definition (outer knob).

(11) BEAM FINDER

Compresses the input waveform into the graticule area, even if the waveform is overdriving the 7912AD input (inner button). Used to determine how the plug-in controls should be changed to match the input waveform. Can not be set under remote control.

(12) VERT OUT

Connects through 50-ohm coaxial cable to rear panel VERT IN.

(13) CAL OUT

Connects through 50-ohm coaxial cable to rear panel CAL IN.

(14) TRIG OUT

Connects through 50-ohm coaxial cable to rear panel TRIG IN.

(15) GROUND

Connects to chassis ground.

(16) PROBE POWER

Provides power for TEKTRONIX active probes.

(17) ON/OFF

Turns on/off the 7912AD power supply if the rear-panel PRINCIPAL POWER SWITCH is on (can be overridden by rear-panel ACTUATE connector). Lights when the power supply is turned on.

Rear Panel

The rear panel controls and connectors are shown in Fig. 2-2. The numbers in the following descriptions refer to Fig. 2-2.

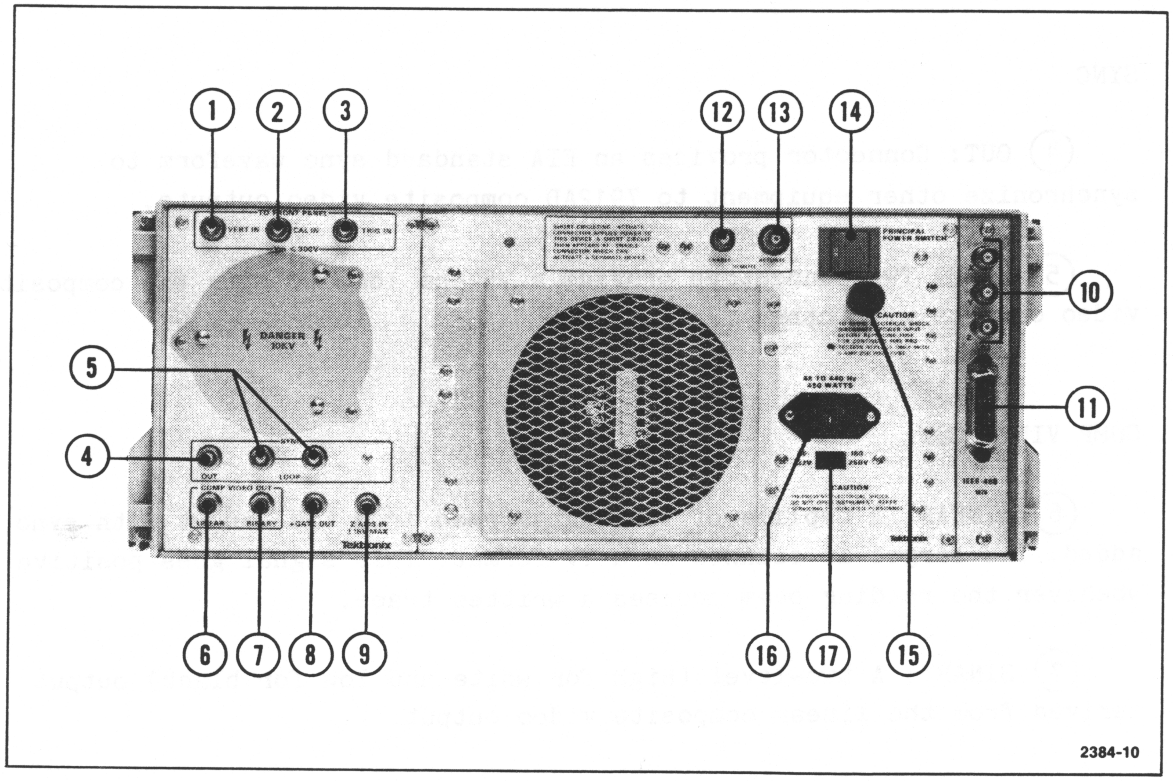


Fig. 2-2. Rear panel controls and connectors. The numbers refer to descriptions in the text of the controls and connectors.

(1) VERT IN

Connects through 50-ohm coaxial cable to front panel VERT OUT.

(2) CAL IN

Connects through 50-ohm coaxial cable to front panel CAL OUT.

(3) TRIG IN

Connects through 50-ohm coaxial cable to front panel TRIG OUT.

SYNC

(4) OUT: Connector provides an EIA standard sync waveform to synchronize other equipment to 7912AD composite video outputs.

(5) LOOP: Two connectors provide a 75-ohm loop to sync the composite video outputs with other TV equipment.

COMP VIDEO OUT

(6) LINEAR: A replica of the signal read from the target with sync added. The target is scanned in a TV format. This signal goes positive whenever the reading beam crosses a written trace.

(7) BINARY: A two-level (high for white and low for black) output derived from the linear composite video output.

(8) + GATE OUT

Provides a positive pulse with a duration equal to and coincident with the time base sweep. The amplitude is approximately 0.5 volts into 50 ohms and 10 volts into 1 megohm.

(9) Z-AXIS IN

± 1 volt input modulates the writing gun intensity over its full range; a zero volt input causes no change in the intensity selected by the intensity controls. A positive signal reduces intensity; a negative signal increases intensity.

CAUTION

Signals connected to Z-AXIS IN control writing beam intensity independently of the 6800 MPU, bypassing the firmware intensity protection. The effect of this input depends on sweep speed and the input waveform; use it with caution to prevent damage to the scan converter target. Connect only low-amplitude signals (±100 millivolts) until the effect on writing beam intensity is monitored.

(10) X,Y,Z

Provide X-Y-Z analog equivalents of the waveform data stored in memory for a refreshed display on a monitor. The outputs are disabled if there is no valid data to display, also while the 7912AD is digitizing or busy with waveform data input or output on the IEEE 488 bus. Scale factors are not displayed. There is no local control of the XYZ display -- it is programmed by the XYZ command.

(11) J13 IEEE 488-1975

Provides connection to the bus specified in IEEE Standard 488-1975.

(12) ENABLE

Applies a TTL low level between the center and outer conductors after the power supply is turned on; allows power-up of a system to be daisy-chained.

(13) ACTUATE

A TTL low level applied between the center and outer conductors turns on the 7912AD power supply. A return to a TTL high level turns off the 7912AD power supply.

(14) PRINCIPAL POWER SWITCH

Power line switch that turns on or off power input to power supply.

(15) FUSE

Replaceable power line fuse.

(16) Power Connector

CAE-22 three-prong power connector; IEC-coded.

(17) Line Voltage Selector

Selects either 115 VAC or 230 VAC operation.

Operating the 7912AD

Before operating the 7912AD, check the environmental and physical specifications at the end of Section 1; the operating temperature and airflow requirements of the instrument must be met. Be sure there is nothing blocking the fan intake (screen on rear panel) or the air exhaust holes on the sides of the instrument.

Plug-Ins

The 7912AD accepts two Tektronix 7000-series plug-ins. These can be selected to tailor the bandwidth, sweep speed, and other characteristics of the 7912AD for your application. See the specifications in Section 1 for recommended plug-ins and their performance in the 7912AD.

CAUTION

Always turn off the 7912AD power before removing or installing plug-ins to prevent damage to the circuitry.

Install an amplifier plug-in in the VERTICAL compartment and a time base plug-in in the HORIZONTAL compartment. Either programmable or non-programmable plug-ins may be used. The time base must provide readout for the 7912AD to determine that a valid sweep rate is selected. If the time base has no readout, the 7912AD main and graticule intensities are turned off.

CAUTION

Intensity and contrast controls of a dual time base plug-in bypass the firmware intensity protection, setting writing beam intensity independently of the 6800 MPU. Before installing the 7B92A Dual Time Base, reduce its Intensity and Contrast controls to minimum. Monitor the effect of these controls on writing beam intensity and use them carefully when operating the 7B92A in intensified or alternate sweep modes to avoid burning the scan converter target. Do not use other dual time base plug-ins such as the 7B52, 7B53A, or 7B92 in intensified or alternate (mixed) sweep modes because they lack a contrast control.

The 7912AD can display scale factor readout from the plug-ins in TV mode as shown in Fig. 2-3. Channel 1 of an amplifier in the VERTICAL compartment is displayed as vertical channel 1. If channel 2 of a dual amplifier is selected, it is displayed as vertical channel 2. Sweep rates of a time base in the HORIZONTAL compartment may be displayed in either horizontal channel 1 or 2, depending on the plug-in.

The readout display may differ from that obtained with a given plug-in in other 7000-series mainframes in two respects:

1) Only eight characters per channel can be displayed. This does not affect plug-ins recommended in the specifications in Section 1. It may, however, omit characters from some digital plug-ins. Also, special characters from such plug-ins may be garbled.

2) An amplifier operated in inverted mode is indicated by a minus sign in front of the scale factor, rather than a down arrow. Special characters used by 7000-series plug-ins to indicate uncalibrated readout are displayed by the 7912AD. Usually this is the greater-than sign (>) for amplifier and time base scale factors, although some plug-ins use the less-than sign (<) or X to indicate uncalibrated readout.

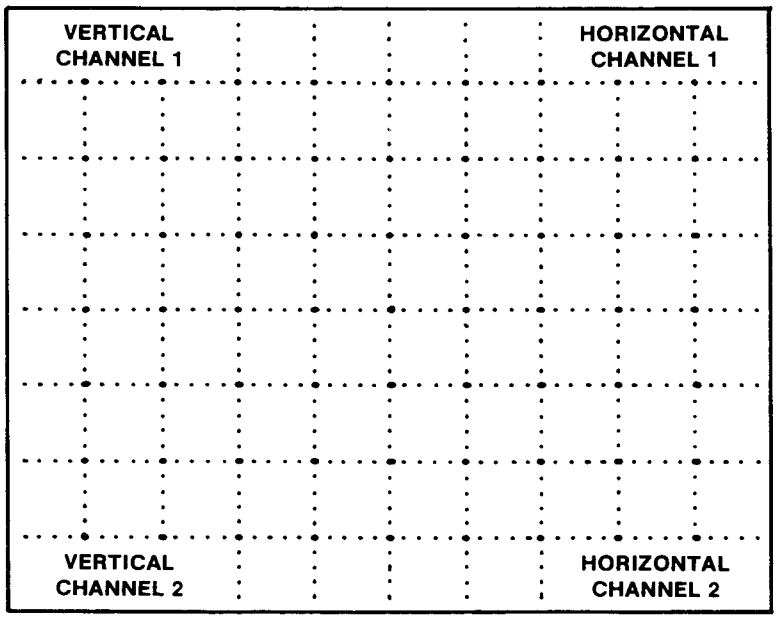


Fig. 2-3. Position of plug-in readout on the TV display.

Supplying Power

The 7912AD power cord must be connected to an outlet with a securely grounded protective-ground contact and the correct single-phase voltage. To connect power to the 7912AD, follow the instructions in Section 4.

For either the front-panel ON/OFF switch or the rear-panel ACTUATE connector to power up the instrument, the PRINCIPAL POWER SWITCH must be turned on.

WARNING

To avoid electric shock, be sure that the protective-ground circuit is not interrupted. This can allow the chassis to float to hazardous potentials. Be sure that the power cord, plug, and outlet provide a secure path to earth (ground) for the protective-ground circuit of the 7912AD.

Waveform Monitors

Waveforms acquired by the 7912AD can be viewed on monitors. A TV monitor is used to display waveforms in real-time as they are acquired in TV mode. An XYZ monitor is used to display waveforms stored in memory. An example of each monitor is shown in use with a 7912AD in Fig. 2-4. Instructions to connect the monitors are given under Cabling in Section 4.

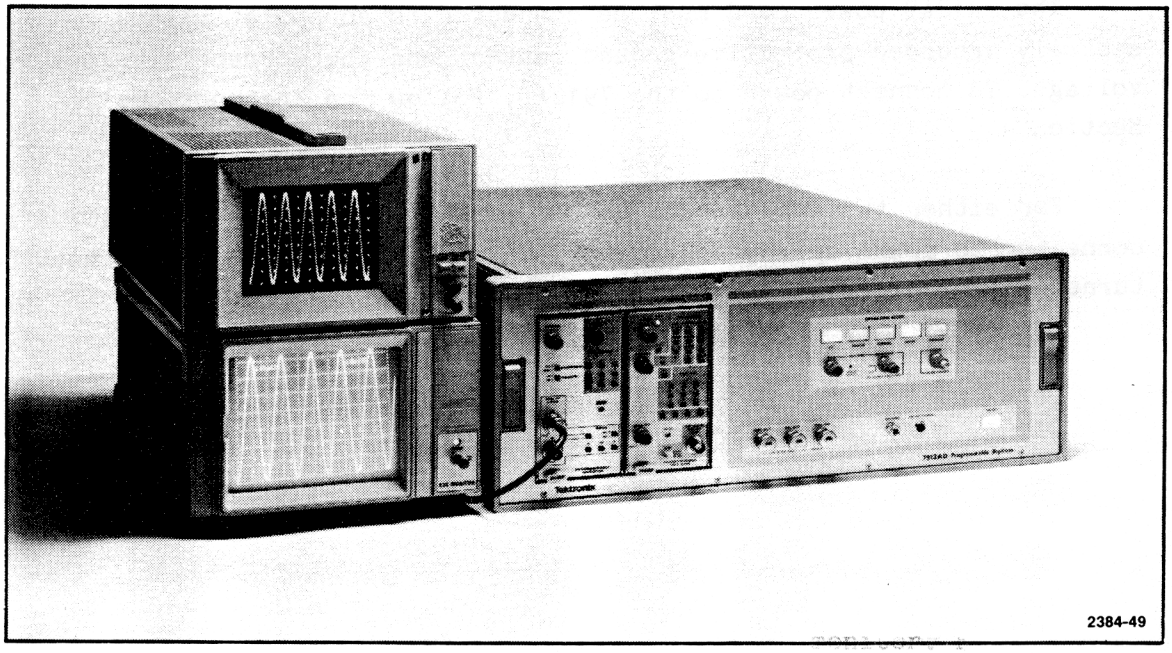


Fig. 2-4. The 7912AD is shown operating with an XYZ monitor (top) and a TV monitor (bottom).

Getting a Picture (TV Mode)

1. Set the INTENSITY controls (MAIN and GRATICULE) to minimum (counterclockwise). Although the 7912AD has protection circuitry to prevent damage to the scan converter tube by high intensity levels, set the intensity controls to minimum before turning on power to be safe.

2. Check that the 7912AD is connected to a compatible video monitor. For instructions to connect a monitor, see Section 4.

3. Turn on the video monitor and set for normal brightness.

4. Set the TV SCALE FACTORS switch to ON.

5. Set the time base plug-in for an automatic sweep at 1 millisecond/division or faster.

6. Set the amplifier plug-in position control midrange.

7. Press the ON/OFF button or apply a TTL active low on the ACTUATE connector. The button should light and the fan should start. If not, check that the PRINCIPAL POWER SWITCH is ON. The 7912AD is automatically set to the local and TV modes following power-up. If not, check that the 7912AD is not under remote control. To prevent this, disconnect the instrument from the IEEE 488 bus. Scale factors set by the plug-in controls should be displayed on the monitor after a short warm-up. If not, check the monitor connections and operating controls and that the plug-ins have readout capability.

The 6800 MPU performs a self-test on power-up before setting the operating modes to local and TV. If the test fails, the 6800 does not light LOCAL and TV, but hangs at the 6800 bus address where the test failed as a clue for diagnosing the problem.

8. After a short wait to allow the scan converter tube to warm up, increase the GRATICULE INTENSITY slowly until the graticule appears on the monitor. The TV mode graticule is shown in Fig. 2-3. Check that the DECREASE INTENSITY light does not come on. Note: If a time base without readout is installed in the horizontal compartment both the main and graticule intensities are turned off.

CAUTION

Although protective circuitry in the 7912AD is designed to prevent damage to the scan converter from high intensity levels, set the MAIN and GRATICULE INTENSITY controls carefully. Avoid excessive blooming. Do not leave either INTENSITY level at the maximum allowed by the protective circuitry for extended periods.

9. Increase the MAIN INTENSITY slowly and watch for a trace. Check that the DECREASE INTENSITY light does not come on. The trace should appear within one-half to one full turn of the MAIN INTENSITY control.

10. If the trace does not appear, press the BEAMFINDER control. This compresses the waveform within the viewing area to detect an over-scanned signal. Use the plug-in controls to bring the trace within the graticule.

11. If a trace still does not appear, recheck the instructions performed in the steps above.

12. Either or both intensity controls may need to be changed for different sweep speeds and input signals. If intensity is too high, blooming occurs. If intensity is too low, portions of the display are missing.

13. Set the FOCUS control for a well-defined trace.

14. Allow the 7912AD to warm up for 20 minutes for specified performance. During warm-up, the intensities must normally be increased slightly over their values shortly after turn-on.

Storing the Waveform Displayed in TV Mode

1. Check that the 7912AD is connected to a compatible display monitor. For instructions to connect a monitor, see Section 4.

2. Turn on the monitor and set for normal viewing level (erase the display if a storage monitor is used).

3. Press the DIGITAL button. A waveform is digitized and stored in memory on the next time base sweep, following approximately two-seconds delay for set up if changing from the TV mode. The graticule, if digitized, includes dots to mark the major divisions only.

4. If the INTENSITY controls are set too low, no data is stored, so there is no display on the monitor. Increase the INTENSITY levels a small amount and repeat step 3. If no waveform is displayed, recheck the instructions above.

NOTE

Once DIGITAL is pressed, the 7912AD begins a digitize operation; it can not be reset to TV mode until finished. This requires that the time base sweep be gated. Therefore, if the time base plug-in is not in auto, but in normal or single-sweep modes, the trigger conditions (level, slope, etc.) must be met in order to digitize. The 7912AD operating modes can then be reset, if desired.

Local Control in an IEEE 488 System

Some pointers are given here to operate the 7912AD locally when it is interfaced to an IEEE 488 system.

Taking Control. The 7912AD goes to local state automatically at power-up. All local operating controls are active, and the LOCAL button lights. An IEEE 488 bus controller can then set the instrument to remote state. In remote state, all front panel controls are inactive except ON/OFF, BEAMFINDER, LOCAL, and REMOTE; the REMOTE button is lighted. Local control can be restored by pressing LOCAL.

To prevent local control, the controller can set the 7912AD to remote with lockout state. All front panel controls are inactive except BEAMFINDER, ON/OFF, and REMOTE; the REMOTE and LOCKOUT buttons are lighted. Pressing LOCAL does not restore local control.

The REMOTE button has another function besides indicating remote control. When this button is pressed, the 7912AD asserts SRQ on the IEEE 488 bus if the interrupt is enabled. The controller may be programmed to respond to this request as desired. For example, one use for the button could be to signal the controller to restore local control when the 7912AD is in the remote with lockout state.

If both LOCAL and LOCKOUT are lighted, the 7912AD is in the local with lockout state. To the operator, this state appears the same as the local state.

When the 7912AD returns from remote to local control, the current value of all local controls is assumed. However, several programmed operating modes, such as graticule-only and XYZ, are not controlled from the front panel and do not change from their condition under remote control.

CAUTION

Immediately check the settings of the MAIN and GRATICULE INTENSITY controls when the 7912AD is returned from remote to local control. Sweep rate or the input signal may be different than when the 7912AD was last operated under local control and the intensity levels may no longer be correct.

Graticule-Only Mode. The 7912AD can be switched to a graticule-only mode. This may be used to digitize the graticule in the absence of a triggered sweep. In this mode, the graticule is written at a repetition rate that simulates the graticule intensity written after a single-sweep; the waveform is not written on the target. This mode can only be selected through the IEEE 488 Interface by the GRAT ON command. Once selected, it can not be defeated from the front panel without turning off power. (The 7912AD powers up with the graticule-only mode cleared). The IEEE 488 bus controller should be programmed to reset the graticule-only mode when restoring local control for the operator to acquire waveforms.

XYZ Outputs. The 7912AD automatically switches the XYZ display to show the results of the last digitize operation or waveform processing operation. For instance, in local mode when the DIGITAL button is

pressed, the XYZ display shows whatever is digitized as soon as the operation completes. Under remote control, waveform processing operations can be called. These include digitize and signal average, determine trace edges, and digitize defects. The display shows the results of the processing as soon as it is completed. If the digitize and signal average operation is called, for example, the signal-averaged waveform is displayed automatically.

The XYZ display mode can be changed under remote, but not local, control. For instance, the display can be changed from that of the last waveform digitized to show a signal-averaged waveform previously acquired if it is still in memory. Or the display can be turned off.

Whatever XYZ display was called under remote control, the XYZ display automatically changes to show the results of digitize or waveform processing operations that follow. So when the 7912AD is returned to local control and another waveform is digitized by pressing DIGITAL, the XYZ display automatically switches to show the waveform.

Acquiring Data

The 7912AD operates much like other 7000-series oscilloscopes when acquiring a waveform for viewing, either in TV or digital mode. Although this similarity carries over to acquiring data in digital mode, some further considerations apply.

Defects. A portion of the scan converter target that is read as data whether or not it is struck by the writing beam is called a defect. While the ideal is no defects, a few may exist on the target (see the CRT target and writing gun specification in Section 1).

Defects can be caused by burns that result from too-high intensity levels for extended periods. Apparent defects can be caused by improper calibration. Refer calibration to qualified service personnel for adjustment of the instrument within the limits stated in the service manual. Attempts to enhance performance by adjusting the instrument outside these limits can instead degrade performance, causing such problems as apparent defects.

If possible, position the trace away from defects so later processing can more easily remove them from the data. The 7912AD contains firmware routines to flag defects for such processing.

Sweep Speed and Intensity. The critical parameter in acquiring data with the scan converter is writing intensity. This is affected by the intensity and focus controls, sweep speed (set by the time base sweep rate), and trace slope (caused by changes in amplitude of the input signal).

A step transition can result in missing data during the transition or blooming before and after the transition (or both). If intensity is set too low, a portion of the trace is missing as shown in Fig. 2-5b. If intensity is set too high, the trace blooms where it travels more slowly, and the top and bottom portions of the waveform overlap. The solution is to increase the sweep rate, reducing the slope of the transition, and to increase the intensity enough to write the transition.

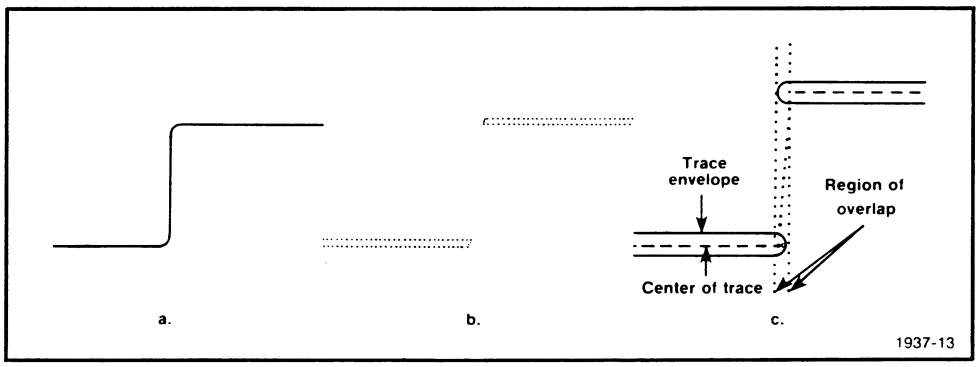


Fig. 2-5. Blooming on a step transition.

The MAIN INTENSITY control requires careful attention when digitizing a waveform with a fast transition. Although blooming on the slow portion (top and bottom) of the trace should be avoided, sufficient intensity should be achieved during the fast transition. A good compromise is shown in Fig. 2-6. Note, however, that the reading beam vertical scan through the transition (part c of the figure) may detect multiple data points. Because of lower intensity during the transition, the trace may be read as a collection of dots rather than as an envelope.

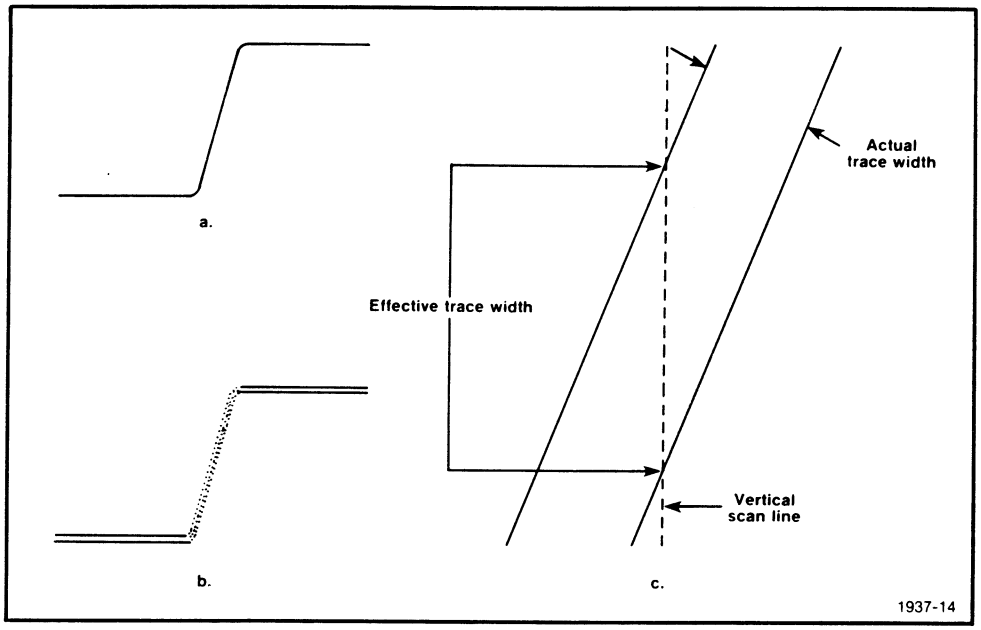


Fig. 2-6. A vertical scan through a fast transition.

How the transition in Fig. 2-6 would be detected is shown in Fig. 2-7. Part a of the figure shows a typical signal read from a strongly written portion of the target. In part b, the signal from a fast transition is weaker, but still above the detection level. However, if this signal is degraded by noise, as in part c of the figure, multiple edges of the trace are detected. It may not be possible to correct this situation by increasing intensity and/or sweep speed, but a firmware routine is provided to determine the trace edge. Other routines allow missing data to be interpolated if intensity can not be increased to fully write fast transitions.

Another waveform that requires a careful balance between intensity and sweep speed is shown in Fig. 2-8. If the intensity is increased to capture the abrupt transition at the top and bottom of the waveform as shown in part b of the figure, bloom causes the peak value to be underestimated if the top and bottom of the trace are averaged. Increasing the sweep speed to reduce the number of cycles for less abrupt transitions would improve the data.

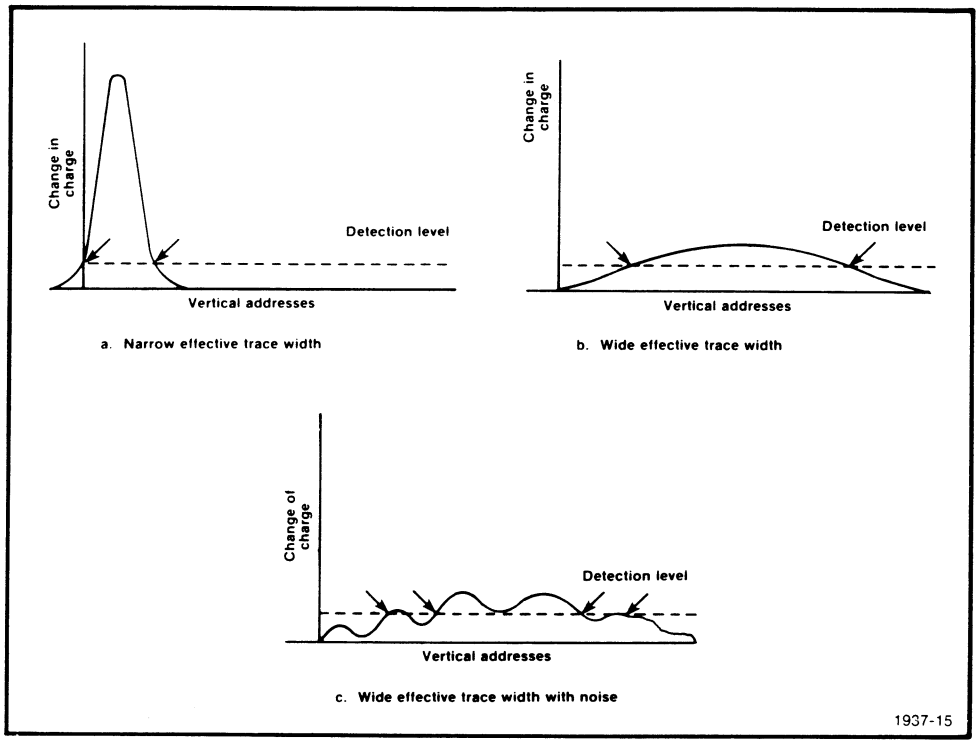


Fig. 2-7. The effect of noise on the signal detected from the target.

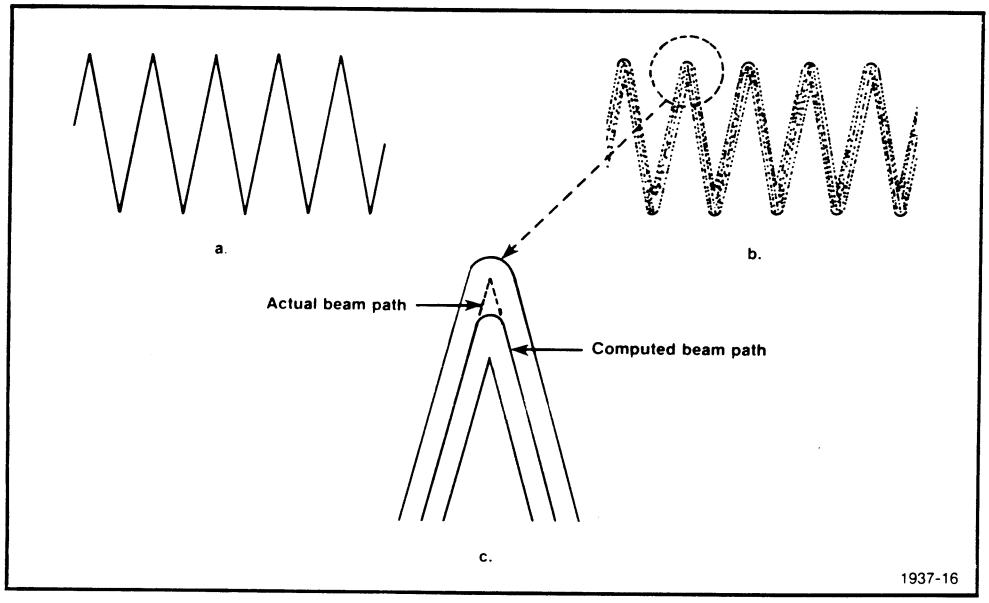


Fig. 2-8. Underextimation of trace peak due to blooming.

Programming the 7912AD

The 7912AD can be operated by remote control over the bus specified in IEEE Standard 488-1975. After the 7912AD is set to remote mode by the system controller, front-panel operating controls are disabled and their functions can be set with mnemonics sent to it in ASCII over the bus.

Data can be output by the 7912AD at the maximum data rate allowed by the slowest listener. Waveform data is output in binary rather than ASCII. This enables greater throughout, in that data is moved in fewer bytes so data transfers require less bus time.

The 7912AD provides a transparent interface between the IEEE 488 bus and TEKTRONIX 7000-series programmable plug-ins installed in the 7912AD. In effect, the IEEE 488 bus is extended to the plug-ins through the 7912AD plug-in interface.

IEEE Interface Function Subsets

IEEE Standard 488-1975 identifies the interface function repertoire of a device on the bus in terms of interface function subsets. These subsets are defined in the standard. The subsets that apply to the 7912AD are shown in Table 2-1.

These functions are implemented by the 7912AD's respone to interface control messages and remote control (device-dependent) messages.

Addressing

7912AD IEEE 488 bus addresses are selected by internal switches. Primary bus addresses can be set over the full range allowed by the IEEE 488 standard: 32 to 62 (decimal) for My Listen Address (MLA) and 64 to 94 for My Talk Address (MTA). However, the values of the 7912AD MLA and MTA are not independent of each other since they share the same lower five bits. If the switches are set for a MLA of 33, for instance, MTA is set to 65.

Secondary addresses are used to identify which of the three units, the mainframe, the vertical plug-in, or the horizontal plug-in, is addressed by MLA or MTA. The 7912AD My Secondary Address (MSA) can be set over the full range allowed by the IEEE 488 standard: 96 to 126 (decimal).

TABLE 2-1

7912AD INTERFACE FUNCTIONS

FUNCTION	SUBSET	CAPABILITY
Source handshake	SH1	Complete. Instrument allows minimum settling time on the DIO (data) lines before asserting DAV (T_1 in the SH state diagram in the standard): $\geq$ 1100 ns for the first byte after ATN is released and $\geq$ 500 ns for the remaining bytes in a message.
Acceptor handshake	AH1	Complete.
Extended talker	TE6	Complete except instrument can not be set to talk-only mode locally; includes response to serial poll; requires secondary address.
Extended listener	LE4	Complete except instrument can not be set to listen-only mode locally; requires secondary address.
Service request	SR1	Complete.
Remote/local	RL1	Complete.
Parallel poll	PPØ	No response to parallel poll.
Device clear	DC1	Complete.
Device trigger	DT1	Complete.
Controller	CØ	None.

The bus addresses of programmable plug-ins are also determined by the 7912AD MLA, MTA, and MSA. The plug-ins share the 7912AD MLA and MTA. The plug-in MSAs are set by the 7912AD MSA in the following manner:

Compartment	**Plug-in MSA**
Vertical	7912AD MSA + 1
Horizontal	7912AD MSA + 2

If the 7912AD internal switches are set for a MSA of 97, for instance, the vertical plug-in MSA is 98, and the horizontal plug-in MSA is 99. If programmable plug-ins are used, the 7912AD MSA should not be set higher than 124 to allow address space for the plug-ins. Instructions for setting the bus address switches are found in Section 4.

Remote/Local Function

The remote/local function of the 7912AD and its programmable plug-ins (if installed) is controlled by the system controller and the LOCAL button. The remote/local function includes four states: local, remote with lockout, and local with lockout. These states are commonly referred to as local mode for local and local with lockout states and remote mode for remote and remote with lockout states.

Local. The 7912AD and programmable plug-ins enter the local state as part of the power-up routine. To enter local state from remote state, one of the following three conditions must occur:

1) The LOCAL button is pressed.

2) The remote enable (REN) line changes from asserted to unasserted.

3) The instrument receives the GTL interface message (ATN asserted) while addressed as a listener.

If the 7912AD is executing a command or is performing a digitize operation, it waits until finished to return to local. The plug-ins return to local with the 7912AD.

When the 7912AD enters the local state, it lights the LOCAL button and assumes the settings of the MAIN INTENSITY, GRATICULE INTENSITY, FOCUS, TV SCALE FACTORS, and BEAM FINDER controls. Other programmable functions, such as XYZ output, remain in their current condition when switching from remote to local. (At power-up, they assume the conditions noted in Table 2-2).

Although the instrument continues to process messages it receives over the bus, it does not execute device-dependent commands that affect local operating controls or alter the state of data memory. Those commands that are ignored are noted in Table 2-2.

Remote. The 7912AD and programmable plug-ins make the local to remote state transition when the 7912AD receives MLA with ATN and REN asserted. Since the plug-ins and the 7912AD share MLA, all three switch to remote state after power-up when the controller addresses any one as a listener with REN asserted.

When the 7912AD enters the remote state, it lights the REMOTE button and continues conditions of all operating functions, whether set by local controls or commands over the bus. Changes in local controls are ignored, except for BEAM FINDER, ON/OFF, LOCAL, and REMOTE. All commands received over the bus are executed.

Lockout. When the local lockout (LLO) interface message is received with ATN asserted, the 7912AD lights the LOCKOUT button and enters the remote with lockout state from remote state, or the local with lockout state from local state. Programmable plug-ins remain in either remote or local state, whichever they were in when LLO was received.

In remote with lockout state, both REMOTE and LOCKOUT are lighted. There is no change in the condition of operating functions. The front panel operates the same as in remote state except that the LOCAL button is not active. All commands are executed.

In local with lockout state, both LOCAL and LOCKOUT are lighted. Since this state allows full local control of the 7912AD and plug-ins, it appears the same as the local state to the operator. There is a difference to the programmer, however. When the 7912AD receives MLA with ATN asserted in local with lockout state (assuming REN has not been unasserted), it goes to the remote with lockout state; if in local state under the same conditions, it goes to remote state.

Remote Control Messages

7912AD remote control messages are device-dependent messages on the IEEE 488 bus. As such, they are not specified in the IEEE standard. 7912AD messages do, however, conform to Tektronix standards intended to enhance compatibility with other IEEE 488 bus-interfaced instruments. To accomplish this, codes and syntax are intended to be unambiguous, correspond to those used by similar devices, and be as simple and obvious as possible. This minimizes the cost and time required to program the 7912AD by making it easier for the programmer to write and understand the needed device-dependent code.

The 7912AD responds to device-dependent messages that contain one or both of two types of commands, set and query. A set command causes the instrument either to set an operating mode or to begin a memory control operation. A query command causes the instrument to return the status of a specified operating parameter.

7912AD remote control messages are sent in ASCII (alpha in upper case) except for the binary block input by one command (LOAD). The 7912AD responds in ASCII, except when transmitting a waveform array; arrays are sent in binary as explained under Waveform Data I/O. The 7912AD ignores the parity bit on ASCII input and always sets it to zero on ASCII output.

Input Buffering and Execution. Messages are input and commands executed under control of the 6800 MPU. A remote control message begins when the 7912AD is addressed as a listener, ATN is unasserted, and the transmitting device begins talking. The message ends when the message terminator is detected by the 7912AD. The 6800 MPU buffers all messages it receives. It does not begin execution of the commands until:

1) The buffer becomes full, or

2) The message delimiter is received.

When either of these conditions occurs, the 7912AD busy status is set; the instrument asserts NRFD unless it is unlistened and reports busy status (bit five of the status byte) if polled. No more commands are accepted until all commands in the buffer are executed; then the busy status is reset and the 7912AD can continue to listen.

The 6800 MPU executes input messages containing multiple commands one command at a time. Commands in a string are handled according to these rules:

1) If a command sets an operating parameter, further commands are not executed until the current command is completed.

2) If the 6800 MPU decodes a digitize command, it initiates the memory controller operation and proceeds to execute further commands that do not conflict with the digitize. Such commands are a set command that would affect the data (such as intensity) or would initiate another memory controller operation.

3) Once any memory controller operation except XYZ is begun, the 6800 MPU waits to execute further memory control commands until the current operation completes. XYZ is an exception because it is an ongoing activity of the memory controller when it has no other task. If the memory controller operation does not digitize or output data, however, the 6800 is free to execute other commands that set or query operating parameters. If there are no further commands, it resets the busy status.

4) When the 6800 MPU decodes a command requesting output, such as a query or output command (READ, DUMP, or REP), it remains busy until allowed to complete the data transfer. It refuses further input until talked and the data is read. If the 7912AD is untalked while transmitting data, it remains busy and waits to finish the transmission. The controller can interupt and reset the talker function by sending the UNT interface message or addressing the 7912AD as a listener. To reset the 6800 output buffer and busy status, however, the controller must perform a device clear with the DCL or SDC interface messages.

Command Syntax. Formats given for the set and query commands are intended as guides and are not intended to fully define the format.

The following format symbols are used:

<> indicates a defined element
[] indicates the element or group of elements are optional and may be omitted
... follows an element or group of elements that may be repeated

The following delimiters are used to punctuate 7912AD commands:

Delimiter	Follows
<space>	Header
<comma>	Argument
<semicolon>	Message unit (command)

When listening, the 7912AD responds to either of two message delimeters:

1) The EOI line asserted concurrently with the last byte in the message whether data, a format character, or a lower-order delimiter such as semicolon. This is the standard delimiter for Tektronix instruments.

2) The ASCII code for line feed (LF) sent as a byte following the message and any format character or lower-order delimiter. This is an alternate delimiter provided for compatibility with some instruments from other manufacturers.

The 7912AD responds to either EOI or LF according to the position of an internal jumper. Since the cover must be removed to get at the jumper, refer selection to qualified service personnel; instructions are found in Section 4.

With EOI selected as the message terminator, any combination of format characters can be inserted at the beginning or end of a message or after a delimiter. Format characters are carriage return (CR), LF, or space.

Format characters can also be used with LF selected as the message terminator. However, the 7912AD interprets LF as the end of the message; it holds up the data transfer by asserting NRFD and executes all commands in the buffer before continuing to handshake data.

When talking, the 7912AD uses EOI to delimit a message. It asserts the EOI line concurrently with the last byte in the message, normally the message unit delimiter (semicolon). However, if the internal jumper is set for LF as the message delimiter, the 7912AD adds CR and LF beyond the normal end of the message (semicolon) and asserts EOI with LF. The 7912AD does not source more data until retalked or serial polled. If the 7912AD has no message to send when it is talked, it responds with a single data byte, hex value FF -- all data lines asserted, along with EOI.

Numbers. Numbers are assumed to be ASCII-coded decimal digits (except for waveform data). Two kinds of numbers are used:

Representation	Description
<NR1>	Unsigned integers including 0
<NR3>	Signed scientific notation

Numbers in NR1 notation are signed or unsigned integers; for positive integers, the plus sign is optional.

Numbers in NR3 notation are used only for 7912AD output in response to some queries. These are floating-point numbers expressed in scientific notation. The mantissa includes a decimal point and is preceded by a sign. The exrad following the mantissa begins with the character E, followed by a plus or minus sign and then one or more digits for the exponent of the multiplier. Examples are:

+1.37E-3	(for 1.37×10^{-3})
-1.E+4	(for -1×10^{4})
<space>0.E+0	(for Ø)

An explicit definition of these number types is given in ANSI X 3.42-1975, "American National Standard for Representation of Numeric Values in Character Strings for Information Exchange."

Set Commands. Unless noted as query only, headers and arguments in Table 2-2 can be used as set commands. The last letter of four-letter headers and arguments can be omitted from set commands.

The format for a single set command is:

<header><space><argument>[<semicolon>]

More than one argument can be used with the READ and DUMP commands. For example:

READ<space><argument>[<comma><argument>]...[<semicolon>]

Examples of single set commands are:

```
MODE DIG
READ VER,PTR,SC1;
```

More than one set command can be sent as part of a single message. This requires the following syntax:

<set command><semicolon><set command>[<semicolon><set command>]...
[<semicolon>]

An example of multiple set commands in a single message is:

MOD DIG;GRAT OFF;DIG DATA;

One rule must be followed if more than one set command is transmitted as part of the same message: only one command that requires the 7912AD to output data can be contained in a single message. Such a command must be placed last in the message; READ, REP, and DUMP are examples of this kind of command. See Input Buffering and Execution above.

Query Commands. Unless noted as set only, headers in Table 2-2 can be used as query commands. A query is executed in either remote or local mode. A message that contains only a query command requires the following syntax:

<header><question mark>[<semicolon>]

An example is:

MODE?

A message can contain only one query command. The query may be preceded by one or more set commands, however. In this case, the query must be the last message unit (command) and must not be preceded by a set command that requires output, such as READ. A message that contains both set commands and a query command requires the following syntax:

<set command><semicolon>[<set command><semicolon>]...
<query command>[<semicolon>]

An example is:

MODE DIG;MODE?

Any commands in a message following a query are ignored as explained under Input Buffering and Execution earlier.

The 7912AD responds to a query with a message similar to the set command format when it is next made a talker. Unless noted in Table 2-2, the syntax is:

<header><space><argument><semicolon>

For example, the query:

MODE?

is answered (in digital mode):

MODE DIG;

TABLE 2-2

7912AD COMMAND SET

Header	Argument	Description	Notes
MOD[E]	TV	Set instrument to TV mode	3,8
	DIG	Set instrument to digital mode	8
DIG	DAT[A]	Digitize data	1,4,8
	GRA[T]	Digitize graticule only	1,4,8
	SSW	Digitize on single sweep trigger	1,4,8
	DEF,<NR1>	Digitize only defects n times	1,4,8
	SA,<NR1>	Digitize and signal average 1 to 64 times	1,4,8
DT	ON	Wait for GET interface message to digitize	
	OFF	Do not wait for GET interface message to digitize	3
GRAT	ON	Write only the graticule on the target	8
	OFF	Reset graticule-only mode	3,8
XYZ	ON	Enable XYZ outputs to display raw data	4,8
	OFF	Disable XYZ outputs	3,4,8
	RAW	Same as ON argument	4,8
	ATC	Enable XYZ outputs to display ATC data	4,8
	SA	Enable XYZ outputs to display signal-averaged data	4,8
	EDG[E]	Enable XYZ outputs to display edge-determined data	4,8
	DEF	Enable XYZ outputs to display defects data	4,8
MAI	<NR1>	Set main intensity from 0 to 1023	8
GRI	<NR1>	Set graticule intensity from 0 to 255	8
FOC	<NR1>	Set focus from 0 to 63	8
SSW	ARM	Arm single-sweep trigger	8
	DIS	In single-sweep mode, but disarmed	2
	NSS	Not in single-sweep mode	2

TABLE 2-2 (cont.)

Header	Argument	Description	Notes
TV	ON	Turn on TV display of scale factors	8
	OFF	Turn off TV display of scale factors	8
REM	ON	Assert SRQ when REMOTE pressed	
	OFF	Do not assert SRQ when REMOTE pressed	3
OPC	ON	Assert SRQ when operation complete	
	OFF	Do not assert SRQ when operation complete	3
DEF	ON	Flag defects in raw vertical data	4,8
	OFF	Reset defect flags in raw vertical data	3,4,8
LOA[D]	<BINARY BLOCK>	Load defects array from IEEE 488 bus	1,4,6,8
ATC		Perform simple ATC on raw vertical data	1,4,8
INT	<NR1> or NONE	Max. no. of consecutive interpolated data points	2
EDG[E]		Determine edges of raw waveform	1,4,8
TW	<NR1>	Set max. trace width for EDGE from zero to 512	4
RT	<NR1>	Set max. ratio of trace widths for EDGE from 1 to 32767	5
SET	<MESSAGE UNITS>	Settings of programmable functions (header is omitted)	2
TES[T]		Self-test data memory	1,4,8
REA[D]	VER	Transmit vertical data array	1,4,7
	PTR	Transmit pointers data array	1,4,7
	SC1	Transmit channel 1 scale factors	1,7
	SC2	Transmit channel 2 scale factors	1,7
	ATC	Transmit average-to-center data	1,4,7
	SA	Transmit signal-averaged data	1,4,7
	EDG[E]	Transmit edge-determined data	1,4,7
	DEF	Transmit defect data	1,4,7
REP	<NR1>	Repeat DIG DAT/READ PTR,VER sequence 1 or more times	1,4,8

TABLE 2-2 (cont.)

Header	Argument	Description	Notes
DUM[P]	RAW PR	Dump raw data memory area Dump processed data memory area	1,4,7 1,4,7
VS1	<NR3> or NONE	Scale factor for vertical channel 1	2
VS2	<NR3> or NONE	Scale factor for vertical channel 2	2
HS1	<NR3> or NONE	Scale factor for horiz. channel 1	2
HS2	<NR3> or NONE	Scale factor for horiz. channel 2	2
VU1	<CHARACTERS>	Units for vertical channel 1	2
VU2	<CHARACTERS>	Units for vertical channel 2	2
HU1	<CHARACTERS>	Units for horizontal channel 1	2
HU2	<CHARACTERS>	Units for horizontal channel 2	2
ERR	<NR1> or NONE	Code for error indicated in last status byte reported	2
SRQ	NULL	Service request code (7912AD provides no other response)	2
ID	<CHARACTERS>	Identity of instrument	2
LIMITS*	<NR1>,<NR1>	Main intensity limit and graticule intensity limit	2

NOTES:

1 -- Can only be used as set command.
2 -- Can only be used as query command.
3 -- Power-up condition.
4 -- Memory control operation.
5 -- Divided by 32 when received by 7912AD.
6 -- BINARY BLOCK is defined under Waveform Data I/O.
7 -- More than one argument allowed, arguments delimited by commas.
8 -- Not executed in local state as set command (does not apply to query).

*Serial Number B050000 & Up

Response to Interface Control Messages

The 7912AD does not respond to the following interface control messages:

PPC - Parallel poll configure
PPU - Parallel poll unconfigure
TCT - Take Control

The 7912AD responds to the following interface control messages in the following manner when the messages are sent as required by the IEEE 488 standard:

GTL - Go to local. This causes the instrument to go to local mode as described under Remote/Local Function earlier in this section.

LLO - Local lockout. If in the remote state, this causes the instrument to go to remote with lockout state. If in local state, this causes the instrument to go to local with lockout state. See Remote/Local Function earlier in this section.

SDC, DCL - Selected device clear and device clear. Either of these messages resets the IEEE 488 bus input and output buffers, halts any memory controller operation, and resets the status byte (except power-up status). If the memory controller was not modifying the data memory in response to a DIG, ATC, LOAD, TEST, or DEF command, it resumes the XYZ display.

SPE, SPD - Serial poll enable and disable. Instrument has full serial poll capability; the response by the 7912AD to a serial poll is described under Status Byte.

GET - Group execute trigger. If enabled by **DT ON**, this command causes a current digitize operation to proceed on the next time base sweep. If the GET response was not enabled or was disabled by **DT OFF**, or the instrument is not currently executing a DIG command, the GET has no effect.

IFC - Interface clear. This resets interface functions only and does not affect operating modes of the instrument. If the instrument was a talker, for instance, it returns to the talker idle state.

Interface messages are shown in the code chart, Table 2-3.

TABLE 2-3
ASCII CODES AND
IEEE 488 (GPIB) MESSAGES

B7 B6 B5 / BITS B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		NUMBERS SYMBOLS		UPPER CASE		LOWER	
0 0 0 0	0 NUL 0 (0)	20 DLE 10 (16)	40 SP 20 (32)	60 0 30 (48)	100 @ 40 (64)	120 P 50 (80)	140 \` 60 (96)	160 p 70 (112)
0 0 0 1	1 GTL SOH 1 (1)	21 LLO DC1 11 (17)	41 ! 21 (33)	61 1 31 (49)	101 A 41 (65)	121 Q 51 (81)	141 a 61 (97)	161 q 71 (113)
0 0 1 0	2 STX 2 (2)	22 DC2 12 (18)	42 " 22 (34)	62 2 32 (50)	102 B 42 (66)	122 R 52 (82)	142 b 62 (98)	162 r 72 (114)
0 0 1 1	3 ETX 3 (3)	23 DC3 13 (19)	43 # 23 (35)	63 3 33 (51)	103 C 43 (67)	123 S 53 (83)	143 c 63 (99)	163 s 73 (115)
0 1 0 0	4 SDC EOT 4 (4)	24 DCL DC4 14 (20)	44 $ 24 (36)	64 4 34 (52)	104 D 44 (68)	124 T 54 (84)	144 d 64 (100)	164 t 74 (116)
0 1 0 1	5 PPC ENQ 5 (5)	25 PPU NAK 15 (21)	45 % 25 (37)	65 5 35 (53)	105 E 45 (69)	125 U 55 (85)	145 e 65 (101)	165 u 75 (117)
0 1 1 0	6 ACK 6 (6)	26 SYN 16 (22)	46 & 26 (38)	66 6 36 (54)	106 F 46 (70)	126 V 56 (86)	146 f 66 (102)	166 v 76 (118)
0 1 1 1	7 BEL 7 (7)	27 ETB 17 (23)	47 ' 27 (39)	67 7 37 (55)	107 G 47 (71)	127 W 57 (87)	147 g 67 (103)	167 w 77 (119)
1 0 0 0	10 GET BS 8 (8)	30 SPE CAN 18 (24)	50 (28 (40)	70 8 38 (56)	110 H 48 (72)	130 X 58 (88)	150 h 68 (104)	170 x 78 (120)
1 0 0 1	11 TCT HT 9 (9)	31 SPD EM 19 (25)	51) 29 (41)	71 9 39 (57)	111 I 49 (73)	131 Y 59 (89)	151 i 69 (105)	171 y 79 (121)
1 0 1 0	12 LF A (10)	32 SUB 1A (26)	52 * 2A (42)	72 : 3A (58)	112 J 4A (74)	132 Z 5A (90)	152 j 6A (106)	172 z 7A (122)
1 0 1 1	13 VT B (11)	33 ESC 1B (27)	53 + 2B (43)	73 ; 3B (59)	113 K 4B (75)	133 [5B (91)	153 k 6B (107)	173 { 7B (123)
1 1 0 0	14 FF C (12)	34 FS 1C (28)	54 , 2C (44)	74 < 3C (60)	114 L 4C (76)	134 \ 5C (92)	154 l 6C (108)	174 ¦ 7C (124)
1 1 0 1	15 CR D (13)	35 GS 1D (29)	55 - 2D (45)	75 = 3D (61)	115 M 4D (77)	135] 5D (93)	155 m 6D (109)	175 } 7D (125)
1 1 1 0	16 SO E (14)	36 RS 1E (30)	56 . 2E (46)	76 > 3E (62)	116 N 4E (78)	136 ^ 5E (94)	156 n 6E (110)	176 ~ 7E (126)
1 1 1 1	17 SI F (15)	37 US 1F (31)	57 / 2F (47)	77 ? UNL 3F (63)	117 O 4F (79)	137 UNT _ 5F (95)	157 o 6F (111)	177 RUBOUT (DEL) 7F (127)

ADDRESSED COMMANDS

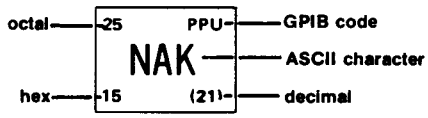
UNIVERSAL COMMANDS

LISTEN ADDRESSES

TALK ADDRESSES

SECONDARY ADDRESSES OR COMMANDS

KEY TO CHART



Error Handling

Errors are reported whether in local or remote mode. They are reported in the following manner.

Command or Execution Error. If a command or execution error is detected:

1. Command execution is halted at the point where the error is detected.

2. The command input buffer is cleared until the message delimiter is detected.

3. The status byte is set to show the error when read by controller-in-charge.

4. No memory data output is started after the error is detected.

5. The instrument asserts SRQ to report the error status.

6. The instrument remains ready for further input.

Internal Error. If an internal error is detected:

1. The status byte is set to show the error when polled.

2. The instrument asserts SRQ to report the error status.

3. If data output is in progress, it may be interrupted.

4. The instrument remains ready for input.

Power Fail Error. If a power fail error is detected:

1. Command execution is immediately halted.

2. Power fail status is set.

3. The instrument asserts SRQ.

@

4. The instrument remains halted until restarted.

If the instrument detects either a command or execution error and an internal error, the internal error is reported first. If more than one internal error is detected, the last one to occur is the only one of that type reported. If more than one execution or command error is detected, the last one of either type to occur is the only one of either type reported.

Error codes returned in response to an error command query are shown in Table 2-4. Three digits are used. The first digit identifies the type of error and corresponds to the abnormal system status byte: 1XX = command error, 2XX = execution error, 3XX = internal error, and 4XX = power fail error. The code always refers to the last status byte reported.

TABLE 2-4

ERROR CODES

CODE	DESCRIPTION
NONE	No error to report.
102	Invalid command header.
103	Invalid command argument.
201	Attempt to arm single sweep while time base is not in single-sweep mode.
202	Checksum error for binary block input by LOAD command.
203	Byte count error for binary block input by LOAD command.
206	Attempt to digitize with invalid sweep rate (slower than 1 milli-second/division).
302	Data memory fault detected in 2900 microprocessor system while performing TEST command or power-up initialization.
304	Invalid or missing readout data from plug-ins.
305	Waveform data memory overwritten.
306	No data for signal averaging.

TABLE 2-4 (cont.)

CODE	DESCRIPTION
307	Defects array is full (it is not allowed to overflow into vertical array).
308	6800 MPU received an interrupt that it can not identify.
401	Power failure is imminent.

Status Byte

The status byte obtained from the instrument during a serial poll contains the following information:

Bit	Meaning
8	Device status = 1; system status = Ø
7	Service requested
6	Abnormal condition = 1; normal condition = Ø
5	Busy
4	Device/system status code
3	Device/system status code
2	Device/system status code
1	Device/system status code

Bits 7 and 5 are flags. Bit 7 indicates the instrument asserted SRQ for the condition being reported. Bit 5 indicates the 6800 MPU is busy executing a command or its input buffer is full. If bit 5 is set, the 7912AD holds up the handshake of any more device-dependent messages by asserting NRFD if it is addressed as a listener.

Any existing abnormal system status is reported first. Both an internal error and either an execution or command error can be saved and reported as discussed under Error Handling. One normal system status byte and one device dependent status byte can also be saved and reported (in that order). Power-up overrides all other status as noted below.

The instrument always asserts SRQ for abnormal system status and power-up. It can be programmed to assert or not assert SRQ for remote request status and operation complete status with the REM and OPC commands. The instrument unasserts SRQ when it has reported the condition for which SRQ was asserted or when it is cleared by the DCL or SDC interface messages.

Device Dependent Status. This is reported only when there is no system status to report. The following status byte is returned:

8 7 6 5 4 3 2 1

1 X 0 X 0 0 0 1 - Remote Request

Remote request indicates that the REMOTE front-panel button has been pushed. Remote request becomes set when the button is pushed and is reset when the instrument status is read or a device clear performed.

Normal Condition System Status. The following status bytes are returned:

8 7 6 5 4 3 2 1

0 0 0 X 0 0 0 0 - No Condition
0 1 0 X 0 0 0 1 - Power Up
0 X 0 X 0 0 1 0 - Operation Complete

The power-up condition replaces any other status. It exists after the instrument has been turned on and continues until the status is read. Operation complete indicates that a DIG or TEST operation has completed. It is set upon completion of the operation and is reset when the status is read, another such operation is requested, or a device clear is performed.

Abnormal Condition System Status. Abnormal conditions (errors) are reported before other status (except when replaced by power-up status). The following status bytes are returned:

8 7 6 5 4 3 2 1

0 1 1 X 0 0 0 1 - Command Error
0 1 1 X 0 0 1 0 - Execution Error
0 1 1 X 0 0 1 1 - Internal Error
0 1 1 X 0 1 0 0 - Power Fail Error

Command error indicates that the instrument has received a command that it can not understand or implement under any circumstances. The command does not affect the state of the instrument.

Execution error indicates that the instrument has received a command that it understands but can not implement due to the current state of the instrument. The command does not affect the state of the instrument. For example, this error would be reported if the instrument received the DIG SSW command while the time base plug-in was not in single-sweep mode.

Internal error indicates that the instrument has detected a hardware failure, an invalid configuration of the instrument (such as a missing plug-in), or an invalid memory state (such as a memory overwrite during a digitize).

Power fail error indicates that a power failure is imminent. The instrument remains capable of responding to a serial poll for at least 10 milliseconds. If power is restored at any time, this condition is replaced by the power-up condition.

Codes for errors of the above types can be read by the error command. For the codes, see Error Handling.

Waveform Data I/O

Output in response to query commands is covered under Remote Control Messages and Command Description earlier in this section. This discussion concerns output of waveform data that has been acquired by the 7912AD. It also covers the only case of waveform data input, that of the LOAD command. Waveform data is output from the 7912AD data memory to the IEEE 488 bus by the memory controller. The LOAD command, however, requires the action of both the 6800 microprocessor and the 2900 memory controller. These systems and the data memory are discussed in the Block Drawing and the Waveform Storage descriptions in Section 3.

In general, waveform data are transferred in order from left-to-right of trace. Although the data is not acquired from the scan converter in this order, it is reordered by the memory controller for output. The DUMP RAW command is an exception to this, however. In this case the data is transmitted just as it was detected from the target.

Block Binary Format. Waveform data is transferred by the 7912AD in binary blocks. The block binary format is:

%<BYTE COUNT>[<DATA VALUE>. . .]<CHECKSUM>;

where:

% is the ACSII percent character indicating a binary block.

BYTE COUNT is a 16-bit binary number indicating how many bytes remain to be transmitted in the block including the checksum, but not including the message unit delimiter (semicolon). It is sent in two bytes, more significant byte first.

DATA VALUE is a 16-bit binary number sent in two bytes, more significant byte first. If the data value is less than 16 bits in length, it is sent right-justified with unused bits set to zero. For example, the decimal number 511 would be sent in two bytes: 00000001 and 11111111.

CHECKSUM is an eight-bit binary number sent in a single byte. It is computed by taking the modulo-256 sum of all preceding bytes in the block except %, that is, by summing in eight bits the value of the preceding bytes but throwing away the carry each time it occurs. The sum is converted to its 2's complement before transmission. This allows the receiver to compute the sum in the same manner and merely check that it is zero after the checksum byte is received.

; is the ASCII semicolon character delimiting the message unit. If this is the only or last message unit in the message, the message terminator is also sent.

The binary block for a simple two-value array is shown in Fig 2-9.

READ PTR,VER and REP Commands. The READ PTR,VER command and the REP command that incorporates the REP PTR,VER command return two arrays, the pointer and vertical arrays. These can be used to reconstruct the waveform acquired by the 7912AD. The arrays are processed from the raw data stored during a 7912AD digitize operation and are equivalent to the vertical and pointer arrays used by TEK SPS BASIC Software to handle 7912AD waveforms.

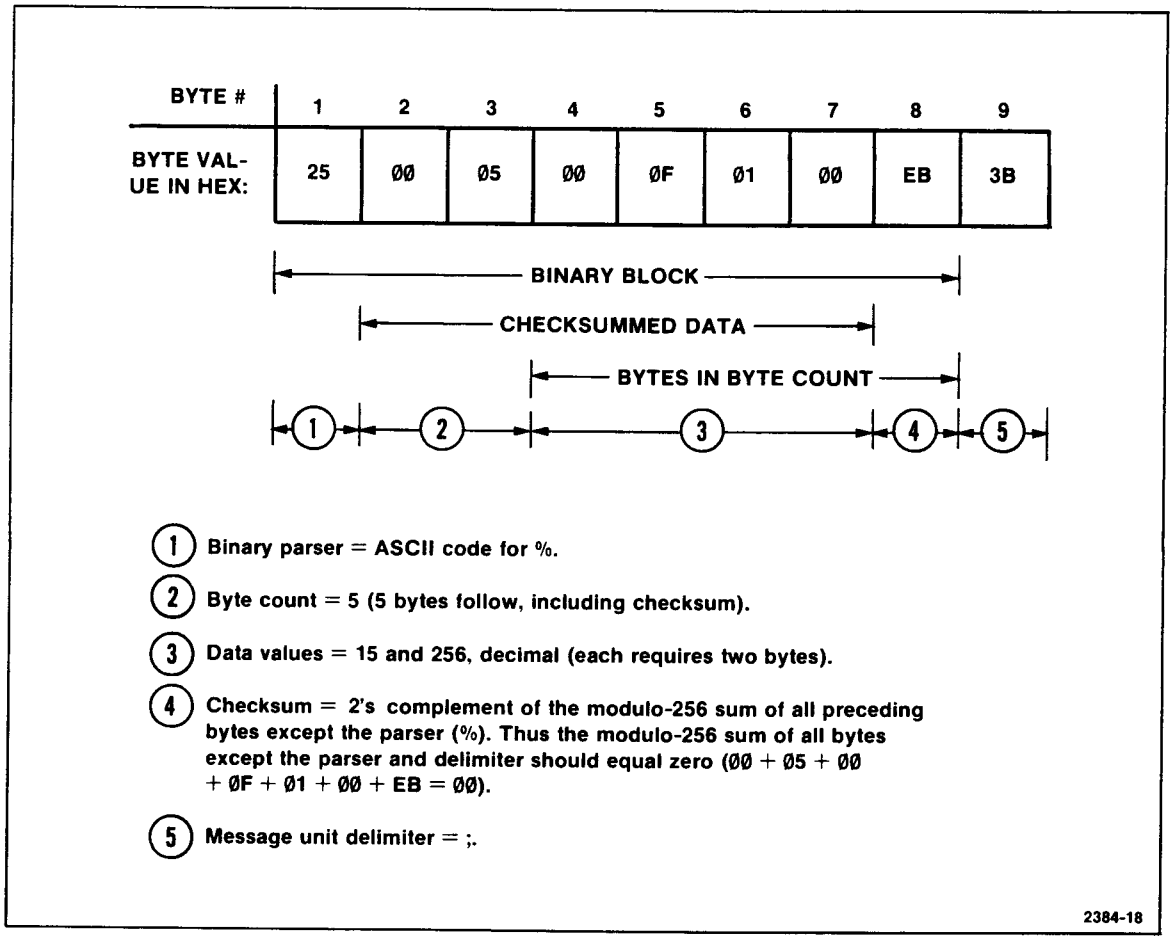


Fig. 2-9. A simple binary block showing the format elements.

Two arrays are necessary because the waveform acquired by the 7912AD is a multi-valued function. It typically contains at least two vertical (Y) values for each horizontal (X) point because of the nature of the scan converter (see Section 1). Y values normally represent voltage, and X points normally represent time.

The pointer array is based on the X (horizontal) array that is stored during a digitize operation. The pointer array is computed using the X array, which records the number of Y values stored for each X (horizontal location or point in time). 512 data values are sent in the pointer array, one for each horizontal point on the waveform. They are sent in order from left to right. Each pointer value points to the last data word in the vertical array sent for the corresponding X (horizontal)

location. Pointers for empty X locations are set to -1 until the first vertical data value is stored. A pointer with the same value as the previous pointer indicates there is no vertical data for that X location. The relationship between the pointer and vertical arrays is shown in Fig. 2-10.

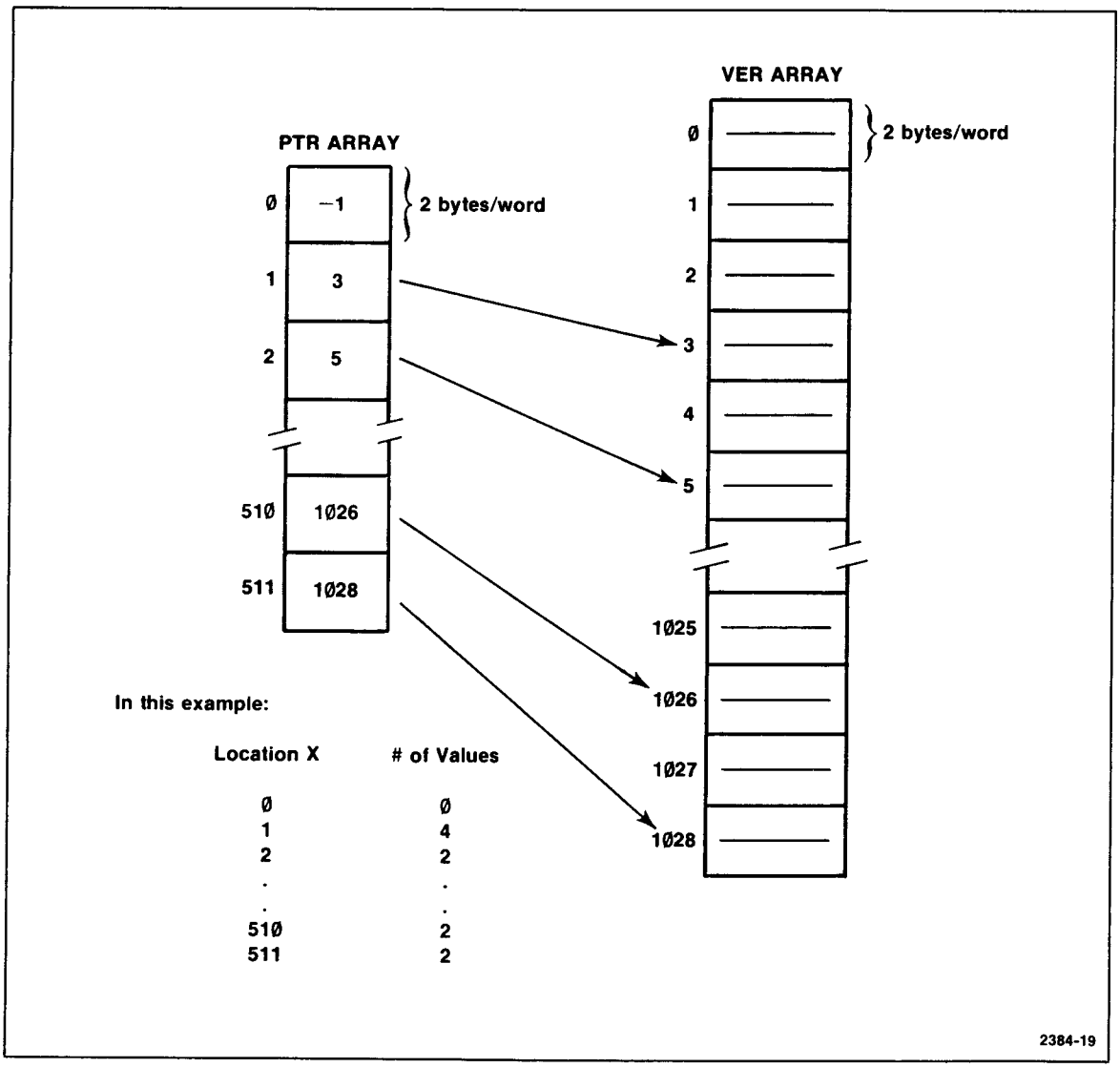


Fig. 2-10. The PTR array is an index to the VER array. The pointer values indicate how many vertical data values are output from each horizontal (X) location on the target.

The vertical array returned by the 7912AD contains up to 3584 data values. These are the values detected during the last digitize operation. They are reordered by internal processing so they are sent in order from left to right of trace. For an X location with more than one vertical data point (typically there are two--one for the top and one for the bottom of trace), the highest value (top of trace) is sent first. Other values for that X follow in descending order. Thus, the first value transmitted is the upper left-most data element, and the last value is the lower right-most data element as viewed on an X-Y graph. Such a graph is provided by the XYZ outputs when connected to a display monitor.

Because vertical values range from zero to 511, they fill only the lower nine bits of a data word; all bits except the LSB in the first byte of the word are unused (set to zero). However, the DEF ON command, sets bit 10 as a flag for data that match data in the defects array. Data that are flagged are treated as negative values and output as 16-bit, 2's complement binary numbers when read by the READ VER command. As a result, some or all of the bits in the first byte may be ones. Thus the value 255 in the vertical array would be transmitted as:

00000000	(first byte)
11111111	(second byte)

If flagged as a defect, however, the value 255 would be complemented:

11111111	00000000	(1's complement)
	+ 1	
11111111	00000001	(2's complement)

and transmitted as:

11111111	(first byte)
00000001	(second byte)

READ ATC. The READ ATC command outputs a simplified array stored as the result of an ATC operation (see the ATC command). The 512-point array is the averaged value of the waveform with a single value per sampling point. Data values can range from zero to 1023; the data word is sent with the two most significant bits as the two least significant bits in the first byte (unused bits set to zero) and the remaining bits in the second byte. The data values are time-ordered; that is, they are sent in order from left-to-right of trace.

Although the data values range up to 1023, they can be rescaled to values from zero to 511 by assuming a block binary point between bits zero and one.

The ATC and READ ATC commands allow read-out of waveforms in a simpler format for a controller with limited processing capability. The data also requires less storage. For both of these reasons, these commands may be useful for data logging and automatic test applications. The tradeoff is less external processing for simpler, therefore less rigorous, normalizing.

READ SA. The READ SA command outputs a simplified array stored as the result of a DIG SA (digitize and signal-average) operation (see the DIG SA command). The 512-point array is the averaged value of the waveforms that are digitized by the DIG SA operation; the array has a single value for each sampling point. The data values are sent in order from left to right-of-trace.

Because the data are summed (as explained for the DIG SA command), the data can be 10 to 15 bits wide (unused high-order bits are set to zero). The data are not divided by the number of signal averages so no precision is lost. Since the number of averages is always a power of two, a block binary point can be assumed to rescale the data to the range of zero to 511. The location of the binary point is implied by the number of averages called by the last DIG SA command:

Number of Averages	Binary Point located to right of bit
1	0
2	1
4	2
8	3
16	4
32	5
64	6

The DIG SA and READ SA commands provide signal-averaging more quickly than the waveforms could be digitized, read out and averaged externally. Also, internal signal-averaging by the 7912AD removes the load from an external processor, making this level of waveform processing available in a system with a simpler controller and with less data storage than would otherwise be required.

READ EDGE. The READ EDGE command outputs two processed arrays stored as the result of an edge processing operation (see the EDGE command). The two 512-point arrays represent the top and bottom of the trace; the top is sent as a binary block, followed by the binary block for the bottom. Each array has a single value for each sampling point sent in order from left-to-right of trace.

Valid data range from zero to 511, sent in the same format as for the READ VER data. Missing or rejected points are sent as -1 in 2's complement notation (-1 = all ones in both bytes).

The EDGE and READ EDGE commands relieve part of the burden on an external processor when more sophisticated normalizing is needed. The edge data is ready for normalizing or geometry correction, such as that done by TEK SPS BASIC Software routines.

READ DEF. The READ DEF command outputs an array with both horizontal and vertical values to represent defects by their X-Y coordinates on the target. The data may have been loaded in the defects array either by a DIG, DEF or LOAD operation.

Values in the array from 512 to 1023 represent X coordinates on the target where 512 is at the far left of the target and 1023 is at the far right. If bit 10 of the data value is considered to be a horizontal flag, the remaining bits can be interpreted as the X coordinates directly, ranging from zero to 511. This can be done in an external processor by clearing this bit after it is detected. Each X value is followed by one or more Y values to represent where the top or bottom of a defect is located. Y values range from 0 to 511.

The array is ordered in time, left to right, so that horizontal values are transmitted in increasing order. Multiple vertical values for an X location are transmitted in descending order.

LOAD. The LOAD defects command is the only case of waveform data input to the 7912AD. It allows a binary block of data values to be stored in the defects array in the 7912AD data memory. This array identifies known defects on the 7912AD target. The data format is the same as that output by the 7912AD for a READ DEF command. In fact, one use of the LOAD command is to reload a defects array previously digitized by the 7912AD with a DIG DEF operation. This allows the defects array to be saved on an external storage device, since it is lost when the 7912AD power is turned off.

To assure that all data values in the array (and only those values) are loaded, the byte count must be accurate when the 7912AD is set to use the line feed character as a message terminator. As explained under Command Syntax earlier in this section, using a data byte for a terminator, as required by some controllers, can cause confusion. When the ASCII code for a line feed occurs in a binary block, it may be either a data byte or the message terminator. To avoid this confusion, the 7912AD, when set to use line feed as a terminator, uses the byte count to decide when a message is terminated. An incorrect byte count can cause the 7912AD to store either too little or too much data, depending on whether it is too high or too low a value.

To illustrate the two invalid conditions, consider the use of the byte count. This value at the beginning of the LOAD binary block tells the 7912AD to input that number of bytes minus one and store them in the defects array. The byte following this block is then input as the checksum. Therefore: 1) If the byte count is too low, not all bytes are stored and the last one accepted is used as the checksum. 2) If the byte count is too large, the checksum and any format or terminator characters sent are stored as data in the defects array and the instrument either hangs (if further data is not sent) or stores invalid data (if further data is sent before it is unlistened).

With the 7912AD set to observe the EOI line for the message terminator, the invalid conditions described above are avoided; the instrument continues to input data until it receives EOI and interprets the checksum properly.

DUMP RAW. The DUMP RAW command returns the internal Y and X arrays from 7912AD memory without reordering or processing. The contents of four internal registers are included as pointers to interpret the Y and X arrays.

The peculiar format of the Y array results from the way the scan converter is read as described in Section 1. During a digitize operation, values are stored in the 7912AD data memory in order as they are read from top to bottom of the target on each of 512 vertical scans. The scans are made sequentially from left to right of the target. However, the reading beam is asynchronous with the writing beam; data elements detected by the reading beam are stored beginning when the time base sweep is triggered, regardless of the position of the reading beam at that time. For this reason, the Y array may wrap around -- the data may start anywhere within the time window, continue to the end of the window (end of the written trace), then continue from time-zero (left of trace) to the starting point.

The X array is a counter array. Each element is a count of the number of Y elements stored at the corresponding X location on the target. The data in the X array is in order from left to right of trace: the first element in the array is the count of Y data during the left-most vertical scan of the reading beam, the next element is the count from the next vertical scan to the right, and so on.

The binary block format for the DUMP RAW output is:

%<BYTE COUNT><CHZYPTR><FSTYPTR><LSTYPTR><LSTDPTR>
<4096 DATA VALUES><CHECKSUM>;

%, BYTE COUNT, CHECKSUM, and ; are defined above under Block Binary Format.

CHZYPTR is a 16-bit binary word pointing to the first data value stored during the left-most vertical scan of the target.

FSTYPTR is a 16-bit binary word pointing to the first valid word in the Y data array.

LSTYPTR is a 16-bit binary word pointing one past the last valid word in the Y array.

LSTDPTR is a 16-bit binary word pointing one address above the last element in the defects array.

The above-described pointers are sent in two bytes, more significant byte first, right-justified with unused bits set to zero.

The DATA VALUES are consecutive words of data memory beginning with address zero and continuing through 4095. This area of 7912AD memory is 10 bits wide. The memory word is sent in two bytes, more significant byte first, right-justified with unused bits set to zero.

DUMP PR. The DUMP PR command returns the processed data arrays from the 7912AD memory without further processing. Since they are already processed into single-valued, time-ordered functions, no pointers are included. The entire processed data memory area is dumped as a single binary block with 1024 data values.

The arrays dumped are those stored by the last processed data operation. For instance, the EDGE command fills the entire processed memory area, while the ATC command fills only the top half and DIG SA fills only the bottom half. The data memory space is defined under Waveform Storage in Section 3.

Scaling the Output Waveform

The ATC array or normalized EDGE arrays can be scaled using a ground reference and the vertical plug-in scale factor. If the ATC array is used, divide each value by 2 before scaling.

First, acquire the ground reference by digitizing a waveform with the amplifier plug-in input grounded. Normalize the ground waveform with the ATC command, read it out (READ ATC), and divide the ATC waveform by 2. Compute the ground level by taking the average value of a portion of the center of the trace. A TEK SPS BASIC command, ZREF, can be used for this task if the EDGE ground waveform is acquired, rather than the ATC ground waveform.

Second, input the scale factor with the appropriate READ or query command: READ SC1 or VS1? for a single-trace plug-in or channel one of a dual amplifier; use READ SC2 or VS2? for channel 2 of a dual amplifier plug-in. Note: this returns the current scale factor; it is not stored with the waveform.

Then, scale the data, point-by-point, by subtracting the ground reference, multiplying by the scale factor (i.e., the number of volts/division), and dividing by the number of data points per division (512/8):

$$SC = \frac{(VAL - GR) \times SF}{64}$$

where:

SC = Scaled data value

VAL = Normalized data value

GR = Ground reference data value

With TEK SPS BASIC, the NORMAD command can be used to normalize and scale the edge arrays directly. See the TEK SPS BASIC Software manuals for instructions.

Programming Reports

The following programming reports apply to instruments with 6800 MPU release number 1 firmware, which corresponds to the ID query response: ID TEK/7912AD,V77.1,F1.Y; (where Y = 2900 memory controller firmware release number).

NOTE

The following reports are for instruments with Serial Number B049999 and below except for Report No: 5, which is also for Serial Number B050000 and up.

REPORT NO: 1

DESCRIPTION: The digitize defects operation is not completed until a sweep occurs. In single-sweep or normal time base modes, this requires that the triggering conditions (level, slope, etc.) be met. Since the graticule-only mode locks out the sweep, the instrument does not digitize defects at all in this mode. The instrument hangs if it does not complete the number of sweeps specified by the digitize defects command (DIG DEF, <NR1>). However, the device clear (DCL or SDC) interface messages can abort the digitize operation and clear the instrument.

SUGGESTION TO USERS: Set the time base to automatic mode and make sure the instrument is not in the graticule-only mode before sending the digitize defects command. If unsure of the latter, send the GRAT OFF command before the digitize defects command.

If the time base is in normal mode, be sure the triggering conditions (level, slope, etc.) are met. Single-sweep is not recommended.

REPORT NO: 2

DESCRIPTION: If a GRAT ON or GRAT OFF command is executed before a digitize operation has been performed, the instrument hangs. The device clear (DCL) interface message does not clear the instrument.

SUGGESTION TO USERS: Always perform a digitize operation after power-up before using the graticule command: either press DIGITAL on the front panel (in local mode) or send a DIG command such as DIG DAT, DIG GRAT, etc. (in remote mode) before sending GRAT ON or GRAT OFF.

REPORT NO: 3

DESCRIPTION: The instrument does not signal average in the graticule-only mode, since graticule-only locks out the sweep (see Report No.1).

SUGGESTION TO USERS: Make sure the instrument is not in the graticule-only mode before sending the DIG,SA command. If the GRAT ON command was sent earlier, send GRAT OFF before signal-averaging.

REPORT NO: 4

DESCRIPTION: The instrument does not turn off the intensities for sweep rates between 1 millisecond and 200 microseconds, the lower limit for reliably digitizing data in the fast-digitize mode (option 4). One millisecond/division is the minimum sweep rate for the standard instrument and 200 microseconds/division is the minimum sweep rate for option 4.

SUGGESTION TO USERS: Use sweep rates of 200 microseconds/division or faster with an option 4 (fast digitize) instrument.

REPORT NO: 5

DESCRIPTION: Contact bounce in the REMOTE button can cause the 7912AD to report more than one remote request when the button is pressed. As a result, if the remote-request SRQ is enabled (REM ON) the 7912AD may continue to assert SRQ even after the remote-request status is read.

SUGGESTIONS to USERS: Continue to poll the 7912AD until it returns a status byte with bit 7 equal to zero and recognize only the first remote-request status byte received.

REPORT NO: 6

DESCRIPTION: Normally the instrument sends a single byte, FF (hex), with EOI asserted if it is made a talker, but has no data to send. The following case is an exception, however. It arises if the instrument has transmitted all bytes in a message, including the last byte with EOI asserted, so it has no further data to send, but then receives its talk and secondary addresses without first being untalked with the UNT interface message. In this case, the instrument does not respond; it does not send data or assert DAV, but hangs the bus.

SUGGESTION TO USERS: Always untalk the instrument after reading data. Do not send the instrument's MTA and MSA after a data transfer without first sending UNT. Of course, if the data transfer was interrupted, send DCL or SDC after untalking the instrument.

REPORT NO: 7

DESCRIPTION: When the 7912AD is addressed as a talker but has nothing to say, it transmits the data byte FF (hex) while asserting EOI. However, if the instrument is untalked before this data byte is handshaked, it asserts EOI with any bytes output by the 2900 memory controller if the instrument is later made a talker. This affects all bytes output in response to the READ, DUMP, and REP commands except READ SC1 and READ SC2.

The instrument can become a talker with nothing to say if:

1) No output command (READ, DUMP, REP, or a query) or SPE interface command is sent preceding the instrument's talk and secondary addresses.

2) Instrument output is interrupted by a DCL interface message, but the instrument is not untalked.

SUGGESTION TO USERS: Protect against the above cases by:

1) Always handshake at least one byte after making the 7912AD a talker.

2) If interrupting 7912AD data output, transmit the UNT interface message before sending DCL.

REPORT NO: 8

DESCRIPTION: When instructed to go to local, programmable plug-ins do so, even if the 7912AD waits to go to local because the 6800 MPU is busy executing a command (such as READ), or the 2900 memory controller is performing a digitize. This can occur whether the LOCAL button is pressed in remote state, the controller sends the GTL interface message, or the REN line goes false.

SUGGESTION TO USERS: Wait until the 7912AD finished executing all commands and performing any digitize operation before sending GTL or unasserting REN. If unsure of the 7912AD's status, either check it or clear it:

1) To check the 7912AD status, poll the instrument and check for the busy flag (bit 5) in the status byte. If a digitize command was sent earlier, check for operation complete status as well. The status byte for not busy and operation complete is: 0x000010. Remember, however, operation complete status could have been cancelled by a previous poll or a device clear that followed the last digitize operation.

2) To override the 7912AD's current status, send the SDC interface message after addressing the 7912AD with both MLA and MSA. This halts any memory controller operation, clears the input buffer (stopping execution of any commands by the 6800 MPU), and resets the status byte. The DCL interface message accomplishes the same thing and does not require that the 7912AD be addressed, but it also resets the programmable plug-ins to power-up status. This may change scale factors, trigger mode, etc.

General Programming and Operating Information

1. The 7912AD accepts both lower-case and upper-case characters in all commands. If lower-case characters are used, the instrument executes the commands as if they were in upper case.

2. The 7912AD has a built-in timeout on the main and graticule intensities. When the instrument is in repetitive sweep mode, the intensities will timeout in approximately five minutes. TIMEOUT OCCURRED message will appear on the TV monitor.

Activating any mainframe pushbutton (except LOCKOUT), or TV SCALE FACTOR on-off switch or receiving a message over GPIB will reset the intensities.

3. When the 7912AD is in TV mode and the REMOTE button pushed, the mainframe primary and secondary GPIB addresses will be displayed on the TV monitor as:

PA XX SA YY

where XX is the mainframe primary address and YY is the mainframe secondary address, the address readout replaces the normal readout on the TV monitor for about five seconds.

4. In case of power-up error, the TV monitor will display the cause and location of the error, such as:

```
RAM  R/W  ERROR
ADDRESS   XXXX
```

where XXXX is the address of byte where error occurred

```
CHECKSUM  ERROR
ADDRESS   YYYY
```

where YYYY is the address of the ROM with bad checksum

```
ROM ADDR  ERROR
ADDRESS   ZZZZ
```

where ZZZZ is the address of the misplaced ROM.

SECTION 3

BLOCK DIAGRAM AND CIRCUIT DESCRIPTION

The 7912AD block diagram (Fig. 3-1) indicates signal and data flow in the instrument. It also relates the scan converter to the other analog circuitry and the two microprocessor systems. The scan converter is shown in two pieces, the writing gun on the left-hand portion of the figure and the reading gun on the right-hand portion.

Power Supply. The Power Supply provides regulated voltages for the analog and digital circuitry as well as the plug-ins. It also supplies the drive to the writing gun high-voltage section. In addition to the ON/OFF switch, it can be turned on and off through the ACTUATE connector. The ENABLE output can, in turn, control another instrument's ACTUATE input.

Analog Signal Flow. Input signals to drive the writing gun come from either the amplifier (vertical) and time base (horizontal) plug-ins or from the Graticule Generator. The Plug-In Interface switches in the Graticule Generator as the signal source for a short period of time following each sweep from the plug-ins to write a dot matrix on the target. This provides a frame of reference for the waveform.

The Vertical and Horizontal Amplifiers are driven by the outputs from the Plug-In Interface and, in turn, drive the vertical and horizontal deflection plates in the writing gun. The vertical signal is delayed so the leading edge of a fast pulse can be written on the target without a pretrigger. The delay allows time for triggering on the input signal and for the time base sweep to begin before the input signal reaches the vertical deflection plates. These plates are actually helical delay lines designed for high-frequency response. The deflecting field appears in the gap between the helices.

Separate intensity lines from the Plug-In Interface and from the Graticule Generator control the writing gun Z-axis. Two lines are needed because the writing gun intensity must be controlled independently during the times it writes the graticule and the waveform. The intensity control signals come from the Translator rather than from the front panel (as discussed below).

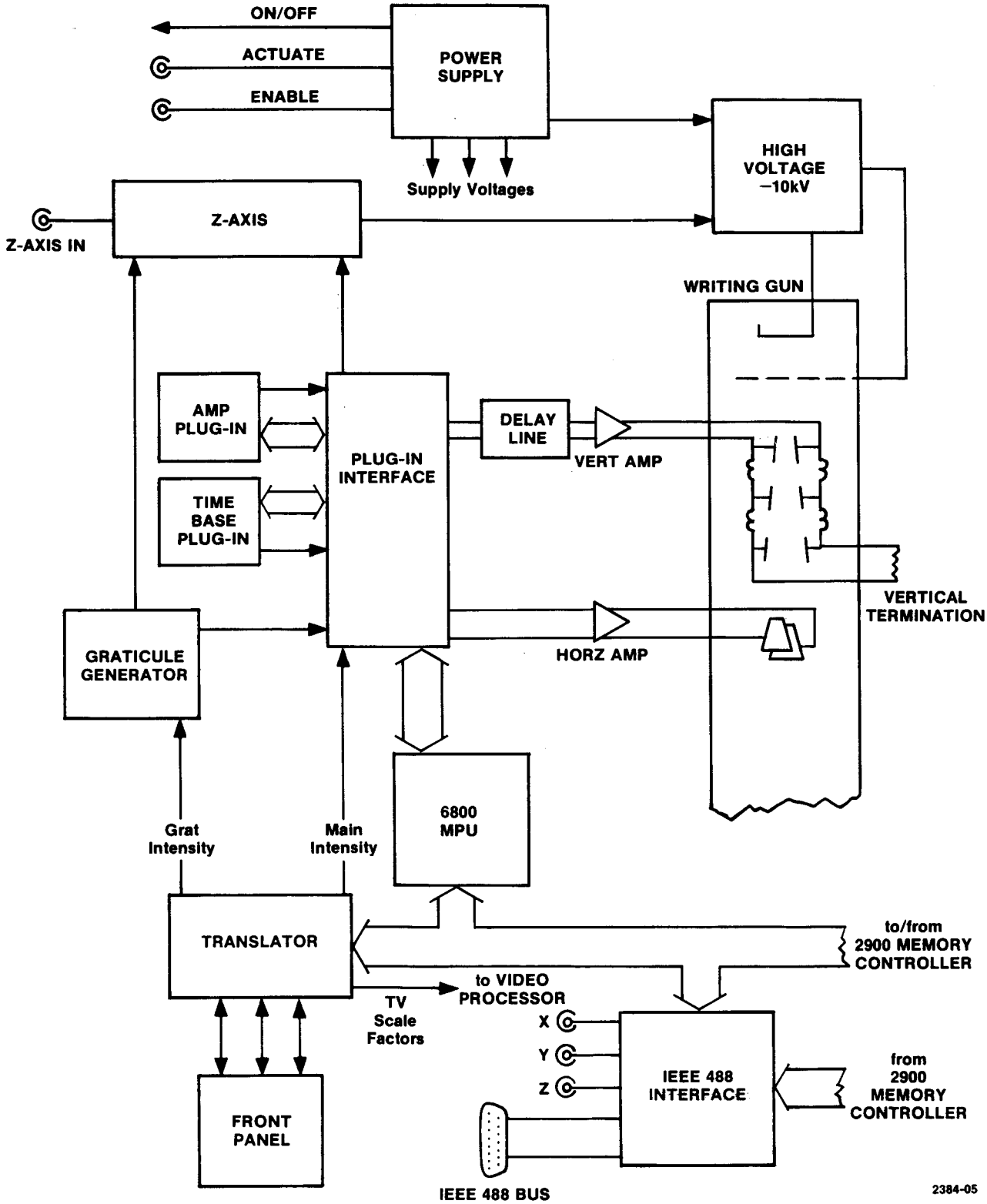
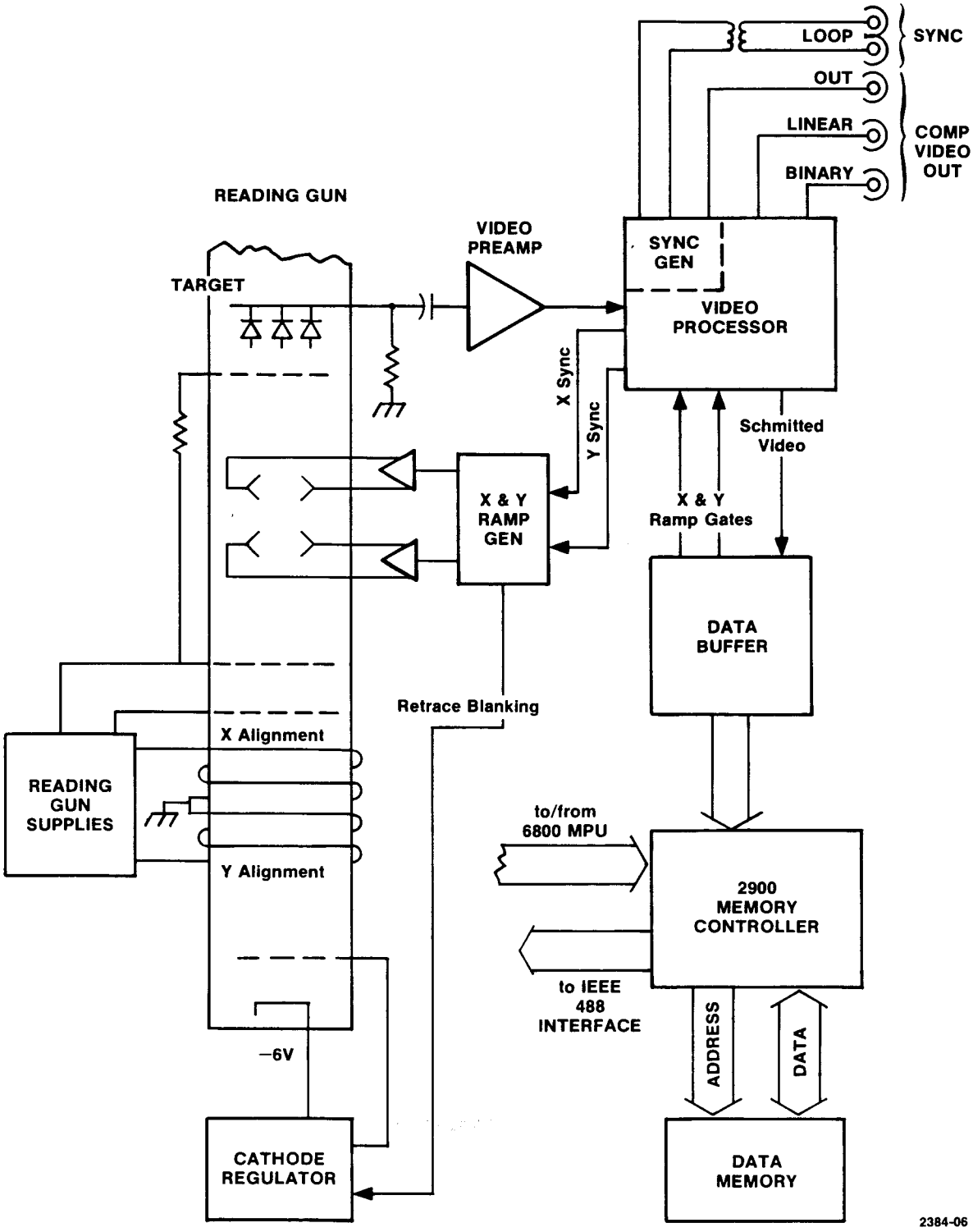


Fig. 3-1. A block drawing of the 7912AD with plug-ins showing the



relationship between the analog and microprocessor systems.

The Z-axis drive goes to the high-voltage assembly to be translated to the very high negative voltage necessary on the writing gun grid. The writing gun is operated at a very high negative potential so the target and deflection amplifiers can be near ground potential. The monoaccelerator (single accelerating potential) design holds spot size of the writing beam to a minimum (0.001 inch).

When read from the target, the waveform and/or graticule is preamplified and then output as composite video for display or passed on to the Data Buffer. The clock that controls reading the target originates in the Data Buffer. X and Y ramp gates derived from the clock are used by the Video Processor to generate sync pulses for the X and Y Ramp Generators in digital mode. In TV mode, a sync generator controls the ramp gate signals; it can be locked to an external signal applied to the LOOP input.

The X and Y Ramp Generators drive the reading gun deflection plates (through amplifiers) and send a signal to the Cathode Regulator to blank the reading beam during retrace. The deflection plates are part of the deflectron shown in Setion 1 as is the magnetic yoke for focusing and aligning the beam. Accelerating voltages provided by the Reading Gun Supplies are much lower for the low-velocity reading gun than those required for the writing gun.

Data Flow. In digital mode, data values are recovered by the Data Buffer. A Y counter keeps track of the vertical position of the reading beam as it scans the target. When the beam crosses the edge of a written portion of the target, the Schmitted video signal changes state. The transition causes the Data Buffer to latch the contents of the Y counter as a data point. Although the 2900 Memory Controller is fast, it could not keep up with the data without buffering. So all points detected during a single scan are stored temporarily in a high-speed cache memory to reduce the data rate out of the Data Buffer.

The 2900 stores the Y data from the cache memory along with the number of points stored for each vertical scan in the Data Memory. Once stored, the waveform data can be processed by the Memory Controller (averaged, for example). The processed data is also stored in the Data Memory.

The Data Memory can be read out over the IEEE 488 bus. The 2900 controls a high-speed data bus going to the IEEE 488 Interface to enable fast data transfers over the bus. The data can also be converted to XYZ outputs for a refreshed display on a monitor.

@

Instrument Control. The 7912AD firmware operating system runs on the 6800 Microprocessor (MPU). It controls instrument status and command input/output through either the front panel or the IEEE 488 Interface.

Front-panel controls for programmable functions do not set operating parameters directly. For instance, the intensity levels are controlled by lines from the translator labeled Grat Intensity and Main Intensity in Fig. 3-1. These control signals are set by the 6800 MPU through Digital-to-Analog (D/A) converters in the translator.

In remote mode, the 6800 sets the levels according to values programmed over the IEEE 488 bus. In local mode, the 6800 compares the intensity levels to levels selected through the front panel controls and adjusts the D/A outputs to match the front panel controls. Whether in local or remote mode, the 6800 monitors the writing beam duty cycle and automatically limits the intensity, if necessary, to prevent damage to the target.

Scale factors are also handled by the 6800, whether in TV or digital mode. The 6800 reads the scale factors from the plug-ins through the plug-in interface. In TV mode, it outputs the scale factors through a character generator on the Translator as video to the video processor. There the scale factor video is added to the composite video display. The 6800 reads out the scale factors on request over the IEEE 488 bus.

The 6800 MPU performs several other tasks. It acts as a transparent interface for programmable plug-ins; command I/O for the plug-ins passes through the MPU onto a bus between the MPU and plug-in interface. This path continues via the bus shown in Fig. 3-1 going to each plug-in. The 6800 also initiates data storage or processing by the Memory Controller in response to commands over the IEEE 488 bus (remote mode) or data storage when the front panel DIGITAL button is pressed (local mode).

Waveform Storage

The 7912AD waveform Data Memory is divided between a raw data area of 10-bit words and a processed data area of 16-bit words as shown in Fig. 3-2. The memory is semiconductor, so data is retained only while power remains on.

Raw Arrays. Vertical data values are stored in the vertical array during a digitize operation. The values include all points detected on the target, whether the edge of a waveform trace, graticule dot, or a defect. Since the reading beam scans the target continuously and is not

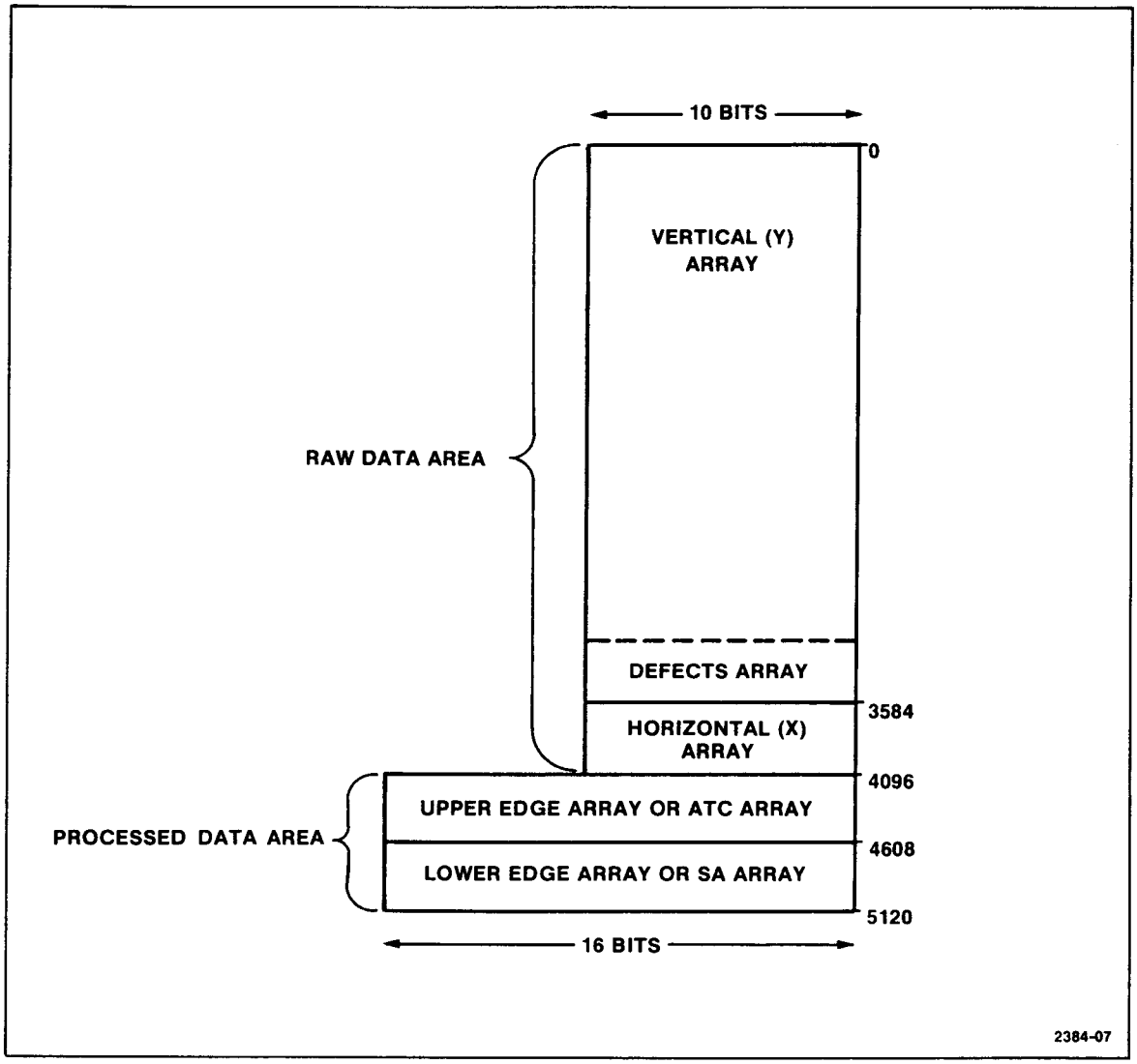


Fig. 3-2. 7912AD data memory map showing arrays used for raw and processed waveforms.

synchronized with the writing beam, it may be anywhere on the target when the 7912AD begins storing data. The data are stored starting at the top of the raw vertical array and are stored continuously until the reading beam returns to where storage began. Data are stored in the order they are detected from top to bottom of each of the 512 vertical scans of the target moving from left to right.

Because of the way data are stored, the raw vertical array may wrap around. That is, the data may start anywhere within the time window (where the target represents a time frame), continue in order to the end of the window, but then return to the beginning and continue until reaching the starting point. This is corrected by internal data

processing so the data is output by the READ commands from left to right of trace. It is not corrected, however, if the raw area of the memory is DUMPed, as noted in Section 2.

The 7912AD keeps track of the number of vertical data values stored during each vertical scan (that is, for each horizontal location of the target) in an X (horizontal) counter array. The counts are stored so that the first X array location contains the number of data values stored during the left-most vertical scan, the next address contains the number of values for the next vertical scan to the right, and so on. When output by the READ command, this array is converted to a pointers array to be used to interpret the vertical array.

A defects array located just above the pointers array can identify target defects (points detected as data whether written or not). Defects are stored in reverse order, that is, the first defect value is written at the highest address in the array and the array is written upward. Values in the defects array between 512 and 1023 are horizontal locations on the target where 512 is the left-most vertical scan and 1023 is the right-most vertical scan. Each horizontal value is followed by values between 0 and 511 to represent defects at that horizontal position on the target.

Using the standard 7912AD's defects capability, vertical raw data that matches data in the defect array can be flagged by setting bit 10 of the word. Further internal processing can reject the defects.

Processed Array. The processed data area does double duty. It can be used either as a single 1K block for the two edge arrays, or split into two 512-word blocks for the average-to-center (ATC) array and the signal-averaged (SA) array. In either case, the arrays are single-valued functions processed by the memory controller. Each array contains 512 points, reordered so they represent the function from left to right of trace. The edge arrays define the top and bottom of the trace. The ATC array is the average of the top and bottom of the trace. The signal-averaged array is the average of a number of ATC arrays from a repetitive waveform.

Because they share the same memory space, it is not possible to store all four processed arrays at one time. Either the edge arrays or the average-to-center and signal-averaged arrays can exist at any time.

Writing System

The writing system in the 7912AD acquires the analog signals from the plug-ins, conditions these signals, and writes the waveform on the scan converter target. It also generates the electronic graticule and writes it on the target on a time-share basis with the input waveform. Five main parts comprise the writing section of the instrument: The Plug-In Interface, Graticule Generator, Vertical Amplifier, Horizontal Amplifier and the Z-Axis/High Voltage circuits.

Plug-In Interface

The Plug-In Interface board (A46) carries two edge connectors - one for the vertical plug-in and one for the horizontal plug-in, as well as circuitry for interfacing the two plug-ins. All communication between the instrument and plug-ins occurs via the Plug-In Interface. Diagrams 2 and 3 represent the Plug-In Interface.

NOTE

For instruments with Serial Number B100837 and up, see diagram 2 (SN B100837 & Up) and diagram 3 (SN B100837 & Up) in VOL II, for revised circuit number designations.

Trigger Buffer. The Trigger Buffer takes the trigger signal from the vertical plug-in and applies it to the internal inputs of the time base plug-in. This buffer isolates the horizontal plug-in from the vertical signal path.

The circuit consists mainly of a special high-frequency integrated circuit, U422, shown in the top-center of diagram 2. This I.C. receives the differential trigger signal from the vertical plug-in and provides isolation between the plug-ins. The output of U422 drives a differential amplifier formed by Q422 and Q428. R414 provides for DC centering of the trigger signal. The differential output is applied to the horizontal plug-in through J626. The overall gain of the Trigger Buffer is within 15% of unity.

Vertical Chop. The Vertical Chop circuitry, shown in the lower-left corner of diagram 2, provides the chop signal to drive a dual-channel vertical plug-in. The heart of the circuit is U126, which includes a clock generator and chop blanking logic. The clock generator produces a 2 megahertz clock signal to drive the chop circuit and the chop blanking logic. If a dual-channel plug-in is installed and set to chop mode, pin 5 of U126 is held low (0 volts). In this mode, the 2 megahertz clock is applied to pin 15 and the D flip-flop, U228B. This flip-flop divides the clock signal by two, producing a 1 megahertz output. Q228 shifts the output level of the flip-flop to drive the emitter follower, Q326. The output of Q326 drives the chop input of the vertical plug-in.

Alternate Drive. If the vertical plug-in is set for alternate mode, the holdoff signal from the horizontal plug-in is used to produce a switching signal (ALTERNATE DRIVE) for the vertical plug-in. The holdoff signal comes from pin B4 of J626 and is applied to the clock input of U228A. U228A divides the holdoff signal frequency by two. The Q output of U228 is level shifted by Q236 to drive the emitter follower state, Q238. The resulting signal is applied to the plug-in connectors, J626 and J926.

Notice that the preset and clear inputs of the flip-flop are connected to ALT OVERRIDE and $\overline{\text{ALT OVERRIDE}}$, respectively. These lines are unused in the 7912AD, but could be used to control dual-channel plug-ins. If the plug-in is set to ALTERNATE mode, these lines allow a remote controller to override the alternate drive signal and select channel 1 or channel 2.

NOTE

For instruments with Serial Number B100837 and up, the immediately previous and immediately following paragraphs are no longer valid. See diagram 2 (SN B100837 & Up) in Vol II, for changes.

Holdoff. The holdoff signal also drives inverter Q538. The output of this inverter is unused.

Sweep Gate. The horizontal plug-in asserts the sweep gate line (pin A1 of J626) when a sweep is in progress. This pulse drives the +GATE buffer amplifier, the Z-Axis logic, and inverter Q546. The sweep gate signal from Q546 goes to the Graticule Generator, Translater, and Data Buffer board.

The +GATE OUT signal available on the 7912AD rear-panel is provided by the circuit shown in the upper-right corner of diagram 2. The sweep gate signal is coupled to a comparator formed by Q138 and Q136. C136 provides regenerative feed-forward to sharpen the leading edge of the +GATE pulse. The output of the comparator drives common-base amplifier Q036 through ferrite-bead inductor E036. CR024 and CR022 protect the driver transistor from voltages applied to the +GATE OUT connector.

Z-Axis Logic. The Z-Axis Logic, shown in the bottom-right of diagram 2, generates the Z-axis control current to set the main intensity. U128 accepts a variety of input signals and generates a variable current (0-4 milliamps) at pin 8 based on these input signals. The main intensity level is fed to pin 16 through R137. This control adjusts the Z-Axis drive to assure proper unblanking when the 6800 microprocessor is

limiting main intensity at low sweep speeds. How the 6800 controls the main intensity level for different sweep speeds and trigger rates is discussed in the Translator description. The level on pin 7 is determined by signals from several sources, including the BEAM FINDER switch, a signal from the horizontal plug-in (to reduce intensity at sweep speeds below 0.1 seconds/division), and the Z-axis inhibit line from the graticule generator. Pin 9 of U128 accepts input from either the rear-panel Z-AXIS INPUT or from the plug-ins (e.g. intensified sweep operation with a 7B92A plug-in). CR136 and CR138 protect U128 from excessive drive applied to the Z-AXIS INPUT connector. The 2 megahertz vertical chop blanking signal from U126 is fed to pin 6. Pin 14 accepts sweep gate signals from the horizontal plug-in to control retrace blanking.

Single Sweep. The SS MODE (Single Sweep Mode), $\overline{\text{ARM SS}}$, and SS ARMED lines (top-right of diagram 2) provide for remote control of the single sweep functions in the time base. SS MODE is asserted when the single-sweep mode has been selected. The 6800 uses the SS MODE and SS ARMED lines to determine if conditions are correct to execute a DIG SSW command. SS ARMED is asserted when the time base single sweep function is armed and ready to accept a trigger. The 6800 asserts $\overline{\text{ARM SS}}$ to arm the single sweep function.

Readout/7K Acquisition. Diagram 3 shows the other half of the plug-in interface. This circuitry acquires the readout information from the plug-ins and carries the 7K bus from programmable plug-ins to the 7K interface. The 7K bus is described in more detail in the 6800 microprocessor system description.

Graticule Generator

Introduction. The Graticule Generator produces a 9 X 11 array of dots that are written on the scan converter target. The dot array simulates the familiar graticule of a standard oscilloscope. The full graticule consists of eight major vertical divisions and ten major horizontal divisions in TV mode. Four minor division marks are also provided at 0.2 division spacing between each major division. This electronic graticule provides a stable visual reference for waveforms displayed on the TV monitor.

The graticule can also be digitized with or without waveform data. The quantity of data produced by digitizing a full graticule can rapidly overflow the data memory, so in digital mode, only the major divisions are marked by dots.

Since the signal paths for the input and graticule signals are identical, any minor non-linearity or distortion in the signal path affects both the waveform and graticule data equally. A computer can compare the digitized graticule to an ideal graticule and correct for these minor distortions, resulting in more accurate data.

Overview. The graticule generator circuit is shown on diagram 4. The graticule is written on the scan converter target on an alternate-sweep time-shared basis with the waveform data. At sweep speeds of 5 microseconds/division or slower, the graticule is written after each time base sweep. When SWP GATE goes high at the end of the sweep, the graticule generator asserts SWEEP LOCKOUT, preventing the time base from initiating another sweep. Then the generator sets the vertical and horizontal channel switches to ignore the plug-in signals and accept the graticule ramps.

For sweep speeds faster than 5 microseconds/division, the graticule generator does not lockout the time base, but it sets the channel switches to ignore time base sweeps. The time base continues to produce sweep ramps, but they are ignored by the mainframe. This prevents instability in the time base caused by disabling the sweep for long periods of time in relation to the sweep speed. The process of generating the graticule is identical regardless of sweep speed.

The graticule is generated by sweeping the writing beam vertically across the target, starting in the lower-left corner. If a major division line is being produced in TV mode, dots are written every 0.2 division - for a total of 41 dots. If a minor division is being written, 9 dots are produced--one at each major division line. In digital mode, dots are produced only at the major vertices.

At the end of each vertical sweep, the horizontal ramp generator steps the writing beam to the right by one minor division increment. Then the beam makes another vertical sweep generating the dots for that row. This process is repeated until the entire graticule is written. Then the graticule generator resets the channel switches to accept plug-in signals and allows the sweep to begin again.

Vertical Ramp Clock. The Vertical Ramp Clock, derived from the 80 megahertz master clock on the Data Buffer board, provides the reference for the Vertical Ramp Generator. The master clock signal is divided down to 5 megahertz on the Data Buffer board (A20). The 5 megahertz clock is fed to U340 in the upper-left corner of diagram 4. U340 divides the clock by eight. The resulting 625 kilohertz signal is further divided by U130 and U140 to produce a 13.89 kilohertz signal. This signal fires one-shot U110.

The output of this one-shot provides a reference timing pulse to stabilize the Vertical Ramp Generator. U450 compares the phase of the one-shot pulse to the retrace pulse from the Vertical Ramp Generator and provides a correction current to the ramp generator.

Vertical Ramp Generator. The Vertical Ramp Generator provides the ramp that sweeps the writing beam vertically over the target to generate the graticule dots. Fig. 3-3 shows a block diagram of the Vertical Ramp Generator.

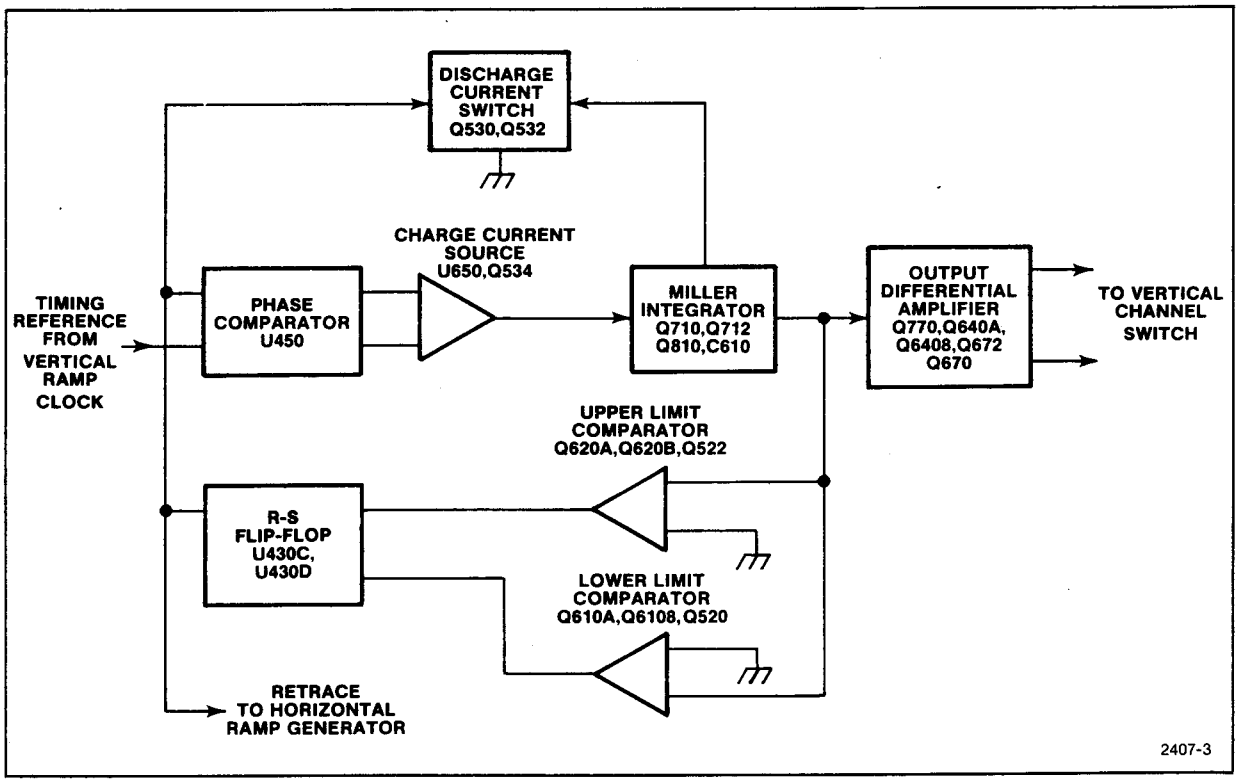


Fig. 3-3. Block diagram of the graticule vertical ramp generator.

The heart of the circuit is a Miller Integrator with C610 (near the center of diagram 4) as the integrator capacitor. Current through Q534 charges C610 to produce a linear ramp voltage at the collector of Q712. The ramp voltage is monitored by two comparators - the upper and lower limit comparators. When the ramp voltage reaches its upper limit, the comparator formed by Q620A and Q620B switches and Q522 turns off for a short time (determined by C522 and R528 on its emitter). This provides a negative-going pulse to the R-S flip-flop formed by U430C and D. The flip-flop resets and pin 11 of U430D goes high. The high on this output is applied to the base of Q532 and to the phase detector for comparison with the vertical ramp clock. Q532 turns off, turning Q530 on. This

provides a discharge path for the integrator capacitor, C610. C610 discharges very quickly and the ramp drops to near zero volts.

When the ramp reaches zero volts, the lower limit comparator (Q610A and Q610B) switches, providing a pulse to set the R-S flip-flop. When the flip-flop sets, Q532 turns on and Q530 turns off. Current through Q534 begins to charge C610 again.

Recall that the output of the R-S flip-flop was fed to the phase comparator, U450. If the slope of the ramp vaies, the retrace pulse from the R-S flip flop and the vertical ramp clock pulse will not arrive at the same time. To correct the slope, U450 detects the time difference between the pulses and generates output pulses of a period proportional to the time difference. These pulses are integrated by U650 to produce a correction current that is applied to the ramp generator.

If the ramp reaches the upper limit point at exactly the right moment, the pulse from the flip-flop and the vertical ramp clock pulse will arrive at the same time. In this condition, the outputs of U450 stay in their cleared state: pin 10 low and pin 2 high. CR552 and CR550 are reverse-biased and the voltage at the junction of CR556 and CR554 is simply the result of the voltage divider formed by the two diodes with R544 and R550. U650 compares this voltage to a reference level and provides base drive current to Q534.

If the ramp rises too quickly, the upper limit comparator resets the R-S flip-flop before the vertical ramp clock pulse occurs. The rising edge on U430D's output clocks pin 10 of U450 high. It stays high until the vertical ramp clock pulse arrives. The high on pin 10 forward biases CR552, while CR550 is reverse biased. This pulls the inverting (-) input of U650 high and U650's output swings negative. C640 begins to discharge through R640 and the drive current for Q534 decreases. As a result, the ramp charge current decreases and the slope decreases, restoring syncroniztion. When the vertical ramp clock pulse arrives, pin 10 of U450 returns to its low state and both CR552 and CR550 are reverse biased.

If the ramp is too slow, the polarity of the correction current reverses because the vertical ramp clock pulse arrives first, setting pin 2 of U650 low. This forward biases CR550 and pulls the inverting input of U650 low. C640 charges in the positive direction and the drive current to Q534 increases, providing more charge current to the ramp generator to increase its slope. The magnitude of the correction current is proportional to the amount of time between the vertical ramp clock pulse and the vertical retrace pulse.

The ramp output signal, taken from the collector of Q712, is applied to a paraphase amplifier composed of Q640A, Q640B, and current source Q770. R950 sets the gain of the amplifier while R850 sets the DC level to adjust overall vertical position of the graticule. Nominal output corresponds to 50 millivolts/division of deflection (the same as the plug-in output).

Horizontal Ramp Generator. The Horizontal Ramp Generator provides a staircase ramp that deflects the writing beam horizontally. Fig 3-4 shows a simplified schematic diagram of the horizontal ramp generator.

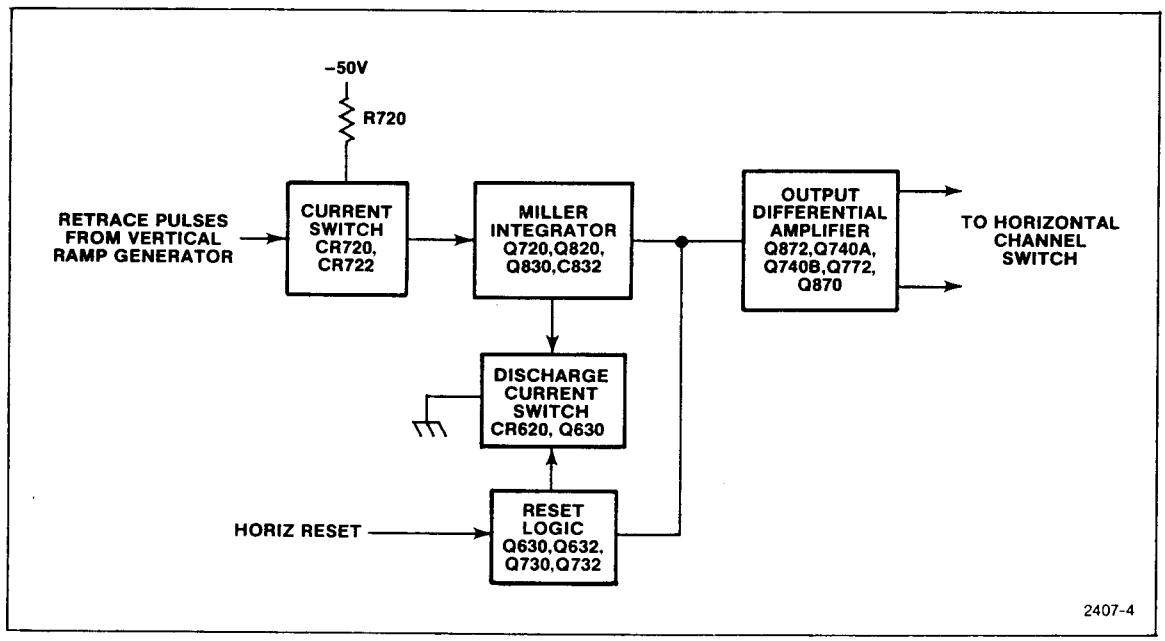


Fig. 3-4. Block diagram of the graticule horizontal ramp generator.

The horizontal ramp generator also uses a Miller Integrator. C832 (bottom-center of diagram 4) is the integrator capacitor. The horizontal ramp holds a constant level while the vertical ramp is running. During the vertical retrace, the horizontal ramp rises, moving the beam over to the next column of dots. The high-impedance of the FET input circuit (Q720) provides the necessary stability for the hold period.

Horizontal ramp timing is derived from the vertical ramp retrace signal. When the vertical retrace flip-flop (U430C and D) is reset at the peak of the vertical ramp, the output of U430C goes low. The low level pulls down the voltage divider formed by R726, R724, and R722 causing the anode of CR722 to go to about -0.6 volts. CR722 turns off and CR720 turns on. Charge current for the integrator flows through R720 and CR720. The horizontal ramp begins to rise and the writing beam moves over to its next position.

When the vertical retrace period ends, the R-S flip-flop is set and U430C's output goes high. The output of the voltage divider rises and CR722 begins to conduct, reverse-biasing CR720. The charge current for C832 is blocked, and since the diodes and Q720 conduct very little leakage current, the ramp voltage remains stable until the next vertical retrace period. Because the amplitude of the steps depend on the vertical retrace time, the ramp amplitude depends on R540. This adjustment is set in the Calibration Procedure for 5 volts of horizontal ramp amplitude.

The horizontal ramp reaches its peak voltge in a discrete number of steps. U220 counts the steps and generates a horizontal reset pulse when the proper number of steps have occured. The horizontal reset signal ($\overline{\text{HORIZ RESET}}$) drives the base of Q630 (bottom-left corner of diagram 4).

When the horizontal ramp is running, $\overline{\text{HORIZ RESET}}$ is high and Q630 is on. As the ramp voltage rises, the voltage on the emitter of Q730 rises as well. This voltage causes Q732 to begin to turn off and its collector voltage swings negative, turning Q632 off. The collector voltage of Q632 cannot rise because Q630 is on, holding the top of R730 near ground. When $\overline{\text{HORIZ RESET}}$ goes low, Q630 turns off. Since the horizontal ramp is near its maximum (5 volts) when $\overline{\text{HORIZ RESET}}$ occurs, Q632 is off as just discussed. The voltage on the collector of Q630 and the anode of CR620 rises. CR620 becomes forward-biased, discharging integrator capacitor C832. The ramp drops very quickly to zero volts and Q732 and Q632 turn on, reverse-biasing CR620 and preventing the discharge current from charging C832 in the negative direction. C832 begins to charge again, but the ramp voltage rises only a few millivolts before Q632 turns off. At this point the ramp generator is ready to start the next cycle. $\overline{\text{HORIZ RESET}}$ stays low, disabling the Horizontal Ramp Generator until the next graticule cycle begins.

The horizontal ramp at the emitter of Q830 drives a paraphase amplifier that is functionally identical to the Vertical Ramp Generator output stage.

Graticule Startup Logic. The Graticule Generator is enabled by the rising edge of $\overline{\text{SWP GATE}}$ or the GRAT ONLY signal. The startup logic is shown at the left-center of diagram 4. Figure 3-5 shows the Graticule Generator timing. Refer to this figure for the following discussion.

When the instrument is in normal operation (graticule only mode off),the graticule is generated only when the time base sweep has been triggered. When the sweep begins, $\overline{\text{SWP GATE}}$ goes low. U080A inverts the signal and the rising edge fires one-shot U170B. If the sweep speed is set for 5 microseconds/division or slower, U170B times out before $\overline{\text{SWP GATE}}$ goes high at the end of the sweep. When U170B times out, its Q output goes low and the positive transition on $\overline{\text{SWP GATE}}$ clocks the $\overline{Q}$ output of U330B high. The high on this output enables U440A to assert SWP LOCKOUT through U440B and Q460, inhibiting sweeps while the graticule generator is running.

If the sweep speed is set faster than 5 microseconds/division, the time base is allowed to run during the graticule period even though the channel switches are set to ignore time base sweeps. In this condition, U170B does not time-out before the end of $\overline{\text{SWP GATE}}$. The positive transition on $\overline{\text{SWP GATE}}$ clocks the $\overline{Q}$ output of U330B low. The low on this output forces U440A's output to go high, releasing SWP LOCKOUT. This allows the time base sweep to run to improve time base stability.

At the end of $\overline{\text{SWP GATE}}$, the negative transition on the output of U080A also clocks U210B and its $\overline{Q}$ output, pin 8, goes low. This causes the output of U070B to go high which, in turn, clears U210B through U080B. The result is a short positive-going pulse at the output of U070B. This pulse is inverted and narrowed by the edge detector formed by U430B and U420C. The narrow negative-going output pulse sets the R-S flip-flop formed by U420A and B, starting the Graticule Generator.

If the instrument is in graticule only mode, the Graticule Generator does not wait for the end of a sweep. In this mode GRAT ONLY is high, holding flip-flops U330A and B (near the center of the diagram) cleared and asserting SWP LOCKOUT, $\overline{\text{Z-AXIS INHIBIT}}$ and MF CHAN SWITCH. The high on GRAT ONLY also sets the graticule start flip-flop (U420A and B) through U070C, U070B and U420B.

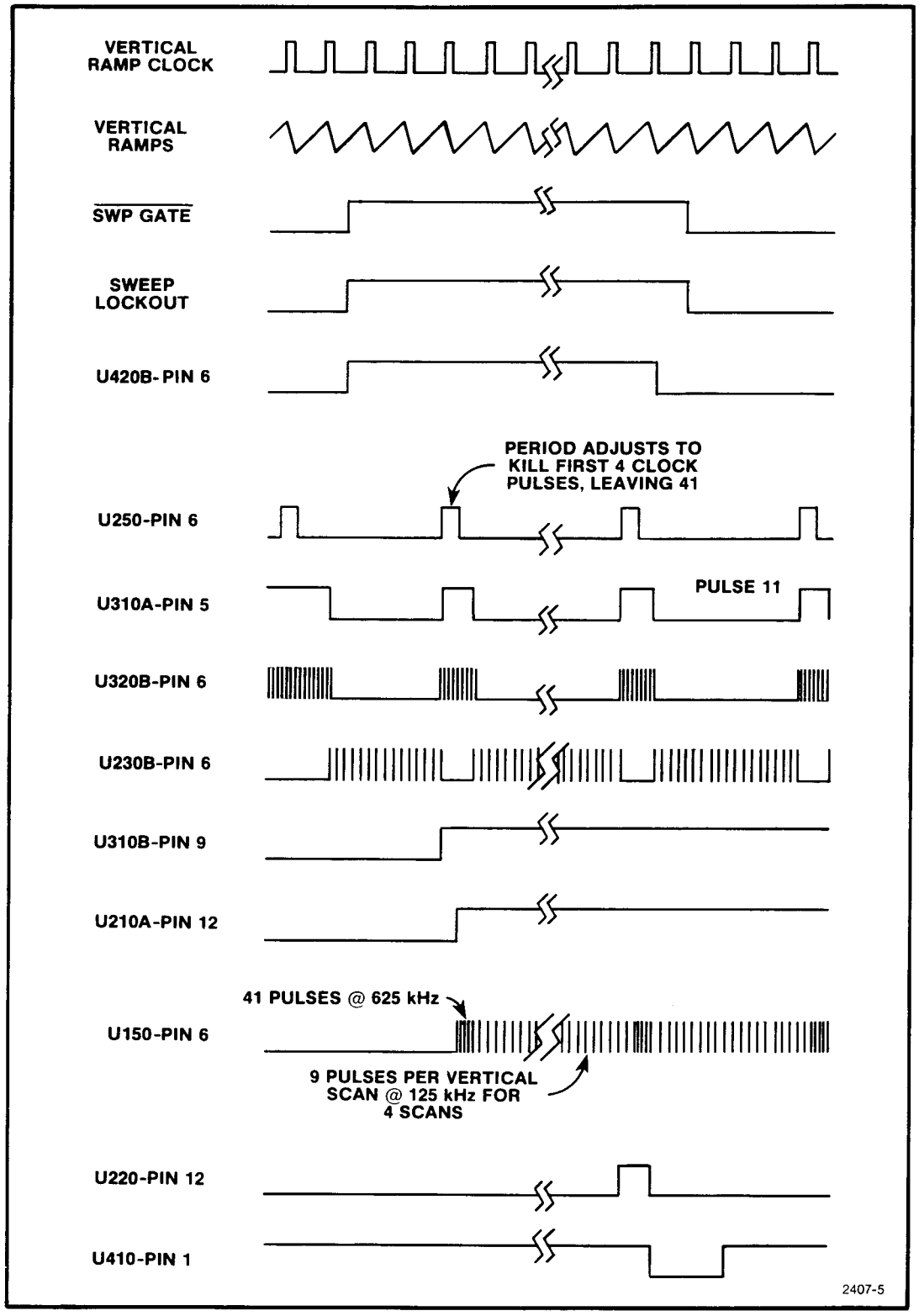


Fig. 3-5. Graticule generator timing in TV mode for sweep speeds ≤ 5 microseconds/division.

When the graticule start flip-flop (U420A and B) is set, U420A's output goes low. The output of U420D (just below the graticule start flip-flop) goes high, which places a high on the D input of U330A and releases the set input of U310A. The low on the output of U420A also goes to pin 11 of U440C. The output of U440C goes high, asserting $\overline{\text{Z-AXIS INHIBIT}}$ and SWP LOCKOUT (if the sweep speed is set for 5 microseconds/division or slower).

The high on U440C's output also disables U080D through U080C, releasing $\overline{\text{SGE}}$ (Sweep Gate Enable). This signal is essentially the same as $\overline{\text{SWP GATE}}$ except that the graticule generation time is subtracted from it. The resulting signal is used to determine the duty factor of the main sweep. Since the Graticule Generator's duty factor is constant, it is not included in the measurement.

If P040 is set to its test position, the GATE inputs of U130 and U140 are tied high, allowing the Graticule Generator to free-run for servicing.

Generating a Graticule. As the writing beam is swept vertically, an entire line of graticule dots must be produced, corresponding to one vertical ramp clock cycle. If a major division line is being generated in TV mode, 41 dots are required. If a minor divison line is being generated (or a major line in digital mode), only nine dots are needed. Figure 3-6 describes the operation in TV mode.

Each falling edge of the clock signal from U140 (top-left) fires the vertical ramp clock one-shot, U110. Its Q output goes high and the edge detector formed by U350A and B produces a negative-going pulse at its output. This occurs with each vertical ramp clock pulse, but the D input of U310A is tied to the output of one-shot U250. This one-shot is driven by divide-by-five counter U240 and it fires on every fifth vertical ramp clock pulse.

Remember that when the startup flip-flop was set, the set input of U310A was released. The Q output of U310A remains high and the Q output of U310B remains low until the logic is ready to start a major division line (every fifth clock pulse). Then U250 is fired, setting the D input of U310A high, and the next vertical ramp clock sets the flip-flop. The rising edge on its Q output clocks U310B and its Q output goes high, setting the J input of flip-flop U210A high, releasing $\overline{\text{HORIZ RESET}}$, and allowing the horizontal ramp to start.

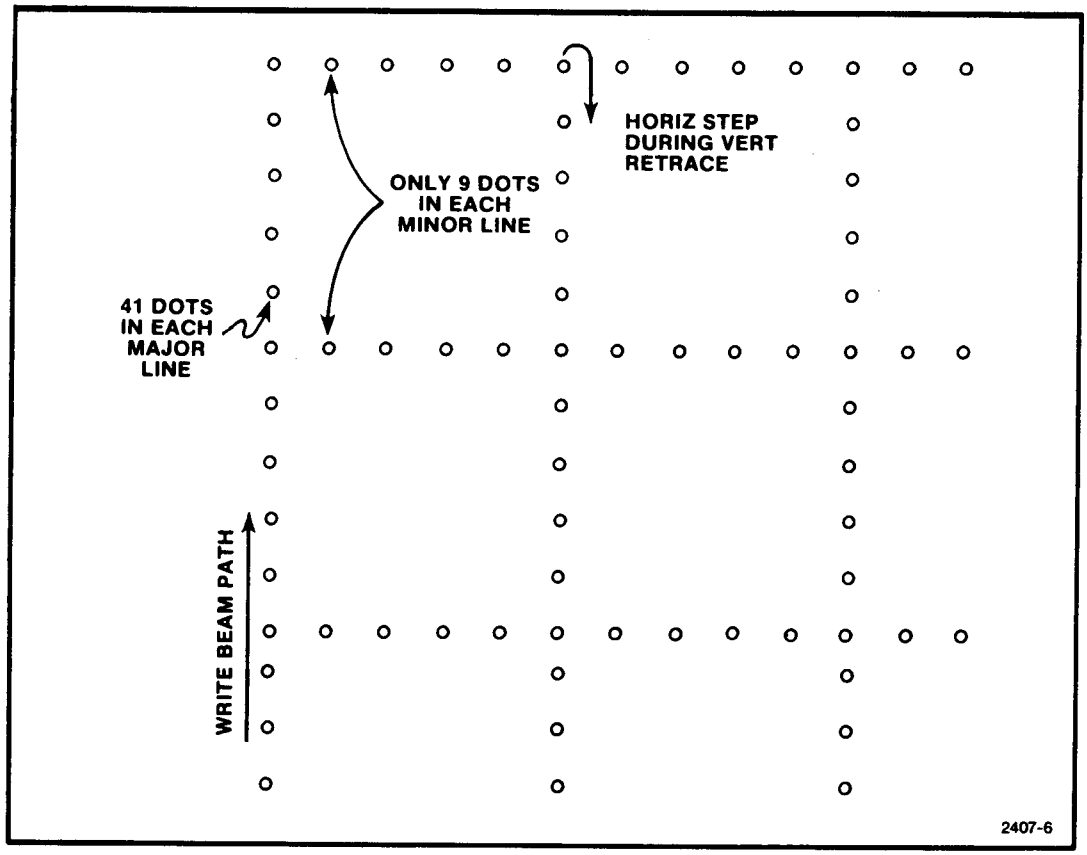


Fig. 3-6. Generating a graticule in TV mode.

When one-shot U250 times out, the negative transition on its Q output clocks U210A and the flip-flop's Q output (pin 12) goes high. At the same time, the $\overline{Q}$ output of U250 goes high, so both inputs of NAND gate U350D are high (top-right of the diagram). The output of U350D goes low and enables one-shot U150 through U350C. This one-shot drives the graticule Z-axis circuitry; its period determines the basic graticule dot size.

U150 is driven by one of two sources - a 625 kilohertz signal from U320B or a 125 kilohertz signal from U230B. The signal that is applied to the one-shot is selected by U060 and U310A.

If the instrument is in TV mode, TV/$\overline{\text{DIG}}$ is high and U060 selects its B inputs (pins 3 and 6). This applies the output of U320B to pin 4 of U150 and applies the $\overline{Q}$ output of U310A to pin 4 of U230B.

At the start of a graticule cycle in TV mode, a full 41 graticule dots must be produced. Then four lines of 9 dots are produced, followed by another full 41-dot line, and so on. Flip-flop U310A alternately enables U320B or U230B as it is set and cleared by U250 and the vertical ramp clock pulses. Refer to the timing diagram in Fig. 3-3. Full lines of 41 dots are produced when U310B's Q output goes high, enabling U320B and driving one-shot U150 with 625 kilohertz pulses. Minor division lines are produced when U310A is cleared and its Q output enables U230B through U060, driving the one-shot with 125 kilohertz pulses.

If the instrument is set to Digital mode, TV/$\overline{\text{DIG}}$ goes low and U060 selects its A inputs. Notice that pin 4 of the one-shot is tied high through U060. U230B is enabled every fifth vertical scan line by the Q output of U310A through U060. This drives the one-shot with 125 kilohertz pulses at the major division lines and disables all input to the one-shot during minor division lines. The result is a graticule with dots at the major divisions only for digitize operations and a full graticule for viewing on the TV monitor where data memory restrictions are not important.

Notice that the period of one-shot U250 is adjustable. Remember that when U250 times out, it delivers the enable signal to U150 through U350C and D. When properly adjusted, U250 delays this enable signal for a time equal to four 625 kilohertz clock pulses. Close inspection of the counters reveals that 45 pulses are available during the vertical scan period, where only 41 are needed. The period of U250 is adjustable to delay the enable signal for U150, ignoring the extra pulses.

Remember that a horizontal step occurs during each vertical retrace, moving the writing beam across the target in small increments. Counter U220 is clocked on every fifth vertical clock pulse. When this counter reaches a count of ten, indicating 50 horizontal steps have occurred, its pin 12 output fires one-shot U410. The pulse from U410 clears the start flip-flop (U420A and B) and resets the Graticule Generator. The mainframe channel switches are reset to accept the plug-in signals, the $\overline{\text{Z-AXIS INHIBIT}}$ control line is released, and the sweep is unlocked. The Graticule Generator now waits for the end of the next sweep unless the instrument is in graticule only mode.

Vertical Channel Switch and Amplifier

Vertical Channel Switch. The Vertical Channel Switch is shown on the left side of diagram 5. Two I.C.'s, U4625 and U4685, comprise the major portion of the channel switch. These special devices are designed to select one of two pairs of differential inputs with a single control line.

In the 7912AD, the vertical channel switch selects either the incoming vertical signal from the plug-in or the vertical ramp signal from the Graticule Generator. The MF CHAN SWITCH signal determines which of the two signals are passed at any time. Q4633, U4641, and the associated components form a dual comparator that alternately turns U4625 or U4685 on. When MF CHAN SWITCH is low, pin 11 of U4641 is high and pin 14 is low, enabling U4625. Pin 5 of U4641 (collector of the bottom transistor) is high and pin 1 is low, disabling U4685. As a result, the vertical signal from the plug-in is passed to the mainframe and the graticule vertical ramps are ignored.

Output signals from the vertical channel switch are delayed with a coiled delay line located adjacent to the CRT in the 7912AD mainframe. Precise termination of the line is important to minimize aberrations in the vertical signal.

High-Frequency Amplifier. The High-Frequency Amplifier stage, consisting primarily of integrated circuit U685, provides a 50-ohm input impedance (100 ohms differentially) to accurately terminate the delay line. The components coupling the input signal to U685 provide forward termination and compensation. The components tied to the inputs at the bottom of U685 set the quiescent operating conditions of the amplifier. R682 and R689 set the quiescent operating level; R684 and R688 are selected to accurately set the gain of the differential channels. These inputs to U685 also provide a means of injecting the auxiliary Y-axis signal into the vertical signal path. The auxiliary Y-axis signal provides trace separation in dual-trace vertical plug-ins. Vertical Gain adjustment R730 and thermistor RT731 set the current gain of the stage by varying the resistance across the output of U685. This adjustment sets the overall gain of the Main Vertical Amplifier circuit while the thermistor provides thermal compensation to stabilize the current gain against temperature variations.

Output Amplifier. The Output Amplifier provides final drive to the CRT deflection plates. The circuit consists primarily of integrated circuit, U745. Discrete components on pins 1-12 and 6-7 set the quiescent operating characteristics of the amplifer. R741 and R756 are selected to accurately set the gain of the differential channels. R753, R754, R767, R768, and R770 set the operating level of the stage while the parallel RC combinations provide frequency compensation for uniform gain throughout the bandwidth of the 7912AD.

The BEAM FINDER switch controls the current source for U745. Normally, the emitter current for U745 flows through the closed (released) BEAM FINDER switch (upper-right of diagram 1). When the switch is pressed, this path is opened and current must flow though R771 (near the bottom-right corner of diagram 5). This reduces the emitter current, limiting the dynamic range of the amplifier stage and compressing the display vertically within the graticule area.

The signal at the outputs of U745 is connected directly to the vertical deflection plates of the CRT. A distributed deflection plate system is used in the instrument for maximum frequency response and sensitivity. The signal at the output of U745 is connected to the deflection-plate structure in the CRT and then to the CRT termination network composed of LR5200, R5205A, LR5201, and R5205B. As the signal passes through the deflection-plate structure in the CRT, its velocity is essentially the same as the velocity of the electron beam passing between the vertical deflection plates. This synchronism of the deflection signal and the electron beam reduces the loss in high-frequency sensitivity due to electron-transit time though the deflection plate structure.

Horizontal Channel Switch and Amplifier

Overview. The Horizontal Amplifier circuit includes the Horizontal Channel Switch and Main Horizontal Amplifier. The channel switch selects the deflection signal from the output of the horizontal plug-in or from the Graticule Generator. The Main Horizontal Amplifier takes the output of the channel switch and provides the gain necessary to drive the CRT deflection plates.

Horizontal Channel Switch. The Horizontal Channel Switch (U528 - diagram 6) selects the deflection signal from the horizontal plug-in or Graticule Generator. The MF CHAN SWITCH (MainFrame CHANnel SWITCH) signal from the Graticule Generator determines which deflection signal is

selected. During the normal sweep time, the Graticule Generator is off, and MF CHAN SWITCH is low, selecting the horizontal plug-in deflection signal. When the Graticule Generator starts, it sets MF CHAN SWITCH high, selecting the Graticule Generator deflection ramp.

U528 provides a differential input for the input signal from the horizontal plug-in at pins 2 and 15, and the signal from the Graticule Generator at pins 7 and 10. R522, R516, R634, and R632 establish the 50-ohm input impedance of the the plug-in inputs. P420 and P630 are set according to the scan mode -- standard or option 4 (fast scan). The jumpers are shown on the diagram set for standard mode. When the jumpers are set for option 4, the input current from the plug-in is divided in half by the resistor network; only half of the input current is applied to the inputs of U528. The output at pins 12 and 13 provide a differential drive signal for the Main Horizontal Amplifier.

The RC network on pins 1, 8, 9, and 16 sets the operating point for the stage.

Input Amplifier. The differential signal from the Horizontal Channel Switch is connected to the bases of Q322 and Q318. Stage gain is controlled by the resistor network between the emitters of the these transistors, and is adjusted with R312. R418 provides a horizontal centering adjustment by balancing the emitter currents in each transistor. Emitter current is supplied from the +15-volt supply, and from the Z-Axis circuitry.

Two lines from the Z-Axis circuit enter the near the top of schematic 6. The leftmost line comes from the intensity protection circuit. If the protection circuit detects excessive beam current, it pulls this line to -15 volts, unbalancing the amplifier and deflecting the writing beam off the target.

The rightmost line supplies current to the emitters of Q322 and Q318 during normal operation. When the BEAMFINDER button is pressed, this current is interrupted and Q334 is forward-biased, applying a positive voltage to the bases of Q224 and Q216. The loss of emitter current for Q322 and Q318 reduces the dynamic range of the stage, while the positive voltage on the bases of Q224 and Q216 reduces the gain. As a result, the display is compressed within the target area regardless of the setting of the position control.

Driver and Output Amplifiers. The Driver and Output Amplifiers provide the current required to drive the CRT deflection plates. Since the circuit normally amplifies only horizontal ramps, it is designed to provide more current for the negative-going half of the input signal (retrace) than for the positive half. Because of this difference in output current, PNP transistors are used in the positive half where current is driven into the deflection plates, and NPN devices are used in the negative half where current is pulled from the plates. The halves are functionally identical except for different resistor values and three diodes (CR212, CR112,and VR006) that accomplish the level shifting required for the NPN devices in the negative half of the amplifier. We will discuss only the positive (top) half of the amplifier in detail.

The positive-going ramp on Q322's collector is coupled to the bases of Q222 and Q224. Q224 provides gain at low frequencies while emitter follower Q224 provides the current gain for the high frequency path through C128 and C132. The high- and low-frequency signal components are summed at the base of Q128. Q128, Q132, Q028 and Q022 form a cascode output stage with Q128 and Q132 paralleled to provide the high drive current for the final output devices. Feedback for the amplifier is provided through R126 and C024.

Z-Axis and High Voltage

Overview. The Z-Axis and High Voltage circuits generate the voltage levels required to drive the writing portion of the 7912AD scan converter tube. A regulated -10-kilovolt cathode supply and a -6-kilovolt focus supply are included, as well as a fast Z-Axis (unblanking) amplifier. Protection circuitry for the scan converter target is also incorporated.

The Z-Axis and High Voltage circuit is shown on diagram 7. Referring to the diagram, the write portion of the scan converter tube is represented at the top center. To the right of the tube is the protection circuit and astigmatism control. The high-voltage supply is shown to the left of the tube and in the bottom-left is the Z-Axis circuit. Notice that the majority of the high-voltage supply is in a potted assembly, A74. The filament supply is shown in the bottom-right.

High Voltage Supply. At the left edge of the schematic are two NPN transistors, Q006 and Q206, driving the primary of an inverter transformer T5300. The transistors receive power from an unregulated ± 17-volt supply; the LC filter composed of L104 and C008 reduces the

supply ripple. This inverter circuit oscillates at about 20 kilohertz, using the small windings on T5300 for feedback to sustain oscillation.

The secondary windings of T5300 drive the focus and high-voltage supplies. The upper winding provides drive for the -6-kilovolt focus supply and D.C. restorer circuit. The lower winding provides drive for the -10-kilovolt cathode and control-grid supply.

-10-Kilovolt Supply. The 20-kilohertz output of T5300 is applied to a full-wave rectifier/voltage doubler formed by the six diodes and two capacitors to the right of the transformer. The output of the doubler is filtered and coupled to a pi-network filter composed of the three .001 microfarad capacitors near the scan converter tube. Below the filter is a Darlington transistor, Q628, connected as a capacitance multiplier. Ripple coupled through the first filter capacitor to the base of Q628 is inverted and amplified. The resulting signal is coupled through the rightmost filter capacitor to cancel the ripple. CR636 and CR624 protect the circuit from damage caused by arc-over in the scan converter tube. Extensive circuit protection against interelectrode arcing is used in all portions of the Z-Axis and High Voltage circuits.

Blanking and D.C. Restoration. The -10-kilovolt supply provides bias for the Scan Converter control grid through the circuit shown at the right of the voltage doubler. The top secondary winding of T5300 provides a high-amplitude sine wave through a 510K resistor to the D.C. restorer circuit. Follow the line from the top secondary of T5300 down through the 510K resistor to a diode. This diode clamps the positive excursions of the sine wave to the level set by the CRT Grid Bias control, R602. The clamp level ranges from about +50 to +130 volts. A typical setting results in a +90-volt clamp level.

The negative excursions are clamped at the current Z-Axis blanking level by another diode, shown to the right of the one just discussed. The Z-axis signal enters at the lower right of the restorer circuit through the 51-ohm resistor just above P842. For the purpose of this example, assume that the signal ranges from about +10 volts (blanked) to +45 volts (unblanked). The actual level is determined by the Z-Axis drive and by the scan converter characteristics. The clipped sine wave results in a square wave where the upper level is established by the CRT Grid Bias control and the lower level by the Z-axis signal.

The square wave is AC coupled to the -10-kilovolt grid-bias supply through the .001 microfarad capacitor, shown next to the Z-axis clamp diode. Positive excursions are clipped at the -10-kilovolt supply level by the diode directly above the coupling capacitor. Negative excursions reverse-bias this diode and forward-bias the diode just below the neon surge protector. The capacitor tied to the anode of this diode charges to the -10-kilovolt supply level minus the amount of blanking signal applied. The potential on this capacitor is applied to the control grid through a one megohm resistor. When unblanking occurs, the square wave amplitude is increased and the voltage on the capacitor returns to near -10 kilovolts, unblanking the writing beam.

Protecting the Circuit. Neon spark-gaps protect several sensitive components in the DC restoration circuit from damage due to interelectrode arcing in the scan converter tube. These devices conduct if their terminal voltage exceeds about 145 volts, protecting the diodes in the circuit from excessive voltage and current levels.

Focus Supply. The -6-kilovolt focus voltage is developed with a DC restorer circuit similar to the one used in the Z-axis circuit. The same sine wave from the top secondary of T5300 is used. The sine wave is clipped by two diodes in the high voltage assembly. The negative excursions are clamped near ground potential, and the positive excursions are limited to the level set by the focus voltage. However, for Serial Number B100913 and up, focus centering (R5210) is added to allow the focus supply voltage to be adjusted from -6 kilovolt to -6.5 kilovolt in order to accommodate minor variations in the crt or H.V. brick.

Regulating the High-Voltage Supply. The -10-kilovolt supply voltage is divided by a voltage divider in the high-voltage assembly. The resulting voltage is applied to operational amplifier U612 (upper left corner of the diagram). The output of U612 controls the base drive current of the inverter transistors Q006 and Q206 through Q616. A decrease in the output voltage causes U612 to increase the base current to Q616, increasing the drive to the oscillator. The increased drive causes the oscillator pulse width to increase, raising the output voltage to the proper level. The High Voltage adjustment, R618, sets the quiescent drive to U612, adjusting the nominal high-voltage level.

Z-Axis Amplifier.

The Z-axis amplifier, shown in the bottom-left corner of diagram 7, accepts signals from the Z-axis logic and the Graticule Generator and amplifies them to the levels required by the scan converter. The amplifier is designed to insure adequate rise and fall times for the 500 picosecond/division sweep rates possible in the 7912AD.

Input Circuits. The current-drive signals from the Z-axis logic and graticule generator are summed at the base of Q806. Q802 thermally compensates the input transistor and Q708 shifts the graticule Z-axis signal to compatible levels. The Z-axis amplifier is connected as an operational amplifier with R808, R818, C808, and C820 providing feedback. Q736 forms a voltage source for the amplifier.

Positive Signal Excursions. Positive-going drive signals reduce the current through Q806, forward-biasing Q726. Zener diode VR718 sets the D.C. operating level for Q726. As Q726 turns on, its emitter swings negative, forward-biasing the bottom half of the common-base output amplifier, Q826. Current from Q736 and the discharge of C735 (bottom-right of the circuit) passes through Q726 and Q826 to charge the control grid capacitance of the CRT. This current path allows the unblanking signal to overcome the grid and wiring capacitance and rise very fast.

Negative Signal Excursions. Negative-going drive signals increase the current through input transistor Q806, causing its collector voltage to rise. Emitter follower Q714 tracks the rising voltage, and the positive step is coupled through Q714, C718, R824 and C830 to the emitter of Q834. The pulse turns Q834 on, quickly discharging the grid capacitance.

Current Source. Q732 functions as a current source for the output stage of the amplifier, compensating for differing sweep speeds and intensity levels. A sample of the Z-axis output signal is coupled through R836 and C832 to drive the base of Q732. Positive signal excursions are passed by CR828 to the base, while negative excursions are passed by CR832 and C738. The R-C network consisting of R826 and C826 compensates for a similar network in the grid supply. CR836 thermally compensates Q732, while R730 provides the D.C. base current.

Feedback. The feedback path for the amplifier consists of R808, R818, C812, C808 and C820. A high-frequency peaking adjustment is provided with C808. The amplifier is compensated by R812, while CR814 acts as a voltage-variable capacitor, compensating for transient-response variations that accompany sweep-speed and intensity changes.

Target Protection Circuit

The diode target in the scan converter tube is sensitive to burns caused by excessive writing beam current density. Burns can be the result of operating at a low sweep speed with a high intensity setting, or reducing sweep speed without first reducing intensity.

The 6800 MPU protects against gross misadjustment of the front-panel controls by limiting the writing beam intensity. The analog protection circuit, shown in the upper-right of diagram 7, supplements the 6800 intensity limit protection. If this circuit detects excessive writing beam current, it deflects the writing beam off target. A front-panel indicator warns the operator if the 6800 or analog protection circuits become active.

Protection Threshold. A sample of the Z-axis output signal is fed to the protection circuit through CR450 (bottom-left corner of the protection circuit). Recall that the Z-axis output typically ranges from about +10 volts (blanked) to about +45 volts (unblanked).

R450 and R452 form a voltage divider that charges C456 to about +10 volts. When the writing beam is blanked by the Z-axis signal, CR450 is reverse-biased. During unblanking the diode conducts for a short time--the time depending on the sweep rate. Slow sweep rates result in more current passing through CR450, adding to the charge on C456. Since the main intensity setting affects the amplitude of the unblanking pulse, the charge rate of C456 depends on a combination of sweep speed and intensity adjustment. If the combination could result in target damage, C456 charges to the threshold voltage of the Schmitt trigger formed by Q356.

The protection circuit also senses the actual beam current in the scan converter tube. Excessive beam current causes the grid to conduct, forward-biasing Q452, immediately charging C456 to the Schmitt threshold level. The threshold, set by R346 and R348, determines the protect level for the scan converter tube.

Deflecting the Beam. When the Schmitt trigger is tripped, the right half of Q356 cuts off. Q256 is no longer forward-biased, and it cuts off as well. As its collector drops toward ground level, Q252 is turned on and its collector swings positive. The positive level cuts off Darlington transistor Q156 and its collector goes negative to forward-bias Q154. Q146 turns on, connecting -15 volts to one side of the differential horizontal amplifier. This unbalances the amplifier and forces the writing beam off the target.

Disabling BEAMFINDER. The front-panel BEAMFINDER compresses any scan into the displayable target area to aid in setting up the instrument. If the target protection circuit deflects the beam off target, however, the BEAMFINDER must be disabled to prevent the beam from being returned to the target.

When BEAMFINDER is pressed, Q046 is reverse-biased, and the emitter current for the horizontal amplifier is interrupted. The protection circuit disables BEAMFINDER by turning Q152 on with Q154. The collector of Q152 goes low and holds Q046 on, regardless of the BEAMFINDER button.

The low on the collector of Q152 also pulls PROTECT ENABLE low, enabling the circuit that drives the front-panel DECREASE INTENSITY indicator.

Reading System

The 7912AD reading system recovers the waveform written on the scan converter target and outputs it as video for display (TV mode) or digitizing (digital mode). The reading system includes the following blocks shown on the 7912AD block diagram (Fig. 3-1): X & Y Ramp Generators, X & Y Scan Control, Read Gun Supplies, Cathode Regulator, Video Preamp, and Video Processor.

In digital mode, the ramps are synchronized by ramp gate signals from the Data Buffer board. In TV mode, the ramps are synchronized by a scan generator IC. The Read Gun Supplies align and focus the reading beam. The Cathode Regulator blanks the reading beam during retrace and regulates the read gun current during the time it is unblanked. The Video Preamp amplifies the small changes in video levels that are detected when the target is scanned. In TV mode, the video is combined with video sync pulses for composite TV outputs. In digital mode, the video is shifted to TTL levels and transmitted to the Data Buffer as a two-level (high or low) signal called SVID (Schmitted Video).

X & Y Ramp Generators

In TV mode, the target is scanned in a standard TV format. In digital mode, however, the scan is, in effect, rotated 90 degrees: the fast scan is vertical, while the slow scan is horizontal. Refer to the descriptions under TV Mode and Digital Mode in Section 1 to review the scan converter operation and for figures that illustrate the two scan modes.

Rather than switch the X & Y Scan Generators when the modes are switched, timing components are switched that change the slope of the ramps. Because the end points of the ramps are fixed, changing the slope of the ramps changes their scan rates.

Ramp Generators. To grasp the scan techniques used by the reading system, let's follow how the X ramp is generated. The circuits used to generate the two ramps look alike; understanding of one can be applied to the other.

See Fig. 3-7 for a simple diagram of the X Ramp Generator (the full diagram for the ramp generators is diagram 8 in the foldouts section). The heart of the generator is the Miller Integrator comprising Q630, Q742, Q740, C622, and resistors connected to one of Q630's gates. The

transistors compose an inverting amplifier that tries to maintain its two inputs at zero by charging C622 with a positive ramp. The slope of the ramp (dv/dt) is controlled by the current through C622; this is set by the resistance between C622 and -15 volts. This resistance is lumped as R_{DIG} and R_{TV} on the X ramp generator figure.

In digital mode, Q320 is turned on, reverse-biasing the diode conected to R_{TV}. This leaves R_{DIG} as the current path for the input side of the Miller Integrator capacitor. In TV mode, the transistor is turned off, allowing R_{TV}, a much smaller value, to swamp out R_{DIG}, speeding up the ramp. R_{TV} is R031. The value of R_{DIG} is set by P030, which selects R033 for normal scan or R032 for option 4. The value of R032 is smaller to speed up the ramp for the fast-scan option. This option cuts the time for a scan of the target in digital mode by about one-fourth.

When the ramp reaches +10 volts, it switches the upper limit comparator, transistor array U440. The threshold of the comparator is set at +10 volts by CR420, R344, and R436. When the comparator switches, it places a low on pin 9 of U240C through Q440. U240C and U240D are wired as an S/R flip-flop, called the Limit flip-flop on the X Ramp Generator diagram; pin 9 is the set and pin 13 the reset. When set, the flip-flop turns on the Discharge Source, Q230, by turning off Q232. This causes the Miller Integrator to ramp down.

Meanwhile, the other output of the flip-flop, called X RAMP GATE, goes low to reset the Start flip-flop (U120C and U240A). This turns on Q130 to reverse-bias the diode connected to the Miller Integrator input. So when the ramp returns to zero and the Discharge Source is turned off, the integrator is put on hold--there is no current path to charge the integrating capacitor. This holdoff time ends on the next $\overline{\text{X START}}$ pulse, which sets the Start flip-flop, turning off Q130 and allowing the Miller Integrator to begin charging again through CR230.

But suppose the ramp slope varies from ideal. Because of the hold-off, the ramp start is synchronized with $\overline{\text{X START}}$. If the slope of the ramp varies, then, the end of the ramp occurs out of step with the X REF pulse supplied by X Scan Control. To correct the slope of the ramp, two D flip-flops, U140B and U140A act as a phase detector to sense the time difference between ramp end and X REF. This time difference is integrated by U040 to generate a correction current that is applied to the Miller Integrator.

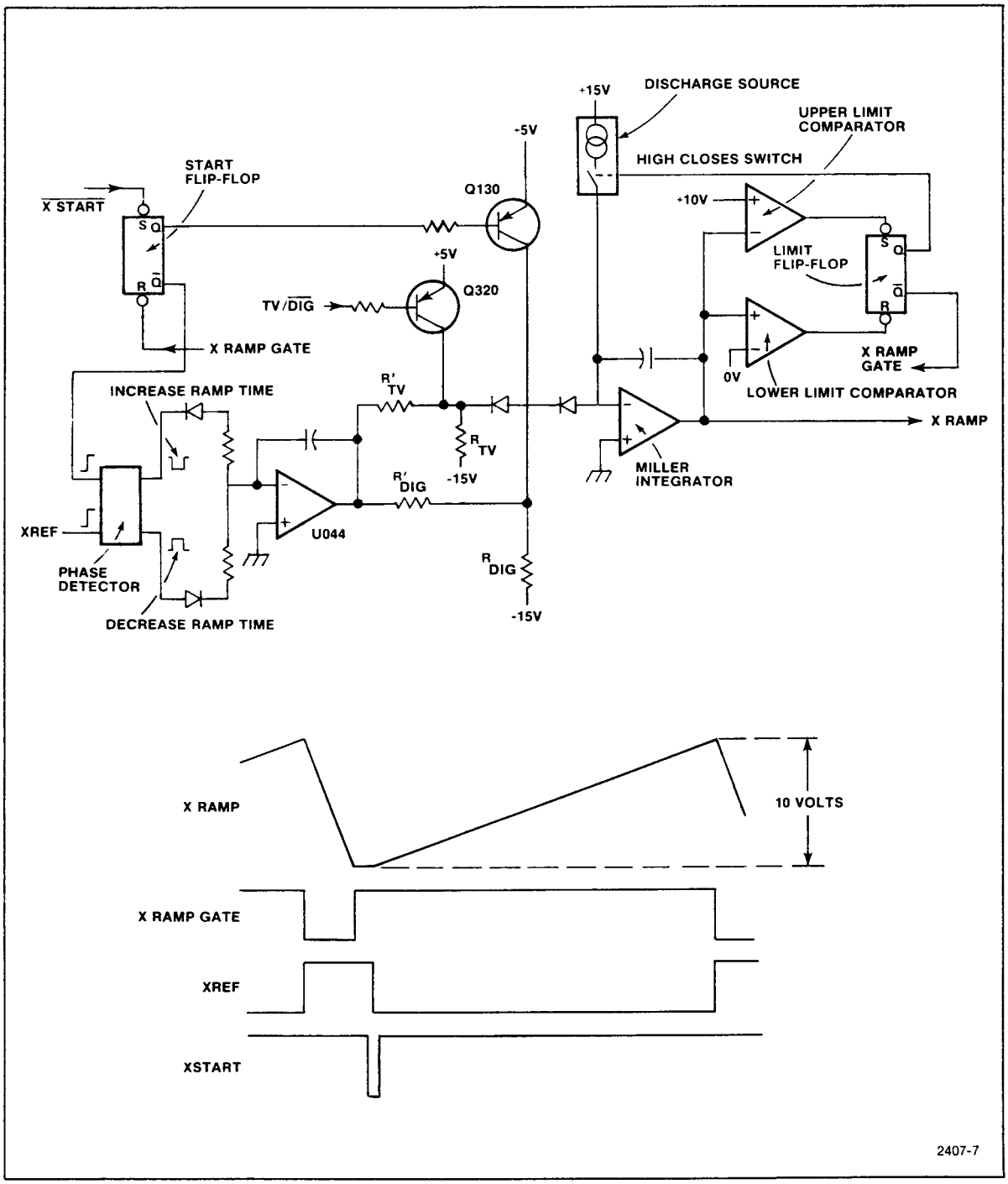


Fig. 3-7. A simple diagram of the X Ramp Generator showing timing on the control lines.

Assume the ramp is too fast, that is, its slope is greater than ideal. In that case, X RAMP GATE goes low, resetting the Start flip-flop and clocking U140B before X REF clocks U140A. For the time between the negative transition of X RAMP GATE and the positive transition of X REF, $\overline{Q}$ of U140B is low, pulling down on the negative input of U040. The resulting high on U040's output charges C042; the greater the difference between the end of the ramp and the reference pulse, the more the output of U040 rises to charge C042. When X REF arrives, U140A is set; the Q outputs of the two flip-flops are ORed to clear both flip-flops. When cleared, the flip-flops reverse-bias the diodes on their outputs; this allows the output of U040 to remain at its present level, injecting a correction current into the Miller Integrator through R_{DIG} (R036 or R034). In TV mode, this correction current is swamped out by the current through R_{TV} (R034).

If the ramp is too slow, the polarity of the current is reversed because U140A is set before U140B. It may take several ramp cycles to bring the ramp end and the X REF pulse together, but each cycle reduces the difference except in one case. When the end of the ramp occurs after $\overline{\text{X START}}$, the Start flip-flop remains reset until the following $\overline{\text{X START}}$ pulse, holding off the ramp. Meanwhile, U040 is attempting to speed up the ramp because the end of the ramp is occurring after X REF. Therefore, the ramp slope increases, but its period remains longer than that of two $\overline{\text{X START}}$ pulses because of the long holdoff. When U040 pumps the largest negative current allowed by the divider formed by R030, CR130, and R224, Q224 turns off. The next X REF pulse then fires (through U1210D and U210C) the Out-Of-Lock one-shot, U340A. This turns off holdoff transistor Q130, allowing the ramp to free-run. Its period with the large correction current is then much shorter than the period of X REF, causing a cange in the correction current that restores the ramp slope to approximately ideal. After $\overline{\text{OOL}}$ times out, $\overline{\text{X START}}$ reasserts control.

This is the process that makes the large adjustment in ramp frequency and slope when the 7912AD operating mode is changed from digital to TV or the reverse. The $\overline{\text{OOL}}$ pulse is a significant portion of the two-second setup time for the instrument to change modes. While aserted, $\overline{\text{OOL}}$ causes the Video Processor to blank the TV outputs until the ramps are again phase-locked.

Scan Amplifiers. Circuits on diagram 9 amplify and translate the X and Y ramps to push-pull signals to drive the reading gun deflection plates. Because the amplifiers are so similar, let's look at the one for the X ramp to gain an understanding of both.

The X ramp is buffered by operational amplifier Q1040-Q1140. The amplifier input is a summing point for the ramp current (adjusted for normal or option 4 scan by P1030) and two other currents. One current, controlled by R930, shifts the level of the input to center the ramp. The other current is a small amount of either the positive or negative side of the Y ramp push-pull signal (adjusted by R1414) to vary the X ramp a slight amount during each vertical scan. This is adjusted during calibration to correct the read scan for any left/right skew.

The ramp is translated to a push-pull signal by the paraphase operational amplifier comprising the transistors just to the right of the input buffer. The feedback resistors in the two sides of the amplifier, R1242 and R1246, are unequal to overcome unbalance inherent in a paraphase amplifier. Q1143A and Q1142B provide a temperature-compensated current source for the amplifier. Although the time for a complete digital scan is the same as the time for a TV scan, the fast ramp in digital mode (the Y ramp) must have twice the slope of the fast ramp in TV mode (the X ramp). This follows from the number of Y ramps (512) to be completed in digital mode for each X ramp compared to the number of X ramps (262.5) to be completed for each Y ramp in the interlaced TV scan. To handle the fast Y ramp in digital mode, the Y paraphase amplifier has peaking through R1200 and C200, while the X paraphase amplifier does not.

The overall gain of the input buffer and paraphase amplifier for the X ramp is one: the single-ended 10-volt ramp is converted to push-pull 10-volt ramps centered at ground. In the case of the Y ramp, however, the overall gain is reduced to change the aspect ratio. The difference in the input resistors R1002 and R1040 (or R1004 and R1041 for option 4) accounts for this difference in gain.

The push-pull ramps are amplified and level-shifted by the amplifier on the right half of diagram 9. These are cascode, push-pull amplifiers with feedback, identical except for the input resistances which set their gain. R1410 and R1420 are slightly smaller than R1440 and R1445, again to make a gain difference that establishes the 3:4 scan aspect ratio. Both amplifiers have a common mode voltage set at +244 volts during calibration. The portion of the ramps within the unblanked scan of the target is set at 93 volts for the X ramp and 69 volts for the Y ramp during calibration.

Scan Control

In TV mode, a single-chip scan generator, U014, shown on diagram 12 controls the reading gun scan. A CMOS IC, it requires level shifters on both inputs and outputs. Either 525 or 625 lines per TV frame can be selected by P104. The generator is driven by a 500 kilohertz clock derived from a Data Buffer clock output or by an external TV sync signal. If used, the external sync is buffered and shaped before being applied to pin 20; the IC senses the external sync by rectifying it. When it senses the external sync, it uses it to phase-lock its own 500 kilohertz oscillator. External sync continuously triggers U206A to block the Data Buffer clock at U302A. If necessary, R002 can be adjusted to insure that the IC stays locked to the external sync.

The reference and ramp start pulses for the X & Y scans in TV mode are derived by logic to the right of the scan generator IC on diagram 12. X REF is generated by U226B, which is clocked high as soon as the scan generator asserts its horizontal blanking output, releasing U226B's clear input. $\overline{\text{X START}}$ is asserted six counts (12 microseconds) later through the action of U322, wired as a BCD counter. This delay allows retrace, started at the positive transition of X REF, to be completed before $\overline{\text{X START}}$ kicks off the X ramp. X REF is unasserted again at the end of horizontal blanking when the scan converter clears U226B.

In digital mode, the X and Y ramp gate signals supplied by the Data Buffer drive one-shots that are selected by U246 as the X and Y reference and start signals.

Y ramp control in both TV and digital modes is similar to that just described for the X ramp.

Read Gun Supplies

The Read Gun Supplies provide alignment and focus for the read gun to achieve minimum shading and good resolution of the reading beam. Shading is caused by off-normal landing of the beam on the target, which varies the detected video baseline. If great enough, this causes a low video level to be mistaken for a high level, and vice versa, when the video is digitized.

While measures are taken by the Video Processor to correct shading, the hybrid design of the read gun reduces the effect at its source. The X & Y ramps drive electrostatic deflection yokes, which accomodate better than magnetic deflectors the different scan rates needed in TV and digital modes. But the Read Gun Supplies on diagram 10 drive magnetic alignment coils for an axial magnetic focusing field. R732, X Alignment, and R632, Y Alignment, are adjusted to set currents from identical DC complimentary amplifiers. These currents (about 17 milliamps, variable $\pm$2 milliamps) produce magnetic fields in the coils that improve video contrast between written and unwritten portions of the target.

R602, Anode, is adjusted for a first anode voltage of +259 volts. When R804, Mag Focus, is then adjusted to focus the displayed video, the change in the focus coil current is sensed by U616. U616 drives Q716 to change the first anode voltage slightly so the anode tracks changes in the coil current; this preserves small reading beam spot size. The first anode voltage also controls the anode connected to pin 8 of the scan converter tube and the mesh.

Cathode Regulator

The Cathode Regulator at the lower right of diagram 10 blanks and unblanks the reading gun while regulating read gun current. Cathode current is regulated by the imbalance between the inputs to U828 introduced by R728, the Cathode Current adjustment. U828 sets the grid voltage to allow enough cathode current through R736 to restore balance to its plus and minus inputs. This is set during calibration while observing the average voltage across R736.

When the blanking signal, CRB (Composite Retrace Blanking), goes high during either vertical or horizontal retrace, it turns off Q948. This turns off CR936 and turns on CR934; these diodes act as a fast switch on the input of operational amplifier Q928-Q834. The voltage at TP838 rises, driving both the grid and cathode more positive. When unblanked, the cathode potential is about -6 volts. The target, which is set at a higher voltage, provides an accelerating potential for the small proportion of the reading beam that passes through the mesh during unblanking. (While cathode current is on the order of 750 microamps, video current from the target is measured in nanoamps.) When the cathode rises approximately 18 volts during blanking, it becomes more positive than the target and all cathode current is captured by the mesh.

Video Preamp

Nanoamp-level video signals detected from the scan converter target are amplified by the Video Preamp, shown on diagram 10. Although the amplifier is AC-coupled, a resistor network ahead of the input capacitor sets the target potential. This potential is adjusted by R1952 to match a value specified for each scan converter tube.

Two amplifier stages are indicated on the video chain block drawing, Fig. 3-8. The first stage is an inverting amplifier formed by Q1957, Q1962, Q1965, Q1968, and Q1973. Although FET Q1957's input impedance is very high, it appears to be a virtual ground because of negative feedback through R1957, a specially selected low-noise resistor. As a result, the amplifier takes all the input current recovered from written portions of the target. These negative video pulses are converted to a voltage output that draws the input current through R1957; R1957 sets the ratio of output voltage to input current at 1 millivolt/nanoamp. R1972, R1977, and C1976 are adjusted for best transient response.

The output stage comprising the five-transistor array U1983 and Q1991 is an inverting amplifier with a gain of five set by R1981 and R1976. The overall gain of the two stages results in a voltage change of 5 millivolts at the output of Q1991 for each nanoamp change in input current. During calibration, a 20-millivolt input (500 nanoamps) is injected through J1947 and the gain of the amplifier is checked. Because the output is loaded by 50 ohms during the check, an overall voltage gain of 10 is noted at J1994. In normal operation, however, the Video Preamp operates into a voltage divider formed by R1994 on diagram 10 and R744 and R732 on diagram 11. This divides by two the input to the amplifier on the Video Processor board. An R-L-C network at that input makes up a four-pole Butterworth filter with a steep cutoff at 4.5 megahertz to reduce noise.

Video Processor

The Video Processor restores the DC level of the video, corrects shading and thermal variations to reduce the effect of noise, and converts the video to a binary signal for digitizing. The Video Processor also adds TV sync signals to the binary and linear video signals for display on a TV monitor.

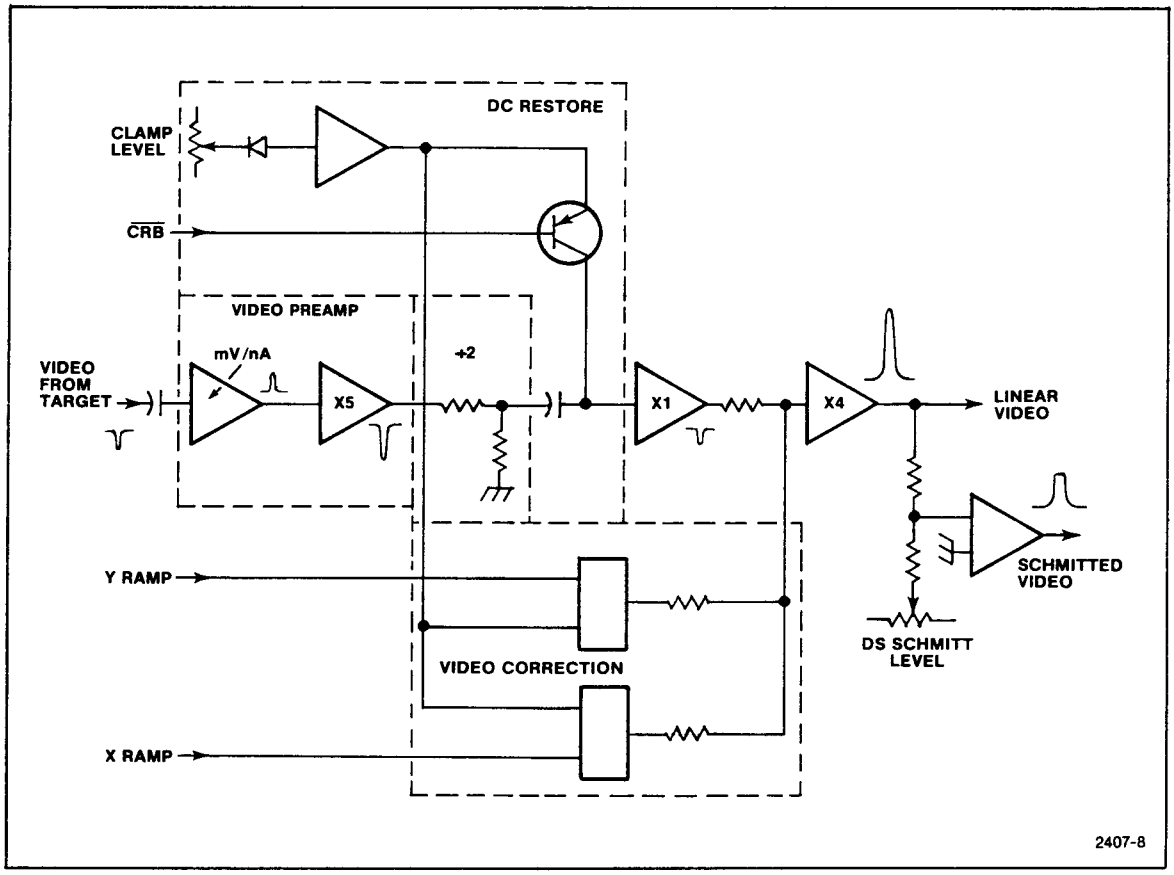


Fig. 3-8. A block drawing of the video chain in the 7912AD showing the main circuits on the Video Preamp and Video Processor boards.

Clamp. DC restoration occurs at the node where Q716, C720, and Q722A connect on diagram 11. This node is shown as the X1 amplifier input on the video chain block drawing. $\overline{\text{CRB}}$ low turns on Q716 during either vertical or horizontal retrace. This charges C720 to the DC level set by U724. The following FET isolates this node so the DC level remains after Q716 is turned off. The conductance of a diode mounted on the CRT corrects for temperature changes. Target noise increases with temperature; current through the diode tracks this change and the increased current through R722 causes U724 to respond by raising its output level. This raises the DC level of the video, reducing the effect of the noise on the Schmitt trigger circuit that follows. Because the video is inverted by the following X4 amplifier before being applied to the Schmitt comparator, raising the DC restoration level lowers the video

baseline at the Schmitt. This tends to reduce the level of noise below the Schmitt trigger point.

The clamp level is adjusted during calibration by blanking a small part of a scan near the center of the target when Q716 is turned off. The video baseline at TP706 during this blanked interval is observed with the writing beam turned off so there are no video pulses. R406 is then adjusted for an equal level at the output of U724.

Video Correction. Several effects, including shading of the reading beam and target leakage, cause the baseline of the detected video to vary as the target is scanned. Every scan converter tube has a slightly different profile; its effect can be reduced by the correction circuits at the lower left of diagram 11. These are calibrated to shape the correction current to offset the variation in the baseline. Because target leakage rises with temperature, the correction current must undergo a corresponding, but opposite change. This is illustrated in Fig. 3-9.

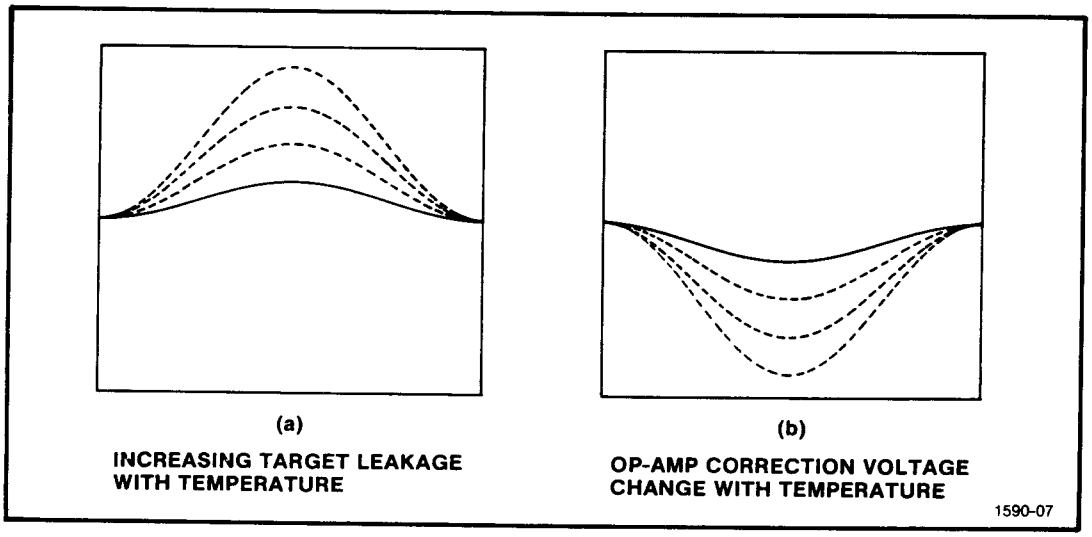


Fig. 3-9. Correcting the video for target leakage.

The video correction signals are based on the X & Y ramps. Properly adjusted, these circuits produce a correction signal that varies in magnitude as the beam scans the target, just canceling the effects of shading and target leakage at each point.

To grasp how this is accomplished, let's follow how the video is corrected during a vertical scan. First the Y ramp is converted to a triangle waveform. As the Y ramp rises from zero, Q836 is turned on, but conducts less as the ramp rises. Q832 is turned off until the ramp approaches +5 volts; until that point the minus input to U826A sums current from R728, R822, and the feedback resistor, but none from Q832. As Q836 begins to conduct less, it steals less current from Q834, which allows the plus input of U826A to go more positive; the op-amp output rises to pull up the negative input.

Near the center of the ramp, approximately +5 volts (depending on R832), Q836 turns off and Q832 begins to conduct, supplying current to the minus input of U826A. As a result, the op-amp output must supply less current to keep the plus input, which is not changing, and the minus input balanced. The result is a triangular output that rises while the ramp is rising from 0 to +5 volts, but falls while the ramp continues to rise from +5 to +10 volts. The symmetry of the triangle wave depends on the setting of R832.

The output of U826A controls a current source for a differential amplifier whose outputs drive U826B, which produces the correction signal. If the differential amplifier is balanced, U826B sees a null at its inputs, so produces no correction signal. If, however, unbalance is introduced by the Y Gain adjustment, R806, the inputs to U826B are unbalanced in proportion to the current controlled by U826A; then U826B produces a current output that is a replica of the triangular wave from U826A to offset this unbalance. Any unbalance is further compounded by current introduced by U724 as a result of temperature changes. During calibration, R832 and R806 are adjusted for least variation in the baseline at TP600. The effect of this correction is shown in Fig. 3-10.

Schmitted Video. The linear video signal at TP600 on diagram 11 represents 10 millivolts for each nanoamp of target video current. This signal is divided by a network connected to pin 2 of U630, the Schmitt trigger. The network is adjusted by R635 to require +400 millivolts of linear video to trip the Schmitt, whose other input at pin 4 is set at about ground. (This corresponds to 40 nanoamps of target current.) Hysteresis is provided by the coupling of the two emitters at pin 3. Positive feedback through R525 sharpens the switching action. The output at pin 5 of the transistor array is level-shifted and supplied to the Data Buffer as SVID.

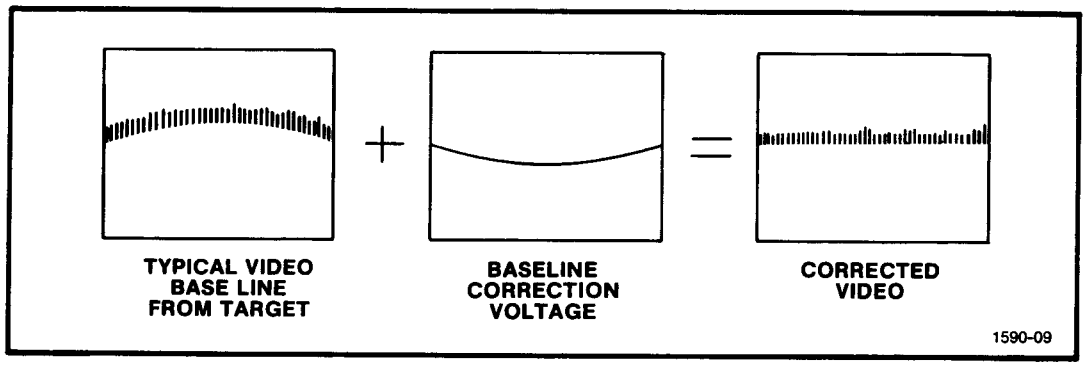


Fig. 3-10. Correcting the video to offset baseline variations.

Video Outputs. One Schmitted video output, pin 10 of U630, is amplified and used to drive the gates on diagram 12 that provide the COMP BINARY VIDEO output. The high-low video is ORed with the readout video, then ANDed with retrace blanking. A TV sync signal from the scan generator IC is added in a resistor network that results in a +1 volt level for full white and a level less than +0.3 volt for black.

Meanwhile, the linear video input to the Schmitt trigger circuit drives Q504 on diagram 12 where it is summed with the readout video. It is blocked at CR428 during blanking, so the video and sync drive Q522 on a time-share basis for a COMP LINEAR VIDEO output.

Note that both composite video outputs are blanked when either $\overline{\text{OOL}}$ or $\overline{\text{DIG}}$ clears the output of U342A.

6800 Microprocessor System

Block Diagram

Figure 3-11 shows a block diagram of the 6800 microprocessor system in the 7912AD. The 6800 system is the instrument master controller. It accepts and decodes commands from the front-panel or the IEEE 488 bus and sets instrument operating parameters in response to these commands. The 6800 also controls the IEEE 488 interface and provides a transparent bus interface to programmable plug-ins. The TV scale factor readout is generated by the microprocessor system.

The 6800 MPU (Microprocessing Unit) acts as the master of the dual-processor architecture in the 7912AD. It passes commands to the fast 2900 system to initiate memory control operations such as digitize, average-to-center (ATC), or send waveform data over IEEE 488 bus.

A 15-bit address bus and an 8-bit data bus provide the communication path between the MPU, MPU memory, and the instrument functions it controls. A set of bus buffers provides drive for the internal busses and generates select signals that allow the MPU to selectively communicate with each of the functions it controls. We will discuss the 6800 bus in more detail later.

When one of the instrument functional blocks requires the MPU's attention, it asserts an interrupt line that sets a bit in the Interrupt Occurred Register. The Interrupt Control Logic signals the processor that an interrupt has occurred. If the MPU has not disabled (masked) interrupts, it temporarily suspends execution of the current task and jumps to a routine that determines the source of the interrupt. Then control is passed to an appropriate service routine. For example, assume the operator has just turned the front-panel TV SCALE FACTORS switch from OFF to ON. The MPU receives an interrupt from the Interrupt Control Logic. It suspends execution of the current task and reads the Interrupt Occurred Register to determine the source of the interrupt. Then control is passed to a routine that enables the scale factors readout. Finally, the processor resumes execution of the previous task. We'll discuss the interrupt sequence in more detail when we discuss the Interrupt Control Logic.

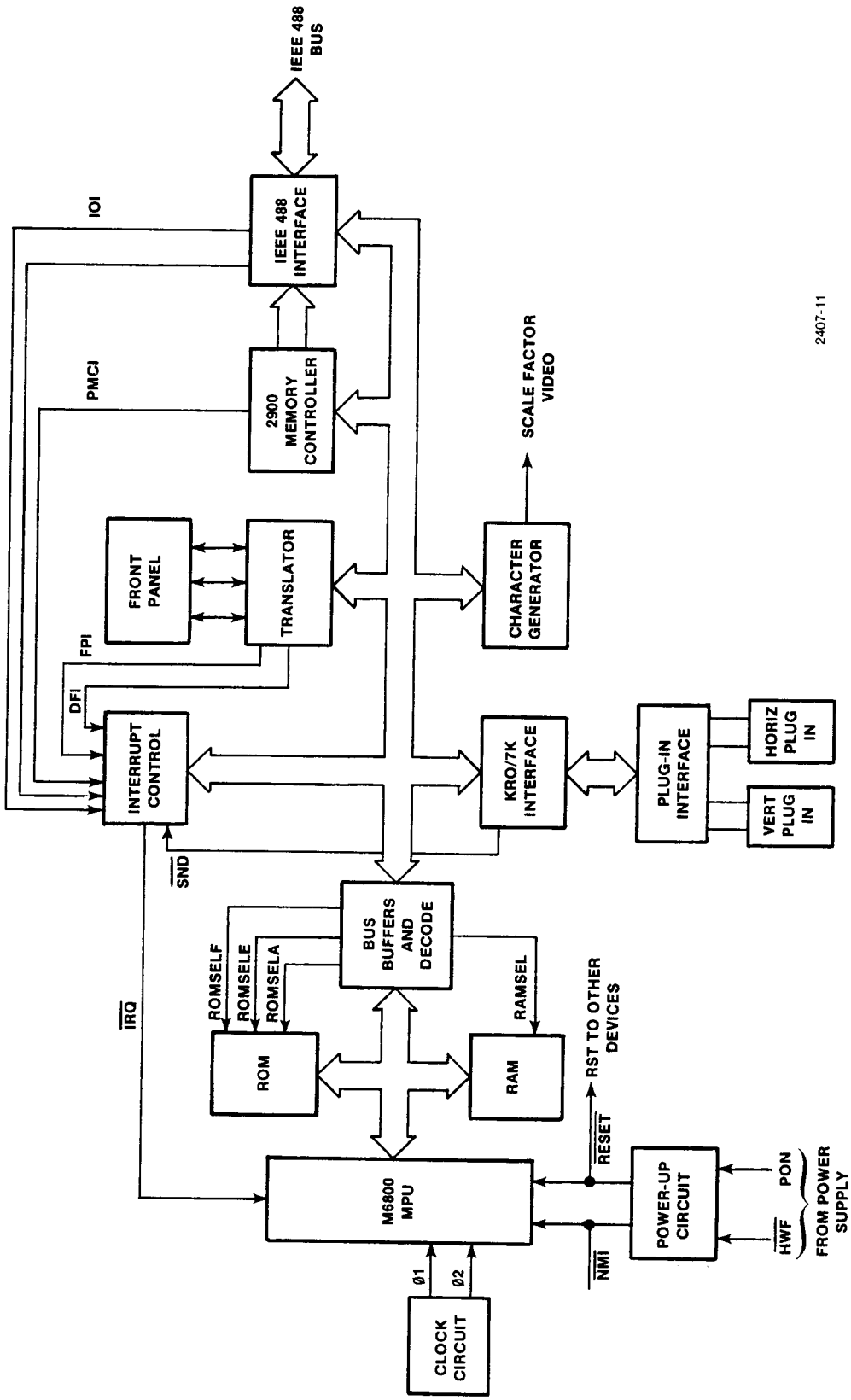


Fig. 3-11. Block diagram of the 6800 MPU system.

The firmware operating system that directs the MPU's activity is resident in 10K (1K=1024) bytes of ROM (Read-Only Memory) on the MPU Memory board (A52), and 2K of ROM on the IEEE 488 Interface. The MPU system also uses 1K bytes of RAM (Random-Access Memory) as a "scratch pad." A limited amount of the RAM space is available for diagnostic purposes.

6800 MPU Architecture

Before we discuss the microprocessor system as it is used in the 7912AD, a review of the 6800 MPU might be helpful. For more information on the 6800, refer to the Motorola M6800 Microcomputer Design Data Manual. Figure 3-12 shows a block diagram of the 6800 internal architecture. The 6800 is an 8-bit parallel processor with an 8-bit bidirectional data bus and a 16-bit address bus. The MPU consists of the following functional units:

Two 8-bit Accumulators
Program Counter
Stack Pointer
Index Register
Condition Code Register
Arithmetic Logic Unit (ALU)
Instruction Register and Decoder/Timing
Data and Address Buffers

Accumulators. The accumulators are used to hold operands and the results of ALU operations.

Condition Code Register. The condition code register indicates the results of ALU operations. Single bits in the register indicate a negative result (N), a zero result (Z), and overflow (V), carry from bit 7 (C), and half carry from bit 3 (H). These bits are used by the conditional branch instructions in the MPU instruction set. Bit 4 of the condition code register masks the MPU's $\overline{IRQ}$ input. When set, the MPU ignores interrupts on the $\overline{IRQ}$ input. Unused bits (6 and 7) in the register are ones.

Program Counter. The program counter register contains a 16-bit address that points to the current program instruction.

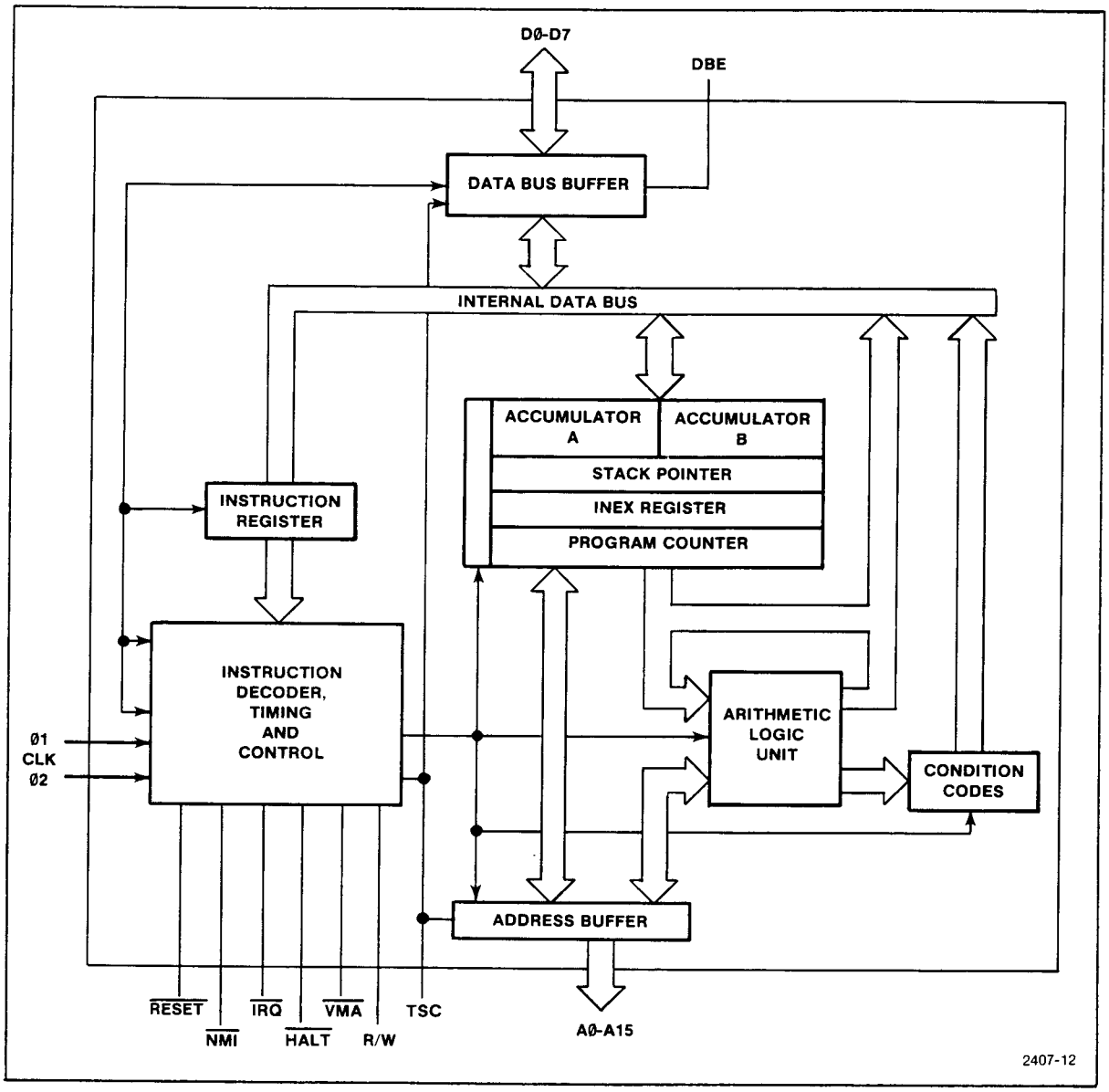


Fig. 3-12. Block diagram of the 6800 internal architecture.

Stack Pointer. The stack pointer is a 16-bit address that points to the next available memory location in the external LIFO (Last-In-First-Out) "stack." This stack is used to store the contents of the MPU registers when an interrupt occurs or the MPU executes a subroutine. The stack is usually located at the highest RAM memory address and it grows toward lower memory addresses as data is added to it. The stack pointer is automatically decremented when data is "pushed" onto the stack and incremented when data is "popped" off.

Index Register. The index register can be used to store 16-bit data or an address used in the indexed mode of memory addressing. Instructions are provided in the 6800 instruction set that load, increment, decrement, compare, etc. the index register.

Instruction Register and Decoder/Timing. During an instruction fetch (the first one, two, or three machine cycles, depending on the instruction), successive bytes of an instruction are loaded from the program memory into the instruction register. The contents of this register are, in turn, passed to the decoder and timing logic which decodes the byte(s) and generates the machine states and control signals necessary to execute the instruction. The timing and control block also generates and receives the external control signals.

Data and Address Buffers. These three-state buffers isolate the 6800 internal busses from the external data and address busses. The data bus buffer is bidirectional.

The Instruction Cycle

The 6800 is driven by a two-phase non-overlapping clock. A machine cycle is defined as the interval between two successive positive-going transitions of the phase-one clock signal. An instruction cycle consists of from 2 to 12 machine cycles required to fetch and execute the instruction. The number of machine cycles required depends on the instruction and addressing mode. For more information on these cycles refer to the Motorola M6800 Microcomputer Design Data Manual.

MPU Control Signals

Clock Phase One and Phase Two (Θ1,Θ2). The two-phase TTL-level clock signals are applied to these inputs.

HALT. When asserted, this input causes the 6800 to halt all activity when the current instruction execution is complete. The HALT input is unused in the 7912AD system.

Three-State Control (TSC). The TSC input causes the 6800 address bus and Read/Write line to go to the high-impedance state. The input is tied low (unasserted) in the 7912AD.

Read/Write (R/W). This output tells the peripheral and memory devices on the MPU bus whether the processor is reading from the data bus (R/W line high) or writing data onto the bus (R/W line low). The standby state of the line is high (reading).

Valid Memory Address (VMA). The VMA output is asserted (high) when the MPU has a valid address on the bus. When VMA is asserted, the memory and peripherals decode the address to determine if it is theirs. In the 7912AD, VMA enables the Address Decoding Logic to generate the select signals.

Data Bus Enable (DBE). This input is the three-state control signal for the MPU data bus. The 6800 bus drivers are enabled when DBE is high. This input is normally tied to the phase-2 clock signal.

Figure 3-13 shows read- and write-cycle timing on the 6800 system bus and the relationship of these control signals to the cycles.

Interrupt Request ($\overline{\text{IRQ}}$). When asserted, this input requests an interrupt sequence in the 6800. The processor completes its current instruction before recognizing the interrupt. Then it tests the interrupt mask bit in the condition code register. If it is set, the interrupt is ignored, otherwise, the following sequence is executed:

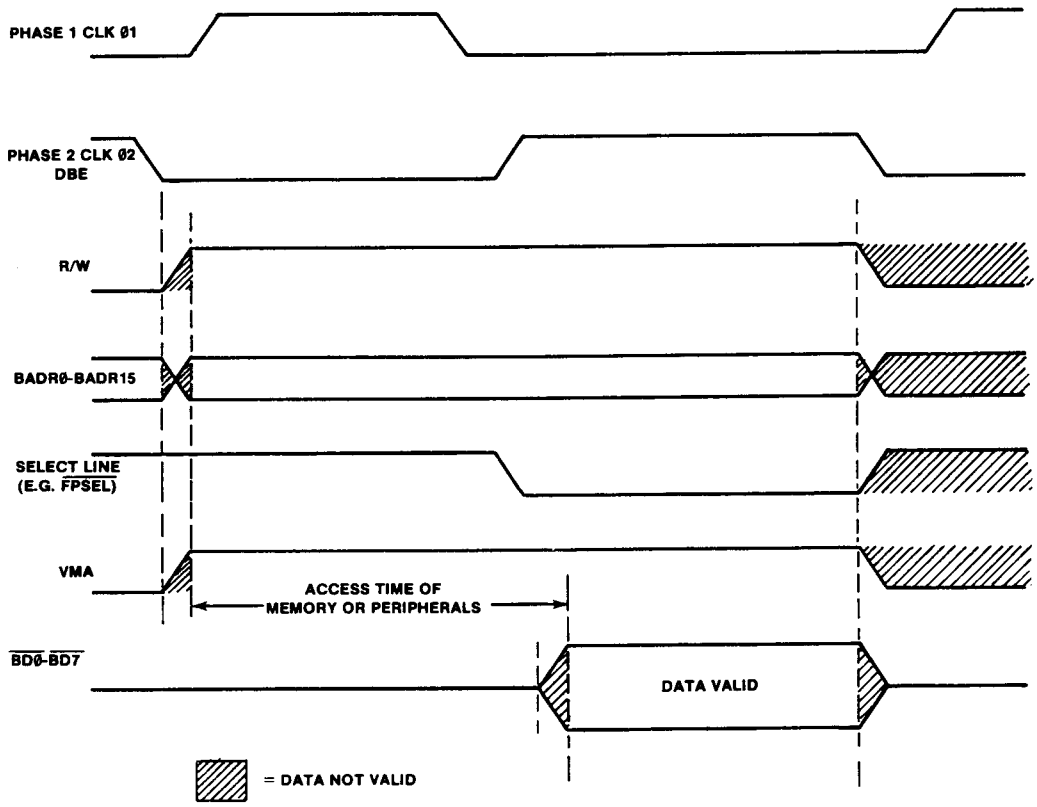
1. Push the contents of the program counter, index register, accumulators, and condition code register onto the stack, decrementing the stack pointer for each byte stored.

2. Set the interrupt mask bit and load the address stored at FFF8 and FFF9 (7FF8 and 7FF9 in the 7912AD, since bit 15 of the address bus (A15) is unused).

3. Execute the interrupt service routine that begins at the address stored at FFF8 and FFF9 (7FF8 and 7FF9 in the 7912AD).

4. At the end of the interrupt routine, return to the interrupted task by retrieving the previous register contents from the stack.

External devices are wire-ORed to the $\overline{\text{IRQ}}$ input. Since multiple devices are connected, the service routine must determine which device generated the interrupt and take appropriate action.



(a) Read cycle timing on the 6800 bus.

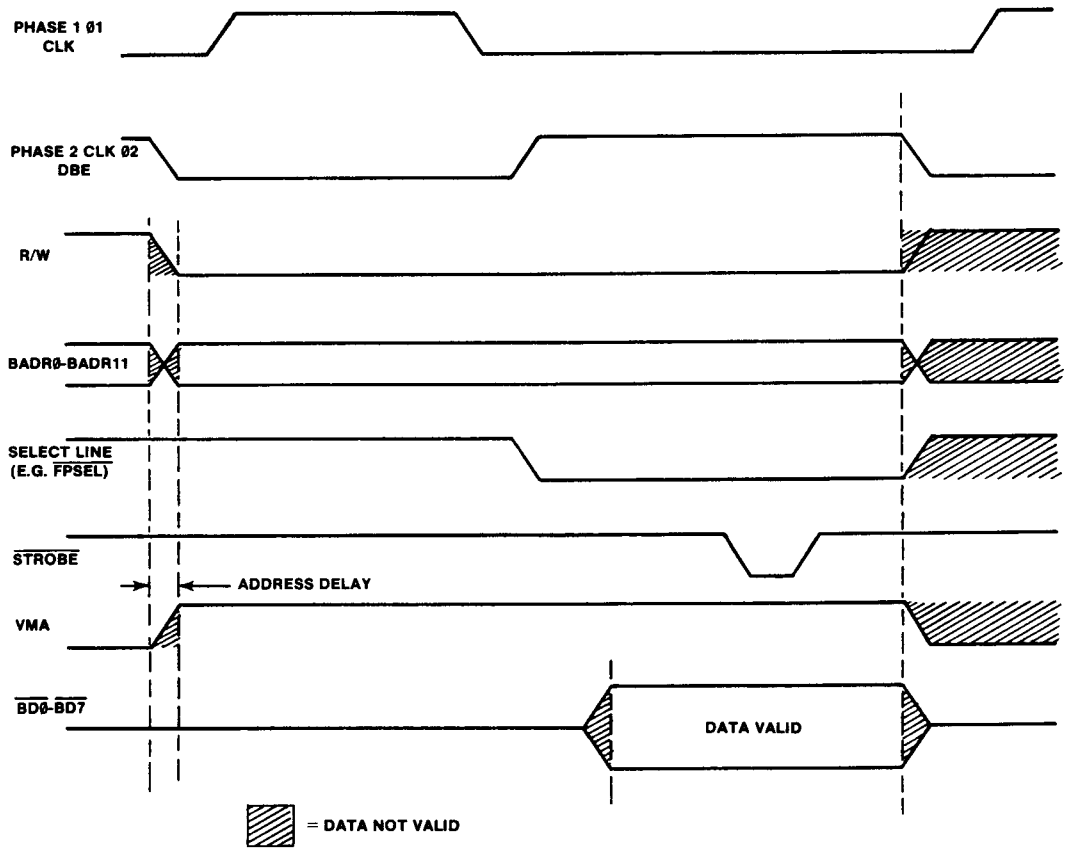


Fig. 3-13. (b) Write cycle timing on the 6800 bus.

Non-Maskable Interrupt ($\overline{\text{NMI}}$). A negative-going transition on this input causes the processor to execute an interrupt sequence as just discussed. The $\overline{\text{NMI}}$ input differs from the $\overline{\text{IRQ}}$ input in two ways: First, the interrupt mask bit has no effect on the $\overline{\text{NMI}}$ input and second, the pointer address (called a vector) to the $\overline{\text{NMI}}$ interrupt routine is stored at FFFC and FFFD (7FFC and 7FFD in the 7912AD).

RESET. This input is used to reset and start the MPU on power-up or on initialization of the processor. When RESET is asserted, the processor begins executing the initialization routine at the address stored in vector FFFE and FFFF (7FFE and 7FFF in the 7912AD). The interrupt mask bit is set during the initialization routine to prevent the processor from servicing interrupts before being initialized. The RESET input must be held low for at least eight clock periods after the 5.1-volt power supply reaches 4.75 volts.

Table 3-1 shows the interrupt vectors for the RESET, $\overline{\text{NMI}}$, and $\overline{\text{IRQ}}$ interrupts. An additional interrupt vector, the software interrupt vector, is also shown. This vector is used when an interrupt is generated by the program running on the 6800.

TABLE 3-1

6800 INTERRUPT VECTORS

Vector		Interrupt
High Byte	Low Byte	Type
7FFE	7FFF	Reset
7FFC	7FFD	Non-Maskable Interrupt
7FFA	7FFB	Software Interrupt
7FF8	7FF9	Interrupt Request

Figure 3-14 shows the MPU's main decision paths when it is executing a program.

NOTE

All addresses are in hexadecimal unless otherwise noted.

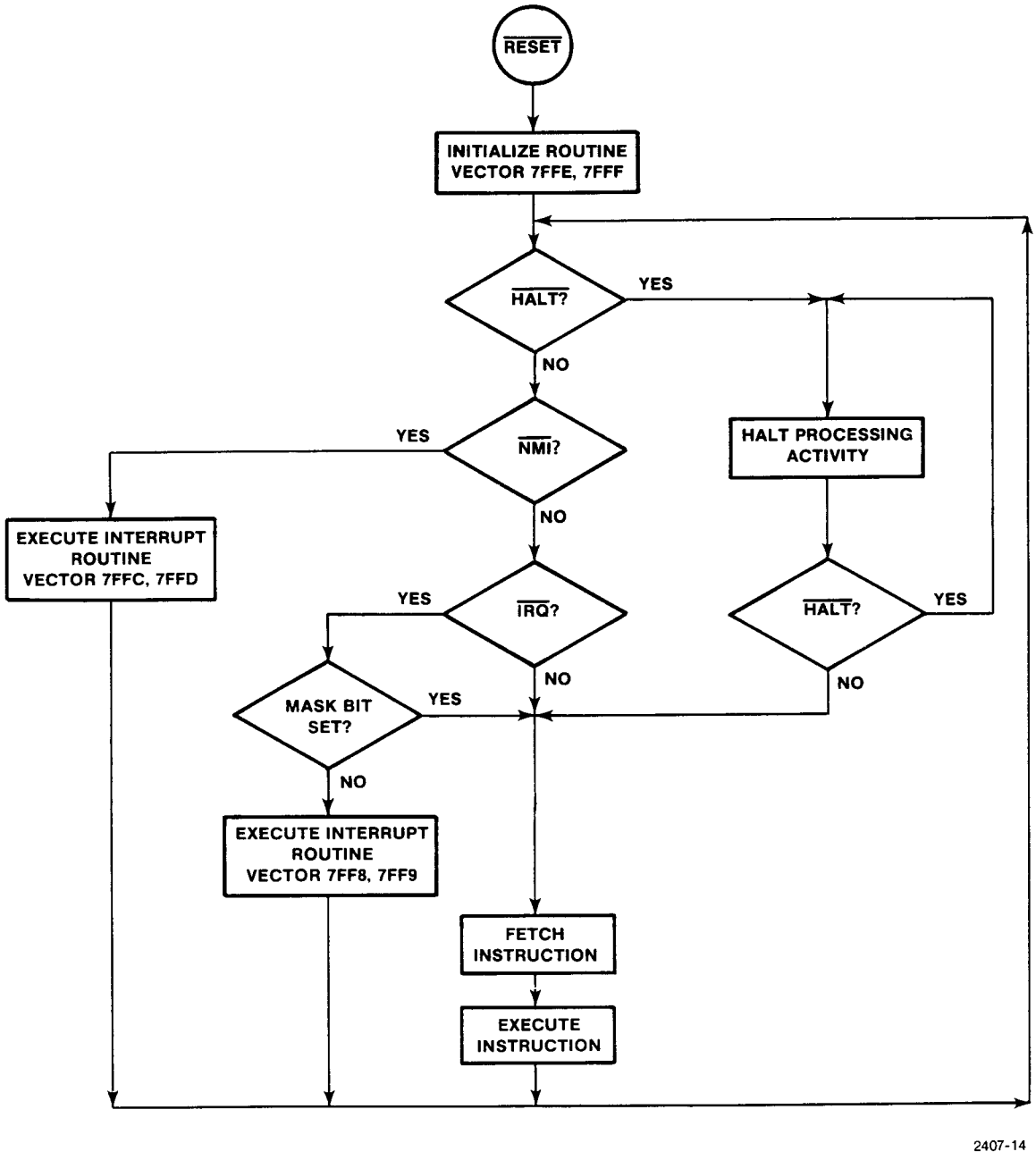


Fig. 3-14. Flow chart of the 6800's main decision paths.

The 6800 Bus

The 6800 communicates with the program memory (ROM), RAM, and the instrument functions it controls through a 15-bit address bus, an 8-bit data bus, and a set of device select lines. The 6800 bus, bus drivers, and decoders are shown on diagram 15.

The 15-bit address bus allows the MPU to address 32K (8000 hex) unique locations including ROM, RAM, and instrument control/status registers. Figure 3-15 shows a map of the 6800 address space. Each of the functions controlled by the 6800 is addressed by the low-order 11 bits of the address bus and one or more select signals derived from A10-A14. For example, to address a location in ROM bank A, the MPU asserts the address of the location (in the range of 2000 to 2FFF) on A0-A14. After a short address settling time, the MPU asserts VMA. The reset signal, RST, is high and during the phase-2 clock period, pins 4 and 5 of U132 (center of diagram 15) are low, enabling the decoder. U132 decodes A12-A14 and asserts pin 13 ($\overline{\text{ROMSELA}}$), enabling ROM bank A to be addressed by A0-A11. The low order bits (A0-A11) select the individual location within ROM bank A. The other ROM banks, RAM, and instrument control registers are addressed in a similar manner where U132 and U234A decode the 5 high-order bits of the address bus (A10-A14) to generate the select signals. Table 3-2 shows the functions selected by each of these signals.

TABLE 3-2

6800 BUS SELECT SIGNALS

SIGNAL NAME	LOWEST ADDRESS	FUNCTION SELECTED
$\overline{\text{FPSEL}}$	5000	Character Generator
$\overline{\text{INTSEL}}$	3C00	6800 Interrupt Control
$\overline{\text{IOSEL}}$	4000	IEEE 488 Interface
$\overline{\text{PISEL}}$	3800	KRO/7K Bus Interface
$\overline{\text{PMCSEL}}$	3400	2900 Memory Controller
$\overline{\text{RAMSEL}}$	0000	MPU RAM Memory
$\overline{\text{ROMSELA}}$	2000	ROM Bank A
$\overline{\text{ROMSELE}}$	6000	ROM Bank E
$\overline{\text{ROMSELF}}$	7000	ROM Bank F
$\overline{\text{TLTRSEL}}$	3000	Translator

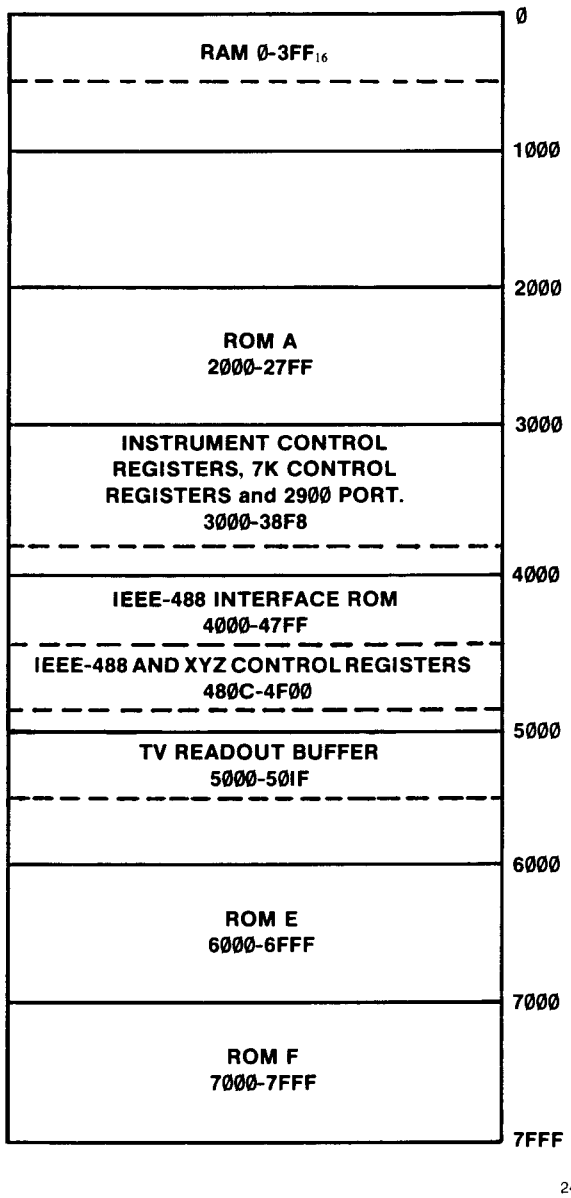


Fig. 3-15. Address map of the 6800 system.

Bus Buffers

U322, U332, and U334 (top-right of diagram 15) comprise the address bus buffer for the 6800 system bus. The enable inputs (pins 1 and 15 of each buffer) are tied to ground, so the buffers are always enabled. This buffer also drives the $\overline{\text{WRITE}}$ and $\overline{\text{STROBE}}$ lines. The $\overline{\text{STROBE}}$ pulse occurs at the center of each phase-2 clock period. This pulse tells devices that the address on the bus is valid and initiates data transfer to or from the selected device. The $\overline{\text{WRITE}}$ line is driven by the MPU R/W output. When $\overline{\text{WRITE}}$ is asserted, the MPU is writing data to the bus. When the MPU is reading data, $\overline{\text{WRITE}}$ is high. The R/W line also controls the 6800 data bus buffers, U312 and U314 (top-center of diagram 15). When R/W is low, the output of U402B is high and the output of U206C is low, enabling the buffer output drivers. If the MPU is reading data from the bus, R/W is high and the buffer receivers are enabled.

The MPU memory (ROM and RAM) and part of the interface to the 7K plug-in bus are connected directly to the MPU data bus, ahead of the bus buffer. When the MPU addresses these devices, the bus buffer is enabled for output to drive diagnostic connector P514 (diagram 16). This connector is provided to facilitate connecting a logic analyzer to the 6800 bus. If, for example, the MPU addresses the memory, ANSR (pin 4 of U402B) is asserted and the data bus output drivers are enabled.

MPU Clock Circuit

The 6800 system clock is derived from an 80 MHz master clock on the Data Buffer board (A20). The clock signal is divided down to 10 MHz on the data buffer board and fed to the MPU clock circuit in the bottom-left of diagram 15. The 10 MHz clock drives the clock input of a 4-bit binary counter (U032). This clock signal is also inverted by U012D and the inverted signal drives three flip-flops (U102A, U001A and U001B). The outputs of the 4-bit counter go to a 4-to-16 line decoder (U022). This decoder asserts one of its 16 outputs (five outputs are used in this circuit) for each of the counter's states. The outputs of the decoder drive the inputs of the three flip-flops.

Refer to Fig. 3-16 as we discuss the operation of the Clock circuit. Assume that the 4-bit counter is cleared (set to zero). U022 decodes the counter's outputs and asserts pin 1. The output of U012A goes high and on the falling edge of the inverted clock, the $\overline{\text{Q}}$ output of U001A goes low. This output stays low until the fifth 10 MHz clock pulse. At that time,

the counter's outputs are set to a binary five (0101) and the decoder asserts pin 6. As a result, the K input of U001A goes high and on the next clock, the $\overline{Q}$ output goes high. On the sixth clock pulse, the output of U001B goes low and stays low until the 13th pulse. On the rising edge of the 13th pulse, pin 15 of U022 goes low, clearing the counter and starting the process over again. The result is a two-phase non-overlapping clock with a period of about 1.4 microseconds.

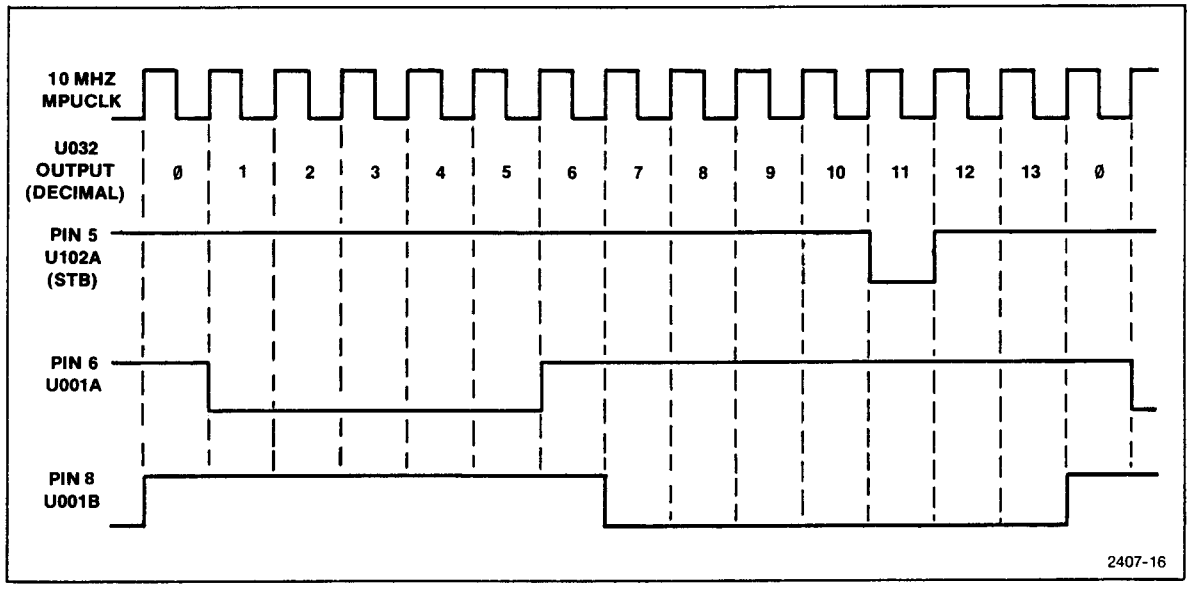


Fig. 3-16. Timing of the 6800 clock circuit.

The outputs of the two flip-flops are fed to the inverter/driver circuits formed by Q212, Q218, U114D, and U114E. Q212 and Q218 are active pull-ups for open collector inverters U114E and U114D. On the falling edge of the non-inverted clock, the transistor turns on, pulling the output of the inverter high very quickly. The transistor stays on just long enough to pull the inverter output up. On the rising edge of the non-inverted clock, the transistors are unaffected. This circuit improves the rise time of clock pulses to meet the 6800 clock pulse specifications.

The clock circuit also generates the $\overline{STB}$ (Strobe) pulse previously discussed. When the 4-bit counter, U032, counts to ten, pin 11 of U022 is asserted. On the rising edge of the next clock, the Q output of U102A

goes low, asserting $\overline{STB}$. On count 11, pin 11 of U022 goes high and the output of U102A is unasserted on the 12th clock. The result is a 100 nanosecond pulse near the middle of each phase-2 clock period. See Fig. 3-16.

Reset Circuit

When power is applied to the 7912AD, the reset circuit shown at the left-center of diagram 15 asserts the 6800's $\overline{RESET}$ input, forcing it to execute the initialize and self-test routines that begin at the address stored in 7FFE and 7FFF.

When the 5.1-volt power supply comes up, U102B is cleared by the RC network of R106, C106, and CR106. The Q output of U102B is low, so the output of U402A is high and $\overline{RST}$ is asserted. The low on $\overline{RST}$ (Reset) holds the 6800 in an idle state until PON makes a low-to-high transition to indicate that the power supplies are stable. During the delay while the power supplies stabilize, C106 charges through R106 and the clear input of U102B goes high (unasserted). The positive-going transition on PON clocks the Q output of U102B high, and fires U204A. The low on U204A's Q output hold $\overline{RST}$ low through U402A. About 14 microseconds later, U204A times out, $\overline{RST}$ goes high, and the 6800 begins executing the initialization and self-test routines.

The $\overline{RST}$ line also resets logic circuits in the Readout/7K Interface.

Power Fail and Hardware Failure Interrupts

If any of the 7912AD's analog power supplies fall out of tolerance, $\overline{HWF}$ (Hardware Failure) goes low. If the line input power is interrupted, PON goes low. In either case, the output of U206A goes high. If NMIEN (Non-Maskable Interrupt Enable) is high, U206B goes low, generating a non-maskable interrupt to the 6800. The NMIEN line is held low (interrupts disabled) during the power-up routine and set high after power-up and self-test are complete.

MPU Memory

The MPU Memory board (A52 - diagram 18) contains 6800 system ROM, RAM, and buffers.

U220 and U240 form a bidirectional data bus buffer. When the 6800 R/W line is low (6800 writing data to memory), the output of U210C is low and the buffer is enabled for input to the memory. If R/W is high (6800 reading data from memory) and any of the $\overline{\text{RAMSEL}}$ or $\overline{\text{ROMSEL}}$ lines are asserted, the output of U210B is low and the buffer is enabled for output from the memory. U330, U332, and U340 comprise a 12-bit address bus buffer.

RAM Memory. Eight 256 X 4-bit RAM packages and select logic comprise the 6800 RAM memory. The chips are arranged in four pairs, each containing 256 8-bit bytes. When $\overline{\text{RAMSEL}}$ is asserted, U530B decodes bits 8 and 9 of the address bus to select one of the four pairs of memory chips. The lowest address of each pair is shown above the select lines on diagram 18. The low-order 8-bits select the individual memory locations in the selected devices.

ROM Memory. The 7912AD's firmware operating system is resident in 10 1K X 8-bit ROM's (Read-Only Memory). Each of these chips is selected by one of the $\overline{\text{ROMSEL}}$ lines and bits 10 and 11 of the address bus as just discussed. When any of the $\overline{\text{ROMSEL}}$ lines is asserted, the output of U440B goes low, enabling ROM data buffer U230 (bottom center of diagram 18).

The firmware that controls the IEEE 488 Interface resides in a single 2K X 8-bit ROM on the IEEE 488 Interface board (A56).

Interrupt Control Logic

The Interrupt Control Logic, shown on diagram 16, consists of two Interrupt Occurred Registers, U712 and U524, and two Interrupt Mask Registers, U728 and U732. This control logic receives interrupt signals from instrument functions controlled by the 6800. These interrupt signals are ORed together through the Interrupt Mask Registers to drive the $\overline{\text{IRQ}}$ input of the 6800.

Interrupt Occurred Registers (U712 and U524).

U524	R-REN	X	X	X	X	X	X	X	3C00 (Read only)
Bit	7	6	5	4	3	2	1	0	
U712	IOI	DFI	PMCI	X	FPI	X	X	SND	3C02 (Read only)

3C00 Bit 0-6: Unused.

3C00 Bit 7 - R-REN: When set, this bit indicates that $\overline{\text{REN}}$ has gone false.

3C02 Bit 0-SND: When set, this bit indicates that a $\overline{\text{SND}}$ interrupt from the 7K interface has occurred.

3C02 Bit 1,2: Unused.

3C02 Bit 3 - FPI: When set, a front-panel interrupt has occurred.

3C02 Bit 4: Unused.

3C02 Bit 5 - PMCI: When set, the 2900 memory controller has interrupted the MPU.

3C02 Bit 6 - DFI: When set, a duty factor interrupt has occurred.

3C02 Bit 7 - IOI: Set when an I/O interrupt from the IEEE 488 interface has occurred.

When an interrupt occurs, a corresponding bit in one of the Interrupt Occurred Registers is set (set to logic one). If the interrupt is not masked, the $\overline{\text{IRQ}}$ line is asserted, interrupting the MPU. As part of its interrupt service routine, the 6800 reads the Interrupt Occurred Registers to determine the source of the interrupt. If any set bits are found, the MPU jumps to a service routine for the highest priority interrupt. If no set bit is found, the MPU returns to its previous task, and if the instrument is strapped for diagnostic mode, an unrecognized interrupt is reported.

All interrupts except $\overline{\text{SND}}$ and $\overline{\text{R-REN}}$ remain asserted until the 6800 clears them as part of the service routine. U702B latches the SND interrupt. The positive transition at the end of $\overline{\text{SND}}$ clocks U702B and its

Q output goes high. This sets bit 0 of the Interrupt Occurred Register. The interrupt latched by U702A is unused. The 6800 clears U702A and U702B by writing to address 3C02. U234B (bottom-center of diagram 16) decodes the address and asserts $\overline{IA2}$. When $\overline{IA2}$ and $\overline{WRITE}$ are asserted, the output of U514A (left-center o the diagram) goes low. The MPU can selectively clear U702A or U702B by asserting $\overline{BD1}$ or $\overline{BD0}$ respectively. When $\overline{BD0}$ is low, the output of U606D goes low, clearing U702B and resetting the $\overline{SND}$ interrupt.

Interrupt Mask Registers (U728 and U732).

U732	R-REN	X	X	X	X	X	X	X	3C01 (Write only)
Bit	7	6	5	4	3	2	1	0	
U728	IOI	DFI	PMCI	X	FPI	X	X	SND	3C03 (Write only)

3C01 Bit 0-6: Unused.

3C01 Bit 7 - R-REN: When set, this bit masks $\overline{REN}$ interrupts.

3C03 Bit 0 - SND: When this bit is set, $\overline{SND}$ interrupts are masked.

3C03 Bit 1,2: Unused.

3C03 Bit 3 - FPI: When set, front-panel interrupts are masked.

3C03 Bit 4: Unused.

3C03 Bit 5 - PMCI: When set, this bit masks memory controller interrupts.

3C03 Bit 6 - DFI: When cleared, duty factor interrupts are masked.

3C03 Bit 7 - IOI: When cleared, I/O interrupts are disabled.

The 6800 can mask (disable) $\overline{IRQ}$ interrupts in two ways. All $\overline{IRQ}$ interrupts can be internally masked by setting a bit in the MPU's condition code register. If this bit is set, the Interrupt Control Logic passes interrupts as usual but the 6800 ignores its $\overline{IRQ}$ input. The 7912AD firmware operating system sets this interrupt mask bit while the 6800 is executing the power-up routine. The mask is also set when routines are being executed that should not be interrupted, such as adjusting the main intensity value.

Interrupts may also be individually masked by setting the appropriate bit(s) in the Interrupt Mask Registers. For example, to mask the I/O interrupt from the IEEE 488 interface (IOI), the 6800 writes to 3C03. U234B decodes the address and asserts $\overline{IA3}$. When $\overline{IA3}$ and $\overline{WRITE}$ are asserted, the output of U514C goes low. The byte on $\overline{BD0}$-$\overline{BD7}$ is latched on the positive transition at the end of the $\overline{WRITE}$ cycle. To mask IOI, the 6800 holds $\overline{BD7}$ low. This sets bit 7 of U728 and pin 6 goes low. As a result, the output of U614B goes high and IOI interrupts are disabled.

U732 masks the $\overline{REN}$ interrupt. This register's address is 3C01.

Readout System Block Diagram

The Readout System acquires the scale factor readout data from programmable or non-programmable plug-ins with readout capability. The 6800 reads the data from the analog decoder, converts it to ASCII and writes the ASCII characters out to the character generator for display on the TV monitor. A block diagram of the Readout System is shown in Fig. 3-17.

Introduction to the Scale Factor Readout System

The Scale Factor Readout System displays the scale factor information encoded by the plug-ins. The 7912AD can acquire the scale factor information from any combination of programmable or non-programmable plug-ins with readout capability. The scale factor information is mixed with the video output signals and displayed on the TV monitor. Scale factors are not displayed on the XYZ monitor.

Several terms must be defined before we discuss the readout system in detail. The definitions of these terms follow:

Character -- A character is a single number, letter or symbol displayed on the TV monitor, either alone or in combination with other characters.

Word -- A word is made up of a related group of characters. In the 7912AD readout system, a word can consist of up to eight characters.

Frame -- A frame is a display of all words for a given operating mode and plug-in combination. Up to four words can be displayed in one frame. Figure 3-18 shows the position of each word in a complete frame.

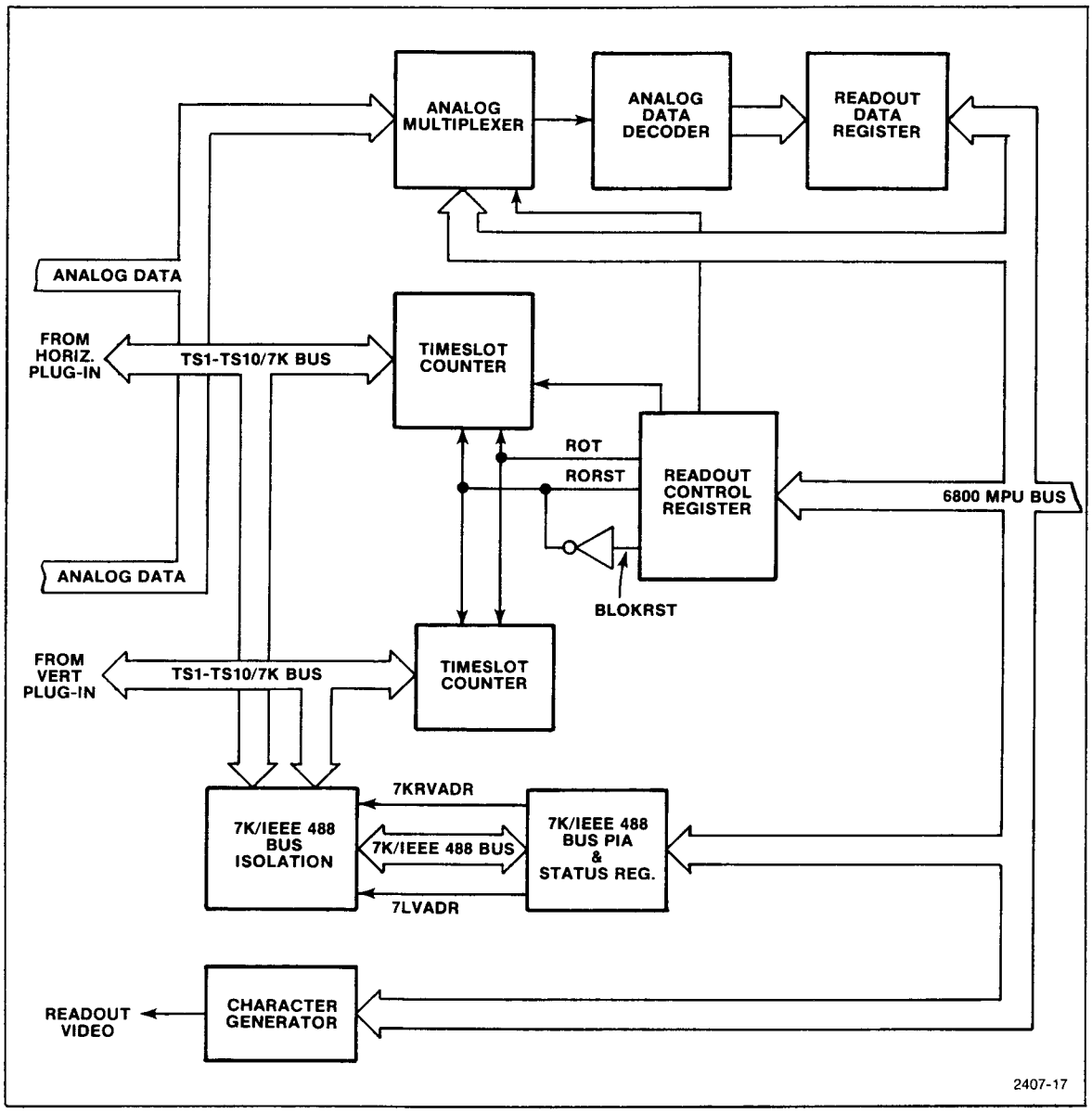


Fig. 3-17. Block diagram of the readout system.

Column -- One of the vertical lines in the character selection matrix (see Fig. 3-19).

Row -- One of the horizontal lines in the character selection matrix.

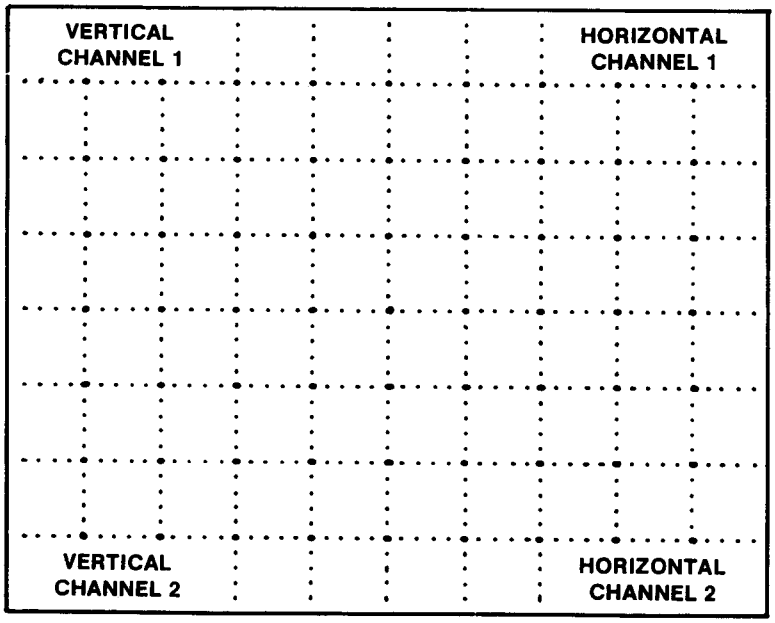


Fig. 3-18. Position of the readout words on the TV display.

Time-slot -- A location in a pulse train. In the 7912AD system, the pulse train consists of ten negative-going pulses. Each time-slot pulse is assigned a number between one and ten. For example, the first time-slot is TS1.

Time Multiplexing -- Transmission of data from two or more sources over a common path by using different time-intervals for different signals.

Display Format. The 7912AD can display up to four words of scale factor readout information on the TV monitor. The readout for each channel of each plug-in is displayed in a fixed location as shown in Fig. 3-18. For example, channel 1 of an amplifier in the VERTICAL compartment is displayed in the upper-left of the monitor screen as shown.

Each word in the readout display can display up to eight characters, although the typical display will contain between two and seven characters per word. The characters are selected from the character selection matrix in Fig. 3-19.

ROW NUMBER \ COLUMN NUMBER →	CURRENT (MILLI-AMPERES)	C-0	C-1	C-2	C-3	C-4	C-5	C-6	C-7	C-8	C-9	C-10
		0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	> 1.0
R-1	0	SKIP[a]	0	1	2	3	4	5	6	7	8	9
R-2	0.1		–	<	I	/	+	–	+	C	=	>
R-3	0.2		ADD[a] ONE ZERO	ADD[a] TWO ZEROS	SHIFT[a] PREFIX ←	SHIFT[a] PREFIX ← AND ADD ONE ZERO						IDENTIFY[a]
R-4	0.3		m	μ	n	p	X	K	M	G	T	R
R-5	0.4		S	V	A	W	H	d	B	c	Ω	E
R-6	0.5		U	N	L	Z	Y	P	F	J	Q	D
R-7	0.6				DECIMAL[a] POINT LOCATION NO. 3	DECIMAL[a] POINT LOCATION NO. 4	DECIMAL[a] POINT LOCATION NO. 5	DECIMAL[a] POINT LOCATION NO. 6	DECIMAL[a] POINT LOCATION NO. 7			
R-8	0.7										DECIMAL[b] POINT	
R-9	0.8											
R-10	0.9	ADD SPACE IN DISPLAY[a]										

UNUSED LOCATIONS. AVAILABLE FOR FUTURE EXPANSION OF READOUT SYSTEM

[a]OPERATIONAL ADDRESS.

[b]DECIMAL POINT CHARACTER. SEE DECIMAL POINT CHARACTER DESCRIPTION IN TEXT.

1195-25

Fig. 3-19. The character selection matrix.

The 7000-Series Readout System. Each character in the readout word is encoded by the plug-in and sent to the mainframe in the form of two analog current levels (row and column current). These current levels usually range from zero to 1 milliamp in 100 microamp steps (in some cases the currents may exceed 1 milliamp). The current level on these lines defines a particular character in the selection matrix. For example, 300 microamps of column current and 0 microamps of row current selects the character 2 from the character selection matrix. A complete display word is formed by time-multiplexing ten row and column current levels, one during each of ten time-slots. The data encoded on the row and column lines is assigned a particular meaning during each time-slot. For example, data on the lines during time-slots 9 and 10 defines the units of measurement (e.g., V=volts, S=seconds, etc.). Table 3-3 shows the standard readout format.

TABLE 3-3

STANDARD READOUT FORMAT

Time Slot Number	Description
TS-1	Determines the decimal magnitude (number of zeroes displayed or prefix change information) or the IDENTIFY function. (No display during this time-slot.)
TS-2	Indicates normal or inverted input (no display for normal input).
TS-3	Indicates calibrated or uncalibrated condition of plug-in variable control. (No display for calibrated condition.)
TS-4	1-2-5 scaling.
TS-5 TS-6 TS-7	Not encoded by plug-in. Left blank to allow addition of zeroes by Readout System.
TS-8	Defines the prefix which modifies the units of measurement.
TS-9 TS-10	Defines the units of measurement of the plug-in unit. May be standard units of measurement (V,A,S, etc.) or special units selected from the character selection matrix.

A set of pulses, called time-slot pulses, synchronize the plug-in and mainframe readout systems. In non-programmable plug-ins, the time-slot pulses are sent to the plug-in on ten time-slot lines (TS1-TS10). Table 3-4 shows the time-slot numbers and their corresponding pin numbers on the plug-in edge connector.

TABLE 3-4

TIME SLOT/DATA LINES

Pin Number	Standard Plug-In/ Programmable Plug-In
A29	TS10/TSCLOCK
B29	TS9/DI08
A30	TS8/DI07
B30	TS7/DI05
A31	TS6/DI05
B31	TS5/DI04
A32	TS4/DI03
B32	TS3/DI02
A33	TS2/DI01
B33	TS1/TS1

These lines are pulled to -15 volts sequentially so that each line goes low during the corresponding time-slot. The analog row and column currents are usually encoded by connecting resistors between the time-slot lines and the row and column lines. The row and column lines are virtual grounds, so the current in the lines is simply the time-slot voltage (-15 volts) divided by the value of the resistor. As a result, the analog currents that define the readout word are time-multiplexed on the row and column lines as shown in Fig. 3-20. The mainframe demultiplexes and decodes these analog currents and generates the display on the CRT.

The readout system implemented in programmable plug-ins is essentially the same except that eight of the ten time-slot lines (TS2-TS9) are used for the 7K data bus. The time-slot pulses are summed and transmitted to the plug-in as a serial train of pulses on TS10. TS1 is asserted during time-slot 1 to synchronize the plug-in and mainframe time-slot counters. Analog data is time-multiplexed and sent to the mainframe on the row and column lines as previously discussed.

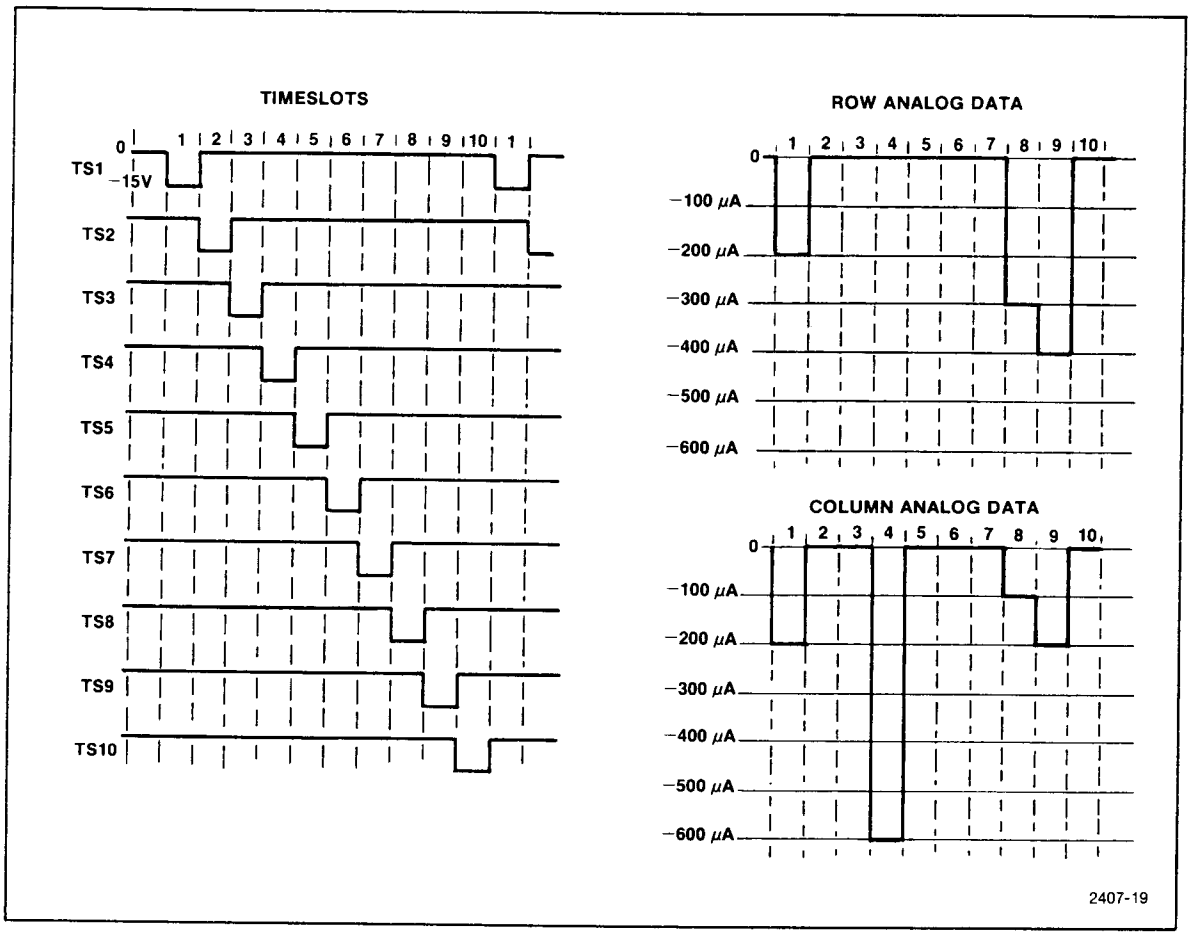


Fig. 3-20. Timing of the multiplexed analog data.

Readout Acquisition

Diagrams 3 and 17 show the readout acquisition system in the 7912AD. The acquisition system consists of four main parts -- the Readout Control Register, the Time-Slot Generator, the Analog Data Multiplexer, and the Analog Data Decoder. The 6800 MPU controls the Time-Slot Generator and Analog Data Multiplexer and reads the 4-bit output word from the Analog Data Decoder.

Readout Control Register. The Readout Control Register (U832, bottom-left of diagram 17) is the port through which the 6800 controls the Time-Slot Generator. The register's address is 38DF (HEX) on the 6800 bus. Table 3-5 shows the name and function of each bit in the register. The non-maskable interrupt enable bit (NMIEN) is not part of the readout system.

TABLE 3-5

READOUT CONTROL REGISTER BITS

Bit	Signal Name	Function
4-7	-	unused
3	NMIEN	1 = enable 6800 NMI
2	ROT	1 = assert next time-slot
1	RORST	1 = reset time-slot generator to TS-10
0	BLOKRST	1 = block reset (hold RORST low)

Time-Slot Generator. The Time-Slot Generator transmits the time-slot pulses to the plug-ins under control of the 6800. Any combination of programmable and non-programmable plug-ins may be installed, so the Time-Slot Generator must be able to detect the plug-in type and send parallel time-slot pulses to non-programmables and serial pulses on TS-10 to programmables.

NOTE

For instruments with Serial Number B100837 and up, see diagram 3 (SN B100837 & Up) in VOL II, for revised circuit number designations.

The control signals from the Readout Control Register drive two decade time-slot counters (U822 and U728 at the center of diagram 3). Programmable plug-ins source at least 100 microamps into TS-10 to continuously reset the counter to TS-10, forcing it to sum all time-slot pulses in a serial stream on TS-10. Table 3-6 shows the control signal sequence and the resultant states of the time-slot counter for both programmable and non-programmable plug-ins. Refer to this table as we go through the counter states. The time-slot counter states are indicated with a number from one to ten to indicate the time-slot number, and an A or N to indicate whether the time-slot line is Asserted or Not asserted. For example, in state 6 non-programmable plug-ins have TS-2 asserted and programmables have TS-10 asserted.

TABLE 3-6

TIME-SLOT COUNTER STATES

State Number	Control Reg. Bits			Time-Slot Counter States	
	ROT	RORST	BLOKRST	Non-prog. Plug-ins	Prog. Plug-ins
0	Ø	1	Ø	1ØN	1ØN
1	Ø	Ø	Ø	1ØN	1ØN
2	Ø	Ø	1	1ØN	1ØN
3	1	Ø	1	1A	1A
4	Ø	Ø	1	1N	1N
5	Ø	Ø	Ø	1N	1ØN
6	1	Ø	Ø	2A	1ØA
7	Ø	Ø	Ø	2N	1ØN
8	1	Ø	Ø	3A	1ØA
9	Ø	Ø	Ø	3N	1ØN
10	1	Ø	Ø	4A	1ØA
11	Ø	Ø	Ø	4N	1ØN
12	1	Ø	Ø	5A	1ØA
13	Ø	Ø	Ø	5N	1ØN
14	1	Ø	Ø	6A	1ØA
15	Ø	Ø	Ø	6N	1ØN
16	1	Ø	Ø	7A	1ØA
17	Ø	Ø	Ø	7N	1ØN
18	1	Ø	Ø	8A	1ØA
19	Ø	Ø	Ø	8N	1ØN
20	1	Ø	Ø	9A	1ØA
21	Ø	Ø	Ø	9N	1ØN
22	1	Ø	Ø	1ØA	1ØA
23	Ø	Ø	Ø	1ØN	1ØN

When the cycle begins, RORST (Readout Reset - bit 1) is asserted (high), resetting the time-slot counters to TS-10. No time-slot lines are asserted in this state. When RORST goes low (state 1), the counter is released to assert TS1 on the next ROT (Readout Trigger) pulse. During state 2, bit 0 of the control register (BLOKRST) is set, turning Q728 on and holding RORST low. This prevents the current sourced to TS-10 by programmable plug-ins from resetting the time-slot counter. At state 3 ROT goes high. Since RORST (bit 1) is held low, TS-1 is asserted for both programmable and non-programmable plug-ins. TS-1 serves as the sync pulse that tells programmable plug-ins that the mainframe time-slot counter is starting a new cycle.

Shortly after ROT goes high, the output of U636D (bottom-left of diagram 17) goes low, asserting $\overline{\text{TIMESLOT}}$. The $\overline{\text{TIMESLOT}}$ pulse drives a voltage source formed by Q409, Q502, and Q504 (left-center of diagram 3). The output of this circuit supplies the voltage source for the outputs of the time-slot counters.

ROT goes low at state 4 and TS-1 is unasserted. Then bit 0 of the control register goes low, Q728 (diagram 17) turns off and RORST is allowed to float. Now the reset current from programmable plug-ins forces the time-slot counters to reset to TS-10. If a non-programmable plug-in is installed, no current is sourced on TS-10 so the counter counts up normally with each ROT pulse as shown in the table. The reset current from programmable plug-ins resets the time-slot counter between each ROT pulse, so the counter sends all the pulses on TS-10. This cycle continues as shown in the table until state 23, when the cycle is repeated and another TS-1 pulse is sent to tell the plug-in that a new cycle is beginning. The resultant pulse train for a programmable and a non-programmable plug-in is shown in Fig. 3-21.

Analog Data Multiplexer. The plug-ins return row and column current levels to the mainframe during the time-slots that define the characters in the readout word. The current levels are time-multiplexed onto four pairs of row and column lines -- one pair for each channel of the vertical and horizontal plug-ins. The Analog Data Multiplexer, under the control of the 6800, demultiplexes the analog data and feeds it to the analog data decoder. The 6800 controls the multiplexer through an 8-bit serial shift register, U812 at the top-left of diagram 3. The MPU selects one multiplexer channel by writing to the shift address (38BF) up to eight times. Each time, SHIFT is asserted and the state of $\overline{\text{BDØ}}$ is shifted into the first bit (Q_A) of the register. On each successive SHIFT, the current state of BDØ is shifted into Q_A and the previously loaded bits are shifted up toward Q_H. Table 3-7 shows the data selected by each channel of the multiplexer. $\overline{\text{BDØ}}$ is asserted (low) for only one of the eight shifts, so only one of U812's outputs is low. The low on this output forward-biases the output transistor for the selected channel. For example, if Q_A is low, the emitter-base junction of Q807 is forward biased and the analog current on this line is fed to the Analog Data Decoder. Q_B-Q_H are high, so the emitter-base junctions of the other output transistors are reverse-biased.

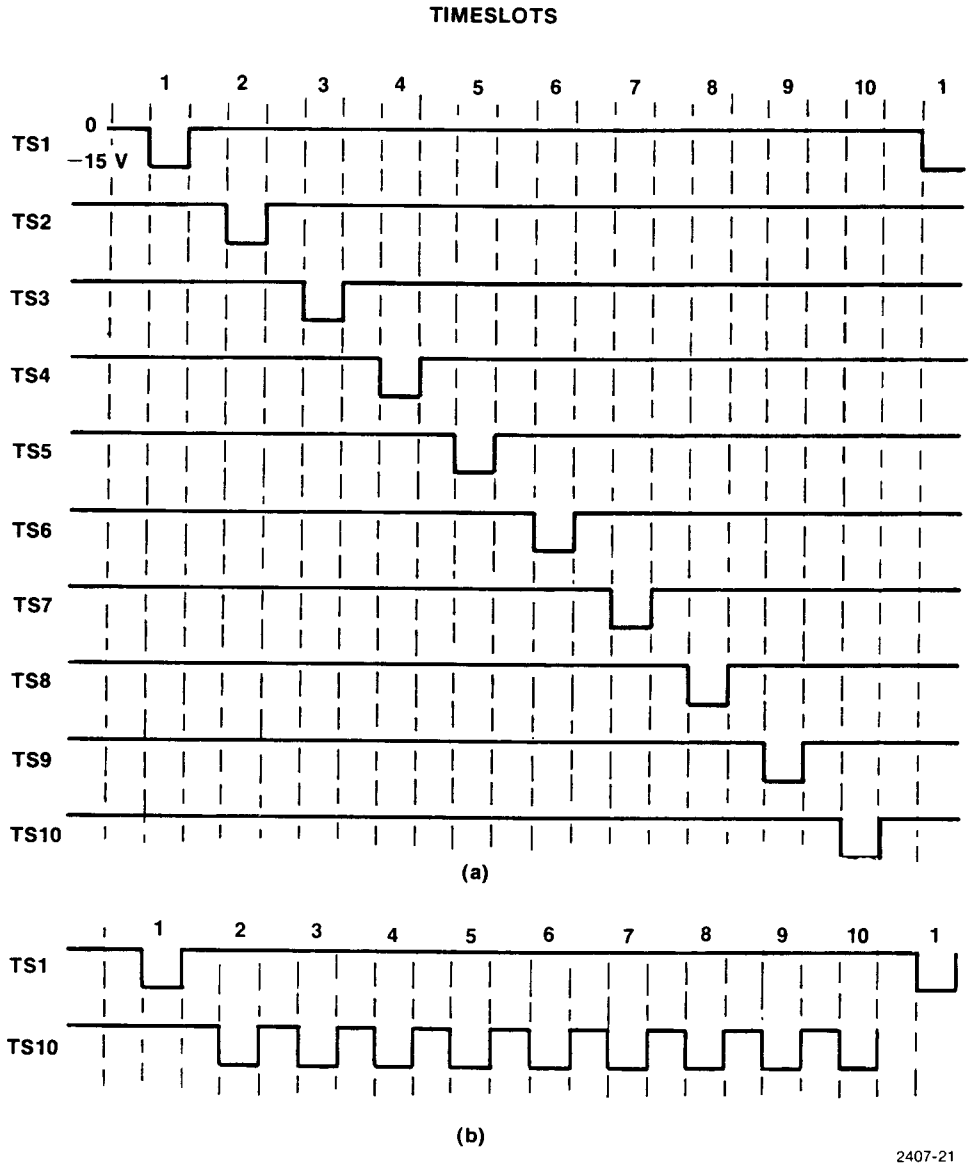


Fig. 3-21. Time-slot pulse timing for programmable and non-programmable plug-ins.

TABLE 3-7

ANALOG DATA MULTIPLEXER CHANNELS

CHANNEL NO.	U812 PIN NO.	DATA SELECTED		
		PLUG-IN COMPARTMENT	CHANNEL	ROW/COLUMN DATA
1	3	Horizontal	1	Row
2	4	Horizontal	1	Column
3	5	Horizontal	2	Row
4	6	Horizontal	2	Column
5	10	Vertical	1	Row
6	11	Vertical	1	Column
7	12	Vertical	2	Row
8	13	Vertical	2	Column

Analog Data Decoder. The Analog Data Decoder (U926 -- left-center of diagram 17) converts the current levels it receives from the analog multiplexer to a binary code. The 6800 reads this code from the Readout Data Register located at 38EF in the 6800 address space.

The analog data is fed to a current-input analog-to-digital converter (A/D), U926, through a divider network. R932 provides an adjustment to correct for minor variations in the analog current levels. U926 converts the analog current to a one-of-ten (0-9) code. One output is asserted for each level between 100 and 900 microamps; no outputs are asserted for a 0 milliamp input. U912 converts this one-of-ten code to its 4-bit BCD equivalent and U814 buffers the data onto the 6800 bus.

If the analog input current reaches 1.0 milliamp, the output of comparator U836 goes high, clearing bit 7 ($\overline{BD7}$) of the readout register. Table 3-8 shows the output codes for each analog input current.

TABLE 3-8

READOUT DATA REGISTER CODES

Analog Input Current	Output Code								Row No.	Column No.
	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BDØ		
0 ma	1	X	X	X	1	1	1	1	1	Ø
0.1 ma	1	X	X	X	1	1	1	Ø	2	1
0.2 ma	1	X	X	X	1	1	Ø	1	3	2
0.3 ma	1	X	X	X	1	1	Ø	Ø	4	3
0.4 ma	1	X	X	X	1	Ø	1	1	5	4
0.5 ma	1	X	X	X	1	Ø	1	Ø	6	5
0.6 ma	1	X	X	X	1	Ø	Ø	1	7	6
0.7 ma	1	X	X	X	1	Ø	Ø	Ø	8	7
0.8 ma	1	X	X	X	Ø	1	1	1	9	8
0.9 ma	1	X	X	X	Ø	1	1	Ø	10	9
≥1.0 ma	Ø	X	X	X	X	X	X	X	14	10

Character Generator

The 6800 reads the row and column data from the Readout Data Register, converts these two 4-bit values to an equivalent ASCII character, and writes the character into the Character Generator. The Character Generator stores the ASCII characters in a RAM memory, called a "refresh memory" because the memory contents are used to refresh the TV display. Then it generates the readout video signal that is mixed with the waveform video for display on the TV monitor.

Generating a Raster-Scan Display. Before we discuss the Character Generator in detail, a review of raster-scan character generation might be helpful.

The picture on the TV monitor is generated by scanning an electron beam horizontally across the face of the phosphor-coated CRT (Cathode Ray Tube). At the same time, the beam is deflected vertically at a much slower rate. The face of the CRT emits visible light where the electron beam strikes it, so the result of this scanning is a closely spaced set of horizontal lines covering the entire face of the CRT. These lines are called a "raster." The entire raster is scanned 60 times each second (50 times per second if option 13 is selected). This raster forms the background on which the picture is displayed.

The brightness of the light emitted from the CRT screen is controlled by varying the intensity of the electron beam as it scans. The video (or brightness) information is sent to the monitor in the form of a varying voltage which controls the intensity of the electron beam, and as a result produces a picture on the monitor screen.

To produce a character on the monitor screen, the video information must be sent to the monitor each time the electron beam sweeps over the area where the character is displayed. Suppose, for example, that we wish to display the character "V." The character is formed on the monitor screen by a series of bright dots in a 7 X 9 matrix, as shown in Fig. 3-22. If the bright dots are represented as ones and the dark dots as zeros, the first row of the character can be represented as 1000001. The remaining eight rows can be represented similarly as shown in the figure. Each of these rows are drawn during one horizontal scan of the electron beam. The ones in these binary words correspond to a high video level (bright area) and the zeros correspond to a low level (dark area). If the same dots are illuminated in the same place each time the electron beam scans that area of the CRT, a stable character is displayed.

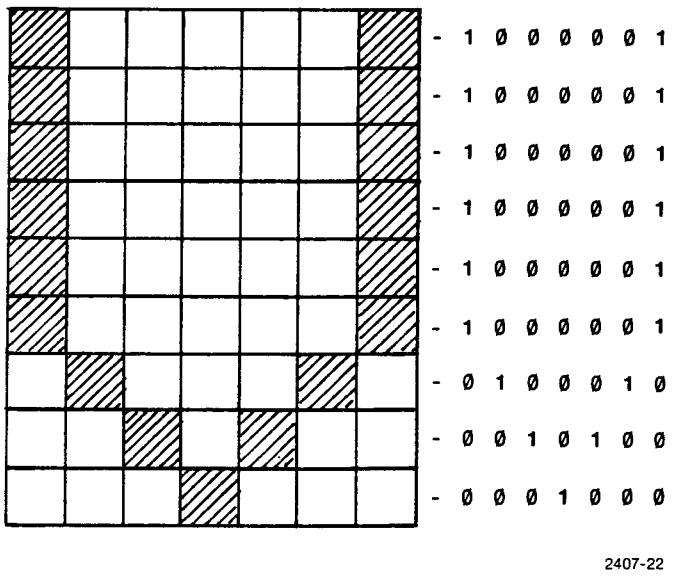


Fig. 3-22. A typical character as displayed on the TV monitor.

The displayed characters are usually stored (in ASCII code) in a RAM refresh memory. Each display cell on the monitor screen (a cell is the space required to display one character) corresponds to one 7-bit memory

location. A set of counters keeps track of the location of the electron beam and cycle through the memory addresses, accessing the same character each time the beam scans the respective locations. The counters cycle through the refresh memory once for each vertical scan of the raster -- called a "field." The output of the refresh memory is fed to a character generator ROM which converts the ASCII character to the 7-bit binary row codes previously discussed. A 4-bit address from the counters identifies which of the nine rows that make up one character is currently being scanned. This parallel code is then converted to a serial bit stream and shifted to video levels to drive the TV monitor.

Character Generator Block Diagram. A block diagram of the Character Generator system in the 7912AD is shown in Fig. 3-23. This system contains the basic components we have discussed -- the address counters, refresh memory, character generator ROM, and parallel-to-serial shift register. In addition to these basic components the 7912AD system contains a dot clock, X and Y sync logic, memory select logic, and video enable logic.

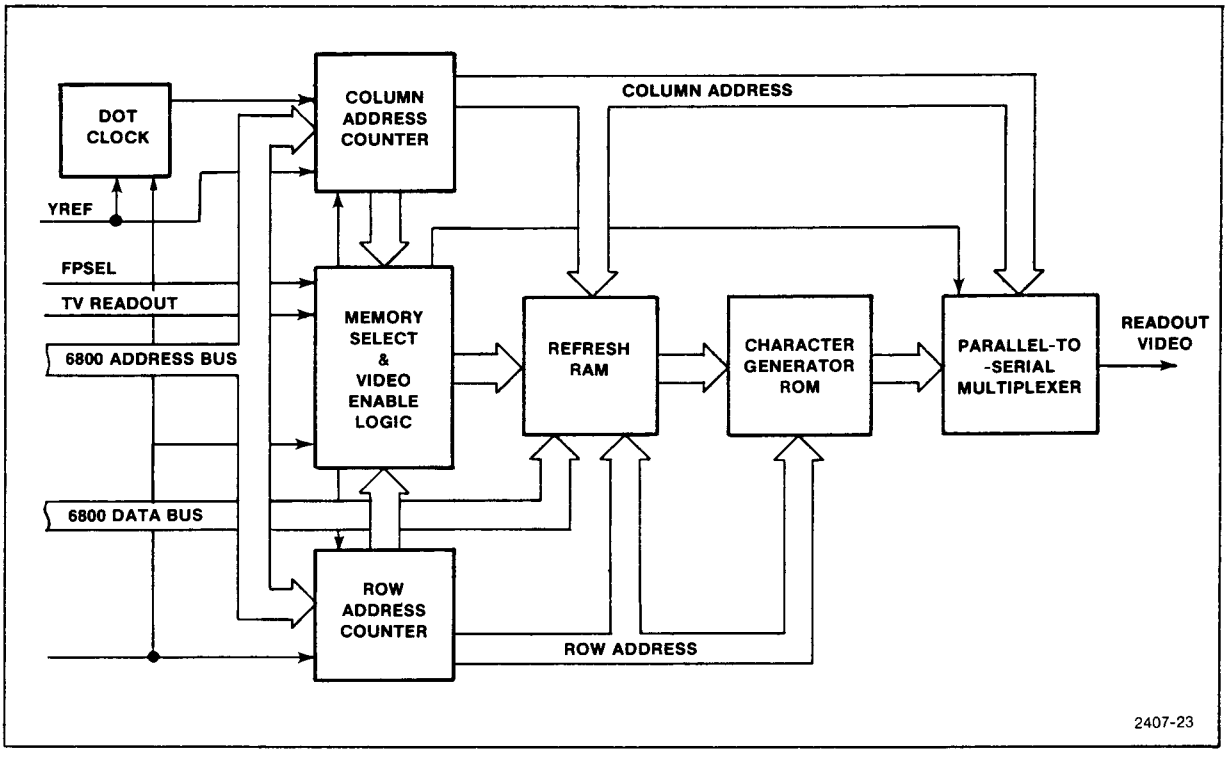


Fig. 3-23. Block diagram of the character generator.

Dot Clock. The Dot Clock (U032A and U032B, upper left of diagram 14) generates the clock for the character generator. This clock is synchronized to the XREF pulses which occur at the beginning of each horizontal retrace period. The clock, formed by two one-shots in a feedback loop, runs at approximately six megahertz. When the XREF pulse goes high at the beginning of retrace, U040A is fired and its $\overline{Q}$ output, pin 7 goes low, clearing U032A. The $\overline{Q}$ output of U032A is forced high and the output of U020D goes high. When U040A times out about one microsecond later, its $\overline{Q}$ output goes high and the output of U020D makes a high-to-low transition, firing U032B. The Q output of U032B goes high for about 170 nanoseconds. Then the output makes a high-to-low transition, firing U032A. When U032A times out, its $\overline{Q}$ output makes a low-to-high transition and the output of U020D makes a high-to-low transition. As a result, U032B is fired again and the cycle repeats itself.

Column Address Counters. U220 and U230 comprise the Column and Memory Address Counters. These counters count the vertical columns in the display. One character consists of eight columns including one blank column per character. The counters also provide the address for the refresh memory.

The dot clock drives U230 through U030B and U030A. On the rising edge of each clock pulse, U230 counts up, incrementing the column address. This 3-bit column address drives the 8-to-1 line multiplexer, U140, in the lower-right of diagram 14. The character generator ROM, U120, feeds the parallel binary code for the dots in one row of the character to the multiplexer. The column address sequentially selects each bit of this parallel code and the multiplexer sends it on the $\overline{\text{RO}}$ $\overline{\text{VIDEO}}$ (Readout Video) line.

Recall that the characters are displayed in a 7 X 9 matrix. When the column address reaches 8 (1000_2) a new character must be fetched from the refresh memory for display. The Q_D output (pin 7) of U230 is toggled, incrementing the memory address to the next character in memory. At the same time, the Q_A, Q_B and Q_C outputs go low. This column address is fed back to U340C and U340D at the left edge of the diagram. The low on these inputs causes their outputs to go low and the output of U130D to go high. On the next rising clock edge, U320B is clocked and its $\overline{Q}$ output goes low. The low on this output blocks the clock signal through U030B by forcing its output high. The clock signal is blocked for one period to add blank space between characters and provide time for the access delay in the refresh RAM and character generator. When U320B is clocked, its Q output goes high and the output of U340D goes high. On the next clock

pulse, U320B is clocked again. This time, the $\overline{Q}$ output goes high and U030B begins passing the clock pulses again. As a result, this circuit blocks one clock pulse at the end of each character.

U220 counts the displayed characters and provides the memory addresses for the refresh memory. At the beginning of each new character (column number 8), the most-significant bit of U230 toggles, incrementing the memory address. The carry output (pin 12) of U230 goes high on the 16th count (every other character), incrementing U220. The XREF pulses fire U040A at the start of horizontal retrace clearing the counters so that they always begin counting from zero at the start of each horizontal line.

Row Address Counters. U200 and U210 comprise the Row Address Counters. These counters count the horizontal lines in the raster and tell the Character Generator which row of dots in the 7 X 9 matrix is being displayed. The counters are incremented at the start of each new line by the XREF pulse. The YREF pulse, which occurs at the beginning of each vertical retrace period, clears the counters so that they always begin counting lines from zero.

Memory Select Logic. The scale factor readout words are located on the monitor as shown in Fig. 3-24. The readout circuit must be disabled while the electron beam is scanning the blank areas between the readout words. The Memory Select Logic accomplishes this task by decoding the outputs of the row and column address counters.

The vertical channel 1 and horizontal channel 1 readout words are displayed 32 lines below the top of the raster, as shown in Fig. 3-24. The Row Address Counters count the first 32 lines before enabling the memory and video. On the 33rd line, the outputs of U200 are:

Q_A	Q_B	Q_C	Q_D
Ø	1	Ø	Ø

When the 33rd line begins, the Column Address Counters count eight character widths (64 columns) before enabling the memory and video. This delay provides eight character widths of blank space from the left edge of the raster before starting the vertical channel 1 readout word. When the column counter counts the ninth character space (65th column), the Q_C output of U220 goes high. Now the A and B input of U300B are high and the enable input (2G) is low. As a result, the Y_3 output goes low,

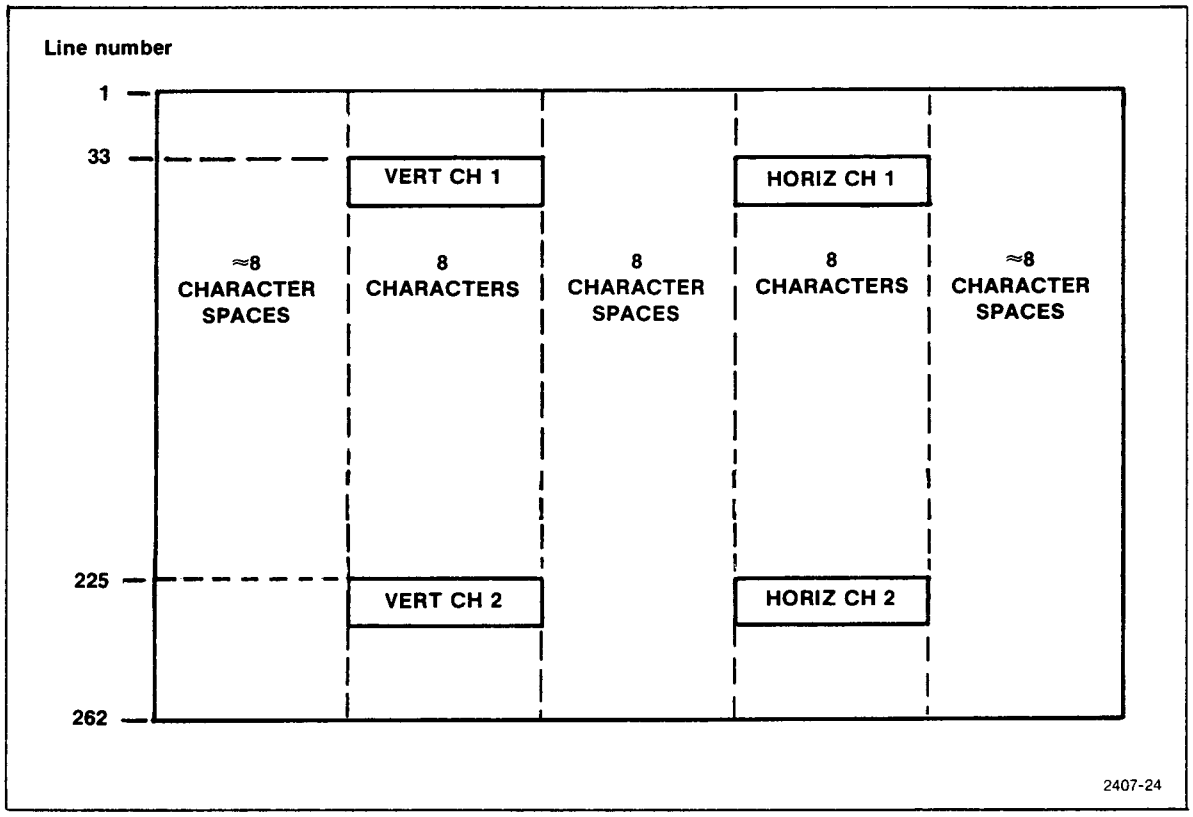


Fig. 3-24. Location of the readout display showing the spacing of words.

enabling U300A. The Q_C and Q_D output of U200 are low so the Y_0 output of U300A goes low enabling RAM chips U000 and U100. These two RAMs store the vertical channel 1 and horizontal channel 1 readout data. When the memory is enabled by asserting the ME input, the ASCII code for the first character is fetched and fed to the Character Generator. The Character Generator outputs the parallel video information that forms the first row of the character. Finally, this parallel information is shifted onto the $\overline{\text{RO VIDEO}}$ line in serial form by U140.

When all eight columns of video information (including one blank column) have been sent, the memory address is incremented and the next character in the readout word is fetched from memory. This process is repeated until one row of dots for all eight characters (including blanks) in the readout word have been displayed.

At this point, the Column Address Counters have counted 16 characters (128 columns). The Q_C output of U220 goes low and the Y_3 output of U300B goes high, disabling the memory. The output of U020B goes

low, disabling the video output of the multiplexer through U020C. The memory and video remain disabled until the 24th character count. This provides the blank space between the top readout words. On the 24th character count, Q_C goes high again and the process just described is repeated. The column counters count through the horizontal channel 1 readout word. Then the memory and video are disabled for eight more character spaces to provide the blank space to the right of the horizontal channel 1 readout word.

Then the XREF pulse occurs, clearing the Column Address Counters and incrementing the Row Address Counters. The next video line is scanned as just described except that the row address is incremented so the Character Generator outputs the code for the second row in the 7 X 9 matrix for each character. The process is repeated for each of the nine lines that comprise one row of characters. On the 48th line, the Q_A output of U200 goes high, disabling the memory and video until the 224th line. This provides the blank space in the center of the screen.

On the 225th line, the outputs of U200 are:

Q_A	Q_B	Q_C	Q_D
Ø	1	1	1

This combination enables the memory and video to display the vertical and horizontal channel 2 readout words. This time, RAM chips U010 and U110 are enabled and the data for these readout words is displayed.

After completing the channel 2 words, the memory and readout video are again disabled, adding the blank lines at the bottom of the screen. Finally, the YREF pulse clears the counters in preparation for starting a new field.

Loading the Character Generator. The MPU loads ASCII characters into the refresh memory by addressing the refresh memory through the row and column address counters. The memory is loaded in 8-byte blocks -- one block for each 8-character readout word. Table 3-9 shows the 6800 addresses for each of these 8-byte blocks.

TABLE 3-9

6800 CHARACTER GENERATOR ADDRESSES

Address	Data
5000-5007	Vertical Channel 1 Readout
5008-500F	Horizontal Channel 1 Readout
5010-5017	Vertical Channel 2 Readout
5017-501F	Horizontal Channel 2 Readout

When the 6800 addresses the Character Generator, $\overline{\text{FPSEL}}$ is asserted. The low on $\overline{\text{FPSEL}}$ causes the row and column address counters to load the address on the 6800 address bus through the A, B, C, and D inputs of the counters. This forces the refresh memory to the address specified by the 6800. U300A and U300B decode the address and enable the selected memory chips. At the same time, the low on $\overline{\text{FPSEL}}$ clears U320A (lower-left of diagram 14); the $\overline{Q}$ output goes high forcing the output of U130A low. This output is tied to the strobe input of U140 through U020C. When the strobe input goes high, the $\overline{\text{RO VIDEO}}$ line is set to its high impedance state, disabling the video output while the 6800 is loading new data into the refresh memory.

At the center of the MPU's phase-2 clock period, $\overline{\text{STROBE}}$ goes low and the output of U340A (bottom-center of diagram 14) goes low, asserting the WE (Write Enable) inputs of the memory. The addressed memory bank loads the data from the 6800 bus into the specified memory location. If there is no readout data for one of the channels, the MPU loads spaces in the refresh memory.

7K/IEEE 488 Interface

The 7K/IEEE 488 Interface provides the interface between the 7K bus and the 6800 MPU. The MPU echoes 7K bus transactions onto the external IEEE 488 bus and visa versa (7K is an abbreviation for the Tektronix 7000-Series of mainframes and plug-ins). The IEEE 488 bus is, in effect, extended through the 7912AD to the plug-ins. Figure 3-25 shows a simplified diagram of the complete 7K/IEEE 488 Interface system.

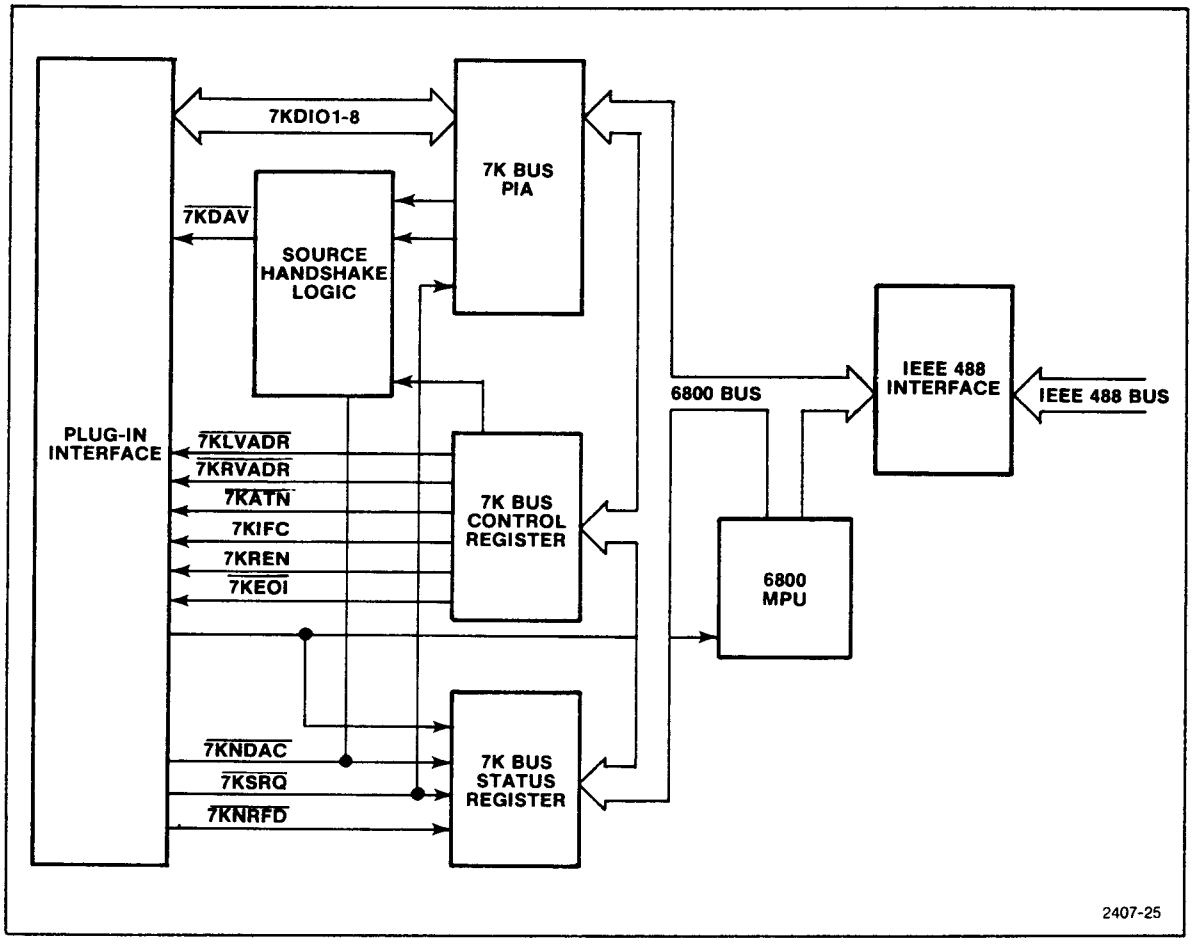


Fig. 3-25. Block diagram of the 7K/IEEE 488 Interface system.

The 7K Bus. The 7K bus that connects programmable plug-ins and mainframes is very similar to the bus specified in the IEEE Standard 488-1975. The 7K bus is divided into three groups of lines: an eight-line data bus, a four-line transfer bus (this part of the bus is modified from the IEEE standard) and a five-line management bus.

The data bus (DIO1-8) is an 8-bit bidirectional bus. All data, device-dependent messages, and addresses are transferred over this bus. The commands, data, and addresses are sent one 8-bit byte at a time in a byte-serial bit-parallel fashion.

The transfer bus carries the handshake sequences that are executed to transfer every byte on the bus. The handshake insures that the data is transferred between the 7912AD and plug-ins in an orderly fashion. The 7K transfer bus contains the three handshake lines specified in the IEEE standard with one additional line. The lines are briefly described below:

7KNRFD (Not Ready For Data) -- When addressed to listen or an ATN message is received, the plug-in(s) assert this line until they are ready to receive a data byte. The 7912AD echoes 7KNRFD onto the external NRFD line on the IEEE 488 bus. When the plug-in is ready to listen, it releases 7KNRFD and the 7912AD releases NRFD, allowing the talker to place a byte on 7KDI01-8.

7KDAV (Data Valid) -- The 7KDAV line is asserted by the 7912AD when it has placed a valid byte on the 7K bus for a listen-addressed plug-in. The line is also asserted when the MPU reads data from a talk-addressed plug-in; the positive transition at the end of the 7KDAV pulse tells the plug-in that the byte is received.

7KNDAC (Not Data Accepted) -- When addressed to listen or an ATN message is received, the plug-in(s) assert this line until they have captured the byte on the bus. The 7912AD echoes this line onto the external NDAC line. When the plug-ins have received the byte, 7KNDAC is released. Then the talker can remove the byte from the bus and release DAV. This completes the handshake process.

7KSND (Send) -- This signal is unique to the 7K bus. The plug-in uses the standard three-wire handshake just described for the acceptor handshake. However, for the source handshake the plug-in and mainframe use a two-wire, non-interlocked protocol. The plug-in asserts 7KSND when it places a byte on the bus. The 7912AD accepts the byte and sends it out through its IEEE-488 interface using the standard source handshake. While the 7912AD is sending the byte, the plug-in monitors the state of 7KDAV. When 7KDAV makes a low-to-high transition at the end of the handshake, the plug-in assumes that the byte was successfully transferred unless 7KATN was asserted during the delay.

The management bus is a group of lines that control the interface and data transfer. These lines communicate interface messages to detect an interrupt from one of the plug-ins, enable remote operation, and denote the end of a message on the data bus. Most of these lines are direct counterparts of the lines on the IEEE 488 bus. The functions of these lines are briefly described below:

7KATN (Attention) -- Asserted by the 7912AD when the IEEE 488 bus ATN line is asserted. When low, information on the data bus is interpreted as an interface message. When 7KATN is high (not asserted), the byte is interpreted as a device-dependent message or data.

7KIFC (Interface Clear) -- Asserted by the 7912AD in response to a low on the external IFC line. When asserted, the IEEE 488 interfaces in the plug-ins are initialized to their idle state.

7KSRQ (Service Request) -- Asserted by the plug-ins to request service from the controller-in-charge on the external IEEE 488 bus. The 7912AD asserts the external SRQ line to signal the controller-in-charge. The controller usually interrupts its current task and conducts a serial poll to determine the source of the interrupt. The plug-in reports its status through the 7912AD when polled.

7KEOI (End Or Identify) -- Asserted by the plug-in when it is talking or by the 7912AD when the plug-in is listening. A low on EOI indicates that the byte currently on the bus is the last byte.

7KREN (Remote Enable) -- The 7KREN line is not a direct copy of the external REN line. The 7912AD asserts 7KREN when it receives the first attention message with REN asserted (e.g., the 7912AD's listen address). 7KREN remains asserted until one of three conditions occur: The 7912AD receives the GTL (Go To Local) command, the front-panel LOCAL button is pressed (when the instrument is not set to remote with lockout state), or the external REN line is unasserted. When 7KREN is unasserted, the plug-in is forced to go to local state.

The 7K bus comes into the 7912AD through the Plug-in Interface board, A46 (diagram 3). Programmable plug-ins use time-slot lines TS2-TS9 for the 7KDI01-8 lines. The 7K data bus is isolated by the set of diodes shown at the center of diagram 3. These diodes keep the time-slot pulses off the 7K bus when a non-programmable plug-in is installed. The 7K management and transfer busses do not share their lines with other functions.

The 6800 controls and communicates with the 7K bus through three devices -- the 7K Bus PIA (U424, diagram 17), the 7K Bus Control Register (U538), and the 7K Bus Status Register (U524). Table 3-10 summarizes the registers and their 6800 addresses.

TABLE 3-10

7K INTERFACE REGISTERS

Address	Register
387X	7K Interface PIA
7C	Input Port (Data Reg. A)
7D	Input Control (Control Reg. A)
7E	Output Port (Data Reg. B)
7F	Output Control (Control Reg. B)
38F4	7K Bus Status Register
38F8	7K Bus Control Register

Peripheral Interface Adapters (PIA). The 6800 communicates with the 7K/IEEE 488 interface and the main IEEE 488 interface through two Peripheral Interface Adapters (PIAs). A brief discussion of the PIA's internal architecture will be helpful in understanding the IEEE 488 interfaces.

Two separate I/O ports, two data direction registers, and two control registers comprise each PIA (see Fig. 3-26). Each line in the I/O ports can be programmed to be an input or output by setting bits in the data direction registers. Two interrupt outputs, $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$, signal the MPU that the PIA has data to be read or needs service.

Two interrupt inputs (CA1 and CB1) are individually programmable as positive- or negative-edge sensitive. Two more lines (CA2 and CB2) can be programmed as edge-sensitive interrupt inputs or peripheral control outputs. The state of these inputs and outputs is programmed through the control registers. The internal interrupt flags are also read from the control registers.

The chip select lines (CS0-$\overline{\text{CS2}}$) are used to address the PIA, while the register select lines (RS0-RS1) select the individual registers within the PIA.

7K Bus PIA. The 7K Bus PIA, U424 at the top-center of diagram 17, handles all communication on the 7K data bus (7KDI01-8). It also controls the $\overline{\text{7KDAV}}$ line. The data bus is bidirectional, so one of the PIA ports is used for reading data from the 7K bus and the other is used for writing data.

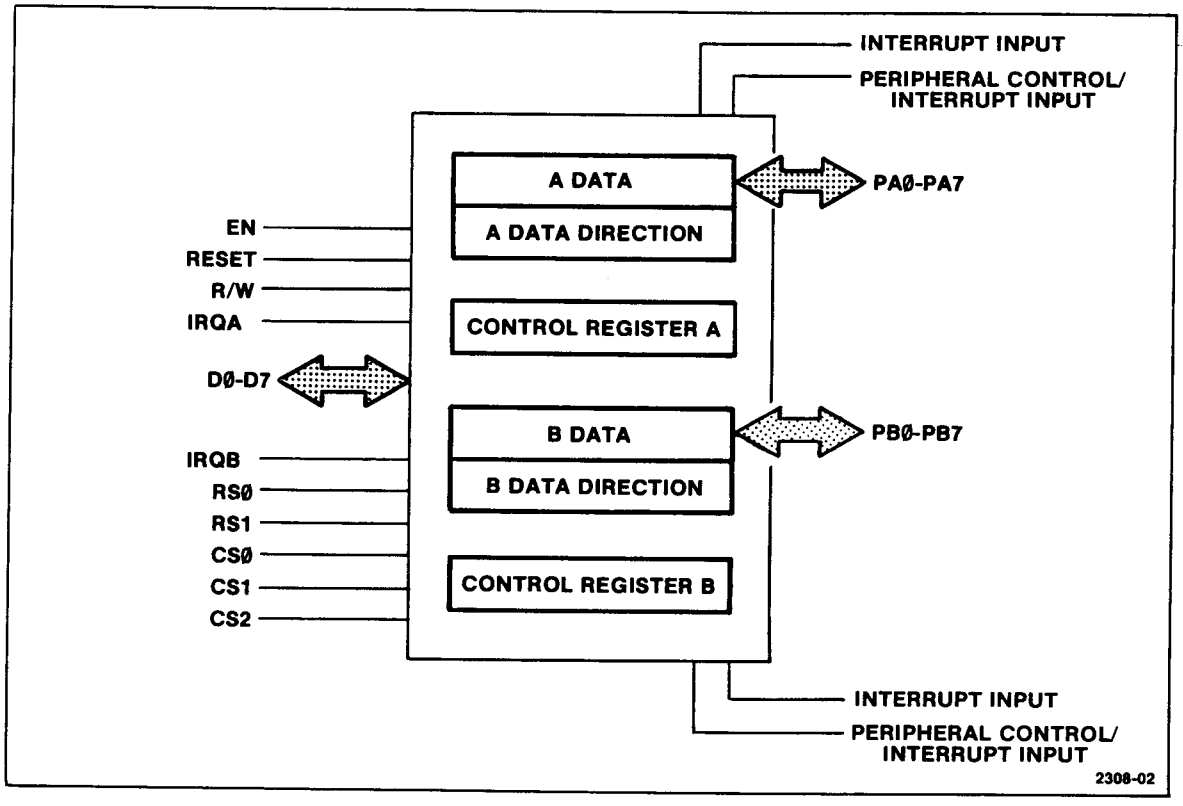


Fig. 3-26. Block diagram of the PIA internal architecture.

When one of the plug-ins is talking, it places a byte on the bus and pulses $\overline{\text{7KSND}}$. The low-to-high transition at the end of the pulse latches the data from the bus in U412. The low-to-high transition on $\overline{\text{SND}}$ also generates an interrupt to the MPU, telling it that the PIA has data to be sent on the IEEE 488 bus. The MPU reads the data from the A port of the PIA. If the other plug-in is not addressed to listen (the usual case), the peripheral control output (CA2) is programmed to go low when the MPU reads the data. The low on CA2 causes the output of U636A to go high which in turn causes the output of U638B and $\overline{\text{7KDAV}}$ to go low. On the next rising edge of the CK2 clock (pin 25 of the PIA), the CA2 output returns to its high state. The high-to-low transition that results on $\overline{\text{7KDAV}}$ tells the plug-in that the byte has been accepted by the 7912AD.

If one plug-in is addressed to talk and the other to listen, the CA2 output is not asserted when the 6800 reads the data from the PIA. Instead, the CB2 output of the PIA (pin 19) is set to go low when the 6800 writes the data to the output port. When the CB2 output goes low as

the result of writing data to the PIA output port, U522A is cleared and the low on its Q output enables bus driver U512. On the rising edge of the next CK2 pulse, the PIA's CB2 output returns to its high state. The high on CB2 and the high on the $\overline{Q}$ output of U522A cause the output of U532A to go high, asserting $\overline{7KDAV}$. This signals the listening plug-in that the data on the 7K bus is valid. When the plug-in accepts the data, it releases $\overline{7KNDAC}$. The positive transition clocks U522A, setting its Q output high to disable the bus drivers and its $\overline{Q}$ output low, to release $\overline{7KDAV}$. The positive transition on $\overline{7KDAV}$ signals the talking plug-in that the transfer is complete. The positive transition on the Q output of U522A also generates an interrupt through the CA1 input of the PIA. This interrupt tells the 6800 that the source handshake was completed. If, for some reason, the listening plug-in doesn't release $\overline{7KNDAC}$, the source handshake can be terminated by clearing bit 1 of the 7K bus control register (pin 19 of U538). Clearing this bit asserts the set input of U522A, resetting it to its idle state.

If either of the plug-ins assert $\overline{7KSRQ}$, the PIA generates an interrupt to the 6800 through IRQB. The 6800 echoes this SRQ to the external IEEE 488 bus. The plug-in reports its status when polled by the controller-in-charge.

7K Bus Control Register. The 6800 controls the 7K management bus and other 7K bus functions through the 7K Bus Control Register. The register, U538 in the bottom-center of diagram 17, is located at 38F8 in the 6800 address space. When the 6800 places the register's address on its bus, $\overline{PISEL}$ (pin 13 of U822D, bottom-left of diagram 17) is asserted. Recall that the $\overline{STROBE}$ pulse occurs near the middle of each phase-2 clock period. As a result, the output of U822D ($\overline{PISTROBE}$) follows the $\overline{STROBE}$ line when $\overline{PISEL}$ is asserted. Data from the 6800 bus is latched into the 7K Bus Control Register on the rising edge of $\overline{PISTROBE}$.

Table 3-11 lists the name and function of the bits in the register.

TABLE 3-11

7K BUS CONTROL REGISTER BITS

BIT	NAME	FUNCTION
Ø	-	Unused
1	$\overline{\text{HSRST}}$	Resets source handshake
2	$\overline{\text{7KRVADR}}$	Addresses right (horizontal) plug-in
3	$\overline{\text{7KLVADR}}$	Addresses left (vertical) plug-in
4	7KREN	7K Remote Enable (inverted)
5	$\overline{\text{7KATN}}$	7K Attention (inverted)
6	$\overline{\text{7KIFC}}$	7K Interface Clear (inverted)
7	$\overline{\text{7KEOI}}$	7K End or Identify (inverted -- output with source handshake only)

Bits 4-7 of the 7K Bus Control Register drive one of the 7K management bus lines through an inverter (U536 A through D). The function of these lines was previously discussed. Bits 1, 2, and 3 of the register drive the $\overline{\text{HSRST}}$, $\overline{\text{7KRVADR}}$ and $\overline{\text{7KLVADR}}$ lines respectively.

The $\overline{\text{HSRST}}$ (HandShake ReSeT) line resets the source handshake logic if a listener fails to release 7KNDAC.

The 7912AD decodes the primary and secondary addresses it receives on the $\overline{\text{IEEE}}$ 488 bus and generates the $\overline{\text{7KLVADR}}$ (7K Left Valid Address) and 7KRVADR (7K Right Valid Address) signals to address the plug-ins. When the secondary address for the horizontal plug-in is received, the 6800 sets bit 2 of the control register, asserting $\overline{\text{7KRVADR}}$. $\overline{\text{7KLVADR}}$ (bit 3) is asserted when the vertical plug-in is addressed. The 7912AD also passes bits 2, 6, and 7 of the addresses to the plug-ins. The plug-ins decode bits 6 and 7 to determine if the address is a talk or listen address and bit 2 to detect the UNT (UNTalk) and UNL (UNListen) messages.

7K Bus Status Register. The 6800 reads the status of several important 7K bus lines through the 7K Bus Status Register, U524, shown in the bottom-right of diagram 17. The 6800 accesses the register by reading from address 38F4. Table 3-12 shows the function of each bit in the register.

TABLE 3-12

7K BUS STATUS REGISTER BITS

Bit	Name	Function
0-3	Unused	
4	$\overline{\text{7KSRQ}}$	7K Service Request
5	$\overline{\text{7KNDAC}}$	7K Not Data Accepted
6	$\overline{\text{7KNRFD}}$	7K Not Ready For Data
7	$\overline{\text{7KEOI}}$	7K End Or Identify

IEEE 488 Interface Control

Introduction. The IEEE 488 interface handles all communication over the IEEE 488 bus for both the mainframe and plug-ins. The interface is controlled by the 6800 microprocessor. All data received from the bus is processed by the 6800; however, data can be sent from the 6800 or directly from the 2900 memory controller. The interface also sends data from the 2900 memory controller to an XYZ monitor. Figure 3-27 illustrates the three basic data transfer paths in the interface.

In this section we will discuss the control and status registers through which the 6800 controls the interface. Figure 3-26 shows a block diagram of the interface. Notice that the PIA (Peripheral Interface Adapter) forms the major control and I/O port for the 6800.

NOTE

This description of the IEEE 488 interface refers frequently to two different busses: the 6800 bus and the IEEE 488 bus. The discussion refers to the busses by name in most cases, but be careful not to confuse them.

IEEE 488 PIA. The heart of the IEEE 488 interface control system is the PIA, U412, shown in the upper-left of diagram 27. Half of the PIA is used as a bidirectional data port. The other half is dedicated to an interface control port.

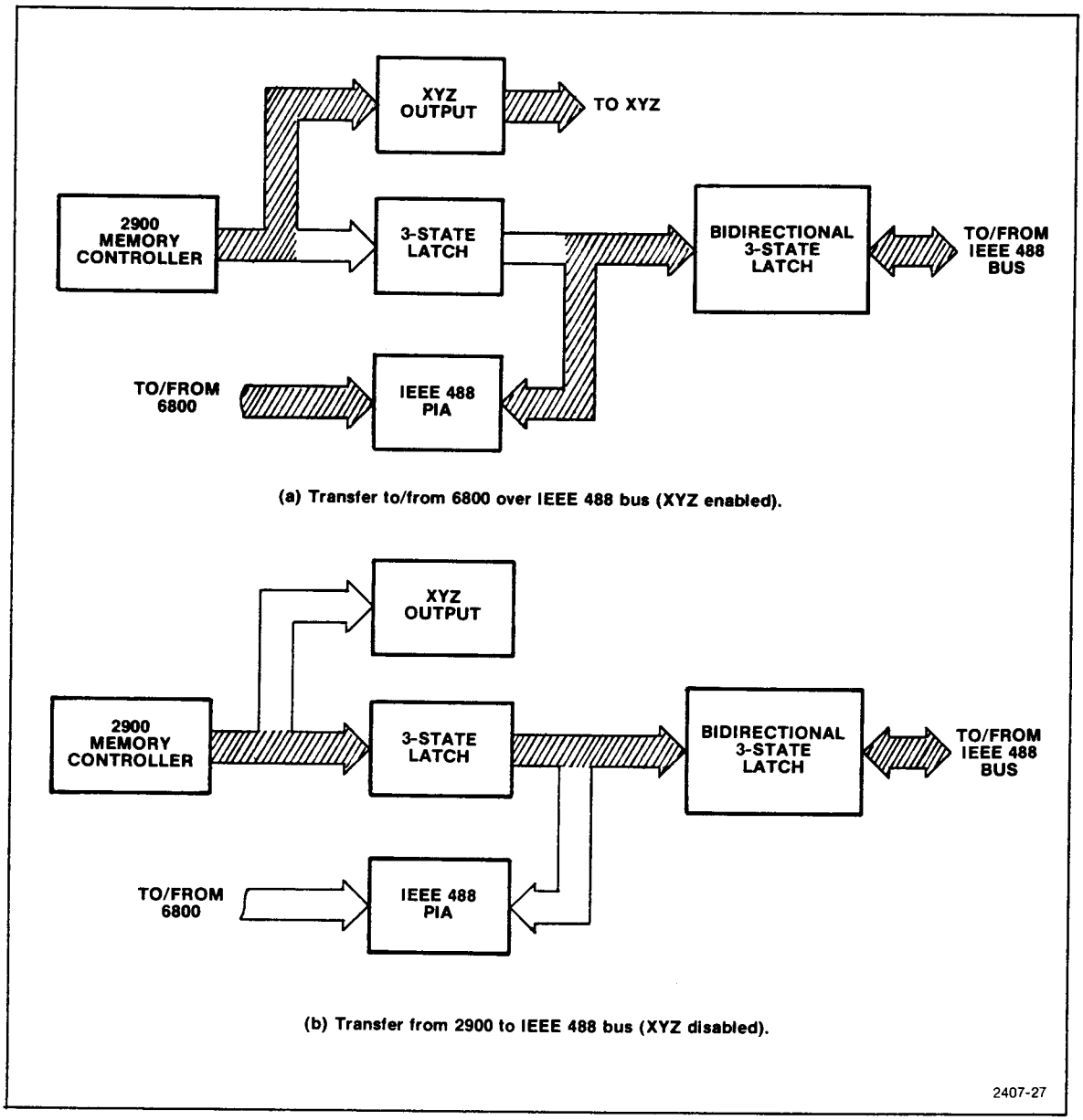


Fig. 3-27. IEEE 488 Interface configurations.

The internal architecture of the PIA was described in the 7K interface section. A review of that description may be helpful.

The 6800 addresses the PIA by placing an address in the range 480C-480F on its bus. The IOSEL line (I/O SELect) is asserted for all addresses in the 4000-4FFF range, enabling U522 (bottom-right of diagram 27). U522 decodes the address and asserts PIA to select the PIA. The two

least-significant bits, BADR0 and BADR1, connect directly to the PIA's register select inputs to select one of the six internal registers (two of the registers are accessed by setting a bit in the control registers).

The PIA serves the dual purpose of an I/O register and a control port. The A port of the PIA is an 8-bit bidirectional port through which the 6800 writes and reads data to or from the IEEE 488 bus. The B port is used as a control port. The lines in this port control the handshake logic or drive one of the IEEE 488 management bus lines. The control signals are listed and briefly defined below:

$\overline{\text{IFCL}}$ (Interface Clear) -- This line is connected to one of the PIA's interrupt inputs and is asserted when the external IEEE 488 bus $\overline{\text{IFC}}$ line is asserted. A negative transition on $\overline{\text{IFCL}}$ causes the PIA's $\overline{\text{IRQB}}$ line to be asserted, generating an I/O interrupt to the 6800. The 6800 responds by initializing the IEEE 488 interface to its idle state, clearing $\overline{\text{TALK}}$ and $\overline{\text{LISTEN}}$. The instrument operating modes are unaffected.

R-ATN (Received ATN) -- This line is asserted when the IEEE 488 bus $\overline{\text{ATN}}$ line is asserted. A positive transition on R-ATN generates an I/O interrupt to the 6800. The interface must stop talking and listen to all bytes sent with $\overline{\text{ATN}}$ true (low).

EOI-MPU (End or Identify) -- When the last byte of a message is being sent over the bus, the 6800 asserts this line. The IEEE 488 $\overline{\text{EOI}}$ line is asserted when EOI-MPU goes high.

$\overline{\text{SRQ-MPU}}$ (Service Request) -- This line is asserted by the 6800 to notify the IEEE 488 controller-in-charge that the 7912AD or one of its plug-ins needs service. When $\overline{\text{SRQ-MPU}}$ is asserted, the external $\overline{\text{SRQ}}$ line is asserted.

BUSY -- The 6800 asserts BUSY when the MPU is busy and will not accept bytes from the IEEE 488 bus. If the 7912AD or a plug-in is addressed as a listener and $\overline{\text{ATN}}$ is false (high), the $\overline{\text{NRFD}}$ bus line is asserted. BUSY goes low when the 6800 is prepared to accept more input.

NBAP (New Byte Available from the Processor) -- This line is asserted by the 6800 when it has a byte to send on the IEEE 488 bus. NBAP initiates the source handshake and remains asserted until the handshake is successfully completed or it is interrupted by $\overline{\text{ATN}}$ and $\overline{\text{DAV}}$.

$\overline{\text{XMT}}$ (Transmit) -- The 6800 asserts this line to enable transfers from the 2900 memory controller to the IEEE 488 bus. $\overline{\text{TALK}}$ must also be true to enable the source handshake required to transfer the bytes over the bus. $\overline{\text{XMT}}$ remains asserted throughout the transfer and goes high (unasserted) when the transfer is complete or an $\overline{\text{ATN}}$ message interrupts the transfer. If the transfer is interrupted, $\overline{\text{XMT}}$ goes low again as soon as $\overline{\text{ATN}}$ goes high.

DATA-IN-EN (Data In Enable) -- When this line is asserted, the receiver portion of the IEEE 488 data bus transceivers are enabled.

$\overline{\text{LISTEN}}$ -- This line is asserted to enable the acceptor handshake while ATN is false. $\overline{\text{LISTEN}}$ is always asserted when the 7912AD is addressed as a listener. The line goes high when the instrument is addressed to talk or when it receives the UNL or IFC messages.

$\overline{\text{TALK}}$ -- This line is asserted to enable the source handshake. $\overline{\text{TALK}}$ goes high if $\overline{\text{ATN}}$ or $\overline{\text{IFC}}$ are asserted. If an attention message other than UNT (UNTalk), DCL (Device CLear), or MLA (My Listen Address) cause $\overline{\text{TALK}}$ to go high, it is asserted again when $\overline{\text{ATN}}$ goes false (high).

R-REN (Receive Remote Enable) -- When the IEEE 488 $\overline{\text{REN}}$ line goes false (high), R-REN goes low, generating an I/O interrupt to the 6800. If $\overline{\text{REN}}$ is high, the 7912AD will not execute any commands that affect the front-panel settings or data memory.

$\overline{\text{DATVAL}}$ (Data Valid) -- This line is asserted by the acceptor handshake logic when valid data is available from the IEEE 488 bus. The high-to-low transition on $\overline{\text{DATVAL}}$ generates an I/O interrupt.

IEEE 488 Bus Status Register. U500 and U302 (top-right of diagram 27) comprise the IEEE 488 Bus Status Register. This is a read-only register used by the 6800 to determine the cause of an I/O interrupt or to read the status of the interface lines. Table 3-13 defines each bit in the register. The 6800 accesses this register by reading from address 4900.

TABLE 3-13

IEEE 488 BUS STATUS REGISTER BIT DEFINITIONS

Bit	Name	Function
Ø	$\overline{\text{IFCL}}$	Cleared when $\overline{\text{IFCL}}$ is asserted.
1	R-REN	Set when $\overline{\text{REN}}$ is asserted.
2	R-EOI	Set when the IEEE 488 $\overline{\text{EOI}}$ line is asserted.
3	R-ATN	Set when $\overline{\text{ATN}}$ is asserted.
4	SENT	Set when a source handshake is successfully completed.
5-6	-	Unused.
7	$\overline{\text{DATVAL}}$	Cleared when $\overline{\text{DATVAL}}$ is asserted.

Talk/Listen Address Register. The Talk/Listen Address Register contains the five low-order bits of the IEEE 488 primary bus addresses. The addresses are set by S400 on the IEEE 488 interface board. U410 and U610D (upper-right of diagram 27) place the address set by S400 on the 6800 bus when the MPU reads from address 4A00. U522, in the lower-right of the diagram, decodes the address and asserts $\overline{\text{TLA}}$ (Talk/Listen Address), enabling the three-state outputs of U410 and U610D.

The upper three bits of the eight-bit primary address are determined by the type of address - talk or listen. The addresses can be set within the full range specified by the standard: 20 to 3E for MLA (My Listen Address) and 40 to 5E for MTA (My Talk Address). Since the talk and listen addresses share the same five low-order bits, there is a fixed correspondence between them. For example, if the switches are set for a MLA of 21, the MTA is set to 41.

Base Secondary Address Register. This register contains the base secondary address for the mainframe and plug-ins as set by S402. The mainframe MSA (My Secondary Address) is equivalent to the address set by S402. The vertical and horizontal plug-ins' secondary addresses are set by the 7912AD MSA in the following manner:

Compartment	Plug-in MSA
Vertical	7912AD MSA+1
Horizontal	7912AD MSA+2

U610C, U410, and U500 place the base secondary address from S402 on the 6800 data bus when the MPU reads from address 4B00. The MSA is selectable within the full range of the IEEE 488 standard: 60 to 7E.

Address Decoding, Bus Drivers and ROM. Diagram 27 also shows the address decoding logic for the IEEE 488 interface, the 6800 bus drivers, and the interface operating system ROM.

All 6800 registers for the IEEE 488 interface are in the range 4800-4FFF. In this range the $\overline{\text{IOSEL}}$ (I/O Select) line is also asserted. When $\overline{\text{IOSEL}}$ is asserted with BADR11 high (addresses 4800-4FFF), U522 decodes the addresses and asserts one of its outputs to enable the addressed register. Table 3-14 shows the 6800 address of each of the interface registers and functions.

U432 is a 2K X 8-bit ROM (Read-Only Memory) that stores the part of the 6800 operating system that controls the interface. The ROM occupies 6800 address space from 4000 to 47FF.

U512 and U502 comprise a bidirectional data bus buffer for the 6800 bus. The buffer is enabled when the PIA or ROM is addressed. If the MPU WRITE line is asserted, the buffer's T_X inputs are asserted, enabling input from the bus. Otherwise the R_X input is asserted, enabling the buffers for output to the 6800 bus.

TABLE 3-14

IEEE 488 INTERFACE REGISTER ADDRESSES

Address	Register or Function
48XX	IEEE 488 PIA
0C	Data Register or Data Direction Register A
0D	Control Register A
0E	Data Register or Data Direction Register B
0F	Control Register B
4900	IEEE 488 Bus Status Register
4A00	Talk/Listen Address Register
4B00	Base Secondary Address Register
4C00	Assert DATACC (Data Accepted)
4D00	Assert CLRSNT (Clear SENT flip-flop)
4E00	Clr DISPLAY latch and init. 2900 output interface.
4F00	Set DISPLAY latch (Enable XYZ)

IEEE 488 Interface Handshake

With a basic understanding of the interface control and status registers in mind, we are ready to discuss the process of transferring data through the interface under the control of the 6800. We will discuss the handshake sequences in two parts -- the source handshake (7912AD talking) and the acceptor handshake (7912AD listening). Remember that the source and acceptor handshakes are simply opposite ends of a single handshake protocol.

Source Handshake. We will make frequent reference to Figs. 3-28, 3-29, and diagrams 27 and 28 as we discuss the source handshake. Figure 3-28 shows a simplified schematic diagram of the source handshake logic when the 6800 is sending data. The process is slightly different when the 2900 memory controller is sending data. Figure 3-29 shows the timing of the handshake signals and relates these signals to the source and acceptor handshake states. The complete handshake logic is shown on diagram 28.

When the 7912AD is addressed to talk, the 6800 asserts $\overline{\text{TALK}}$ by writing to the control output port (port B) of the PIA. The low on $\overline{\text{TALK}}$ causes $\overline{\text{DATA-OUT-EN}}$ to be asserted, enabling the IEEE 488 bus drivers

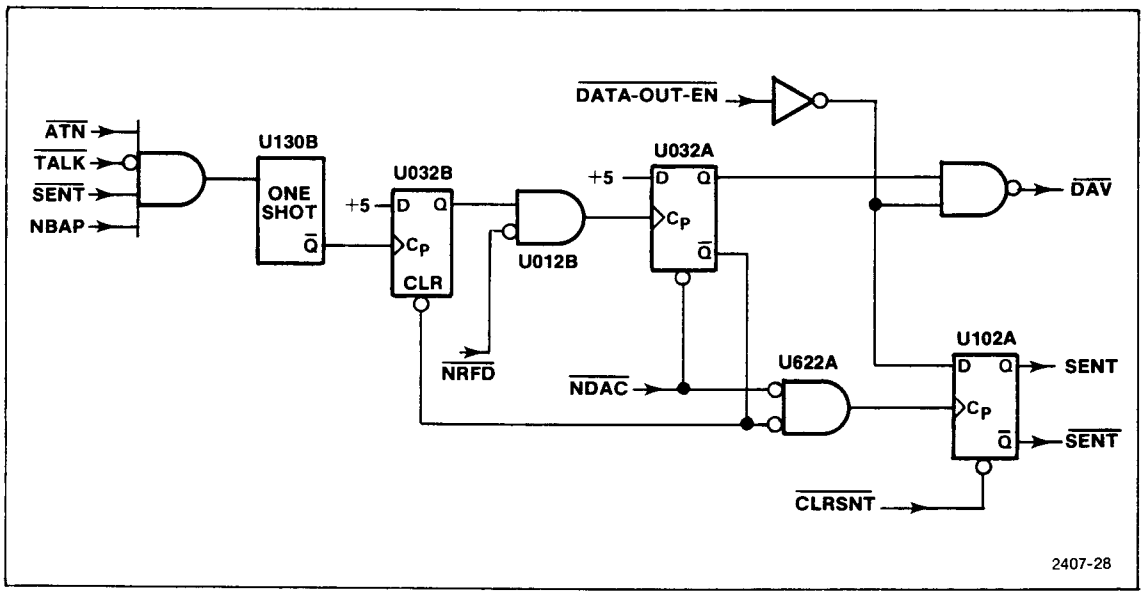


Fig. 3-28. Simplified schematic of the source handshake logic.

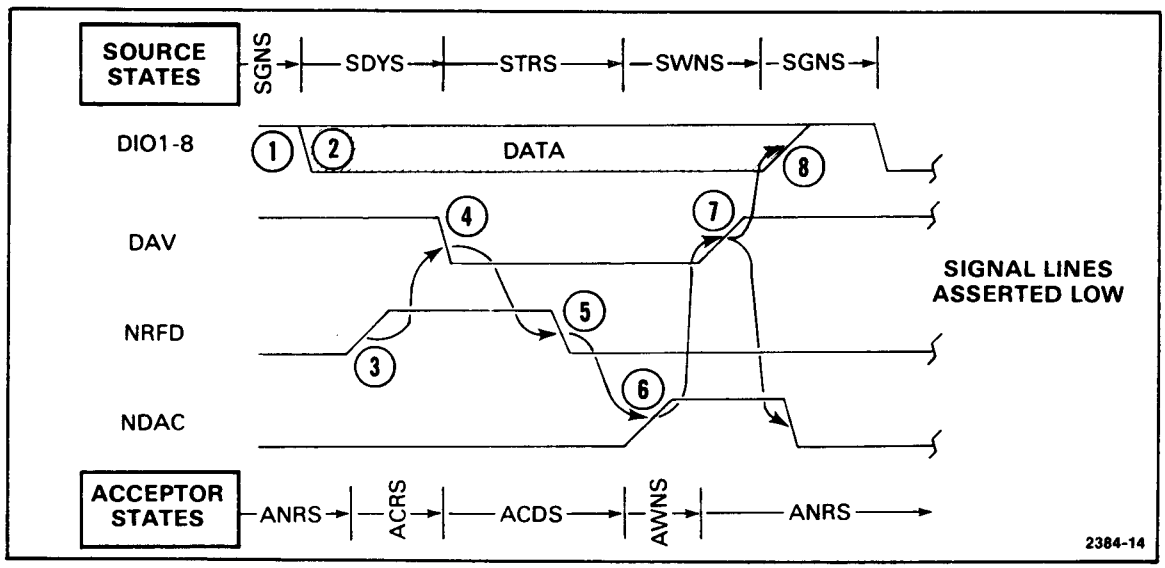


Fig. 3-29. Handshake protocols on the IEEE 488 bus. The numbers are referred to in the text.

(upper-right of diagram 28). At this point the interface is in the Source GeNerate State (SGNS - at number 1 in Fig. 3-29). Then, the 6800 writes the byte it wants to send to port A of the PIA and pulses $\overline{\text{CLRSNT}}$ by

writing (or reading -- either operation asserts the address on the bus) to address 4D00. The low on $\overline{\text{CLRSNT}}$ clears the SENT flip-flop, U102A (see Fig. 3-28). Since the bus drivers are enabled, the byte from the 6800 is asserted on the IEEE 488 bus. Then the 6800 writes to port B of the PIA, asserting NBAP (New Byte Available from the Processor). This signals the handshake logic that the byte has been placed on the bus and that it is time to move to the Source DelaY State (SDYS -- number 2 in Fig. 3-28).

Referring to Fig. 3-28, the output of the first AND gate goes high when NBAP is asserted. The positive transition on the output of this gate fires one-shot U130B. The delay generated by U130B gives the data on the bus time to stabilize before $\overline{\text{DAV}}$ is asserted. When the one-shot times out, the positive-going transition on its $\overline{\text{Q}}$ output clocks U032B. The $\overline{\text{Q}}$ output of U032B goes low and if $\overline{\text{NRFD}}$ is unasserted (high), the output of U012B goes high, clocking U032A. The high on U032A's Q output is inverted by U610B to assert the IEEE 488 bus $\overline{\text{DAV}}$ line (number 4 in Fig. 3-29). The low on $\overline{\text{DAV}}$ tells listeners that a valid byte is on the bus. This is defined in the IEEE 488 standard as the Source TRansfer State (STRS).

The high on the Q output of U032A also goes to the SENT flip-flop through an inverter and U622A. Now the interface waits until all the listeners have accepted the byte and released $\overline{\text{NDAC}}$. $\overline{\text{NDAC}}$ is a wired-OR line, so all listeners must release it before the bus line goes high. When it does, the output of U622A goes high, clocking the SENT flip-flop, U102A, and asserting SENT. The 6800 waits for SENT (bit 4 of the bus status register) to go high, indicating that the byte was successfully transmitted. The high on $\overline{\text{NDAC}}$ also clears U032A, releasing $\overline{\text{DAV}}$ (number 7 in Fig. 3-29). Then the listeners assert $\overline{\text{NDAC}}$ completing the handshake process. The interface is left in the SWNS (Source Wait for New cycle State -- number 7).

If the 6800 has another byte to transmit, it pulses $\overline{\text{CLRSNT}}$ to clear the SENT flip-flop. Then it writes the new byte to the bus, repeating the process. If the byte being transmitted is the last in a message, the 6800 also asserts EOI-MPU, which asserts $\overline{\text{EOI}}$ while transmitting the byte. If the instrument is strapped to delimit messages with a carriage-return and line-feed, these two bytes are added to the message and $\overline{\text{EOI}}$ is asserted with the line-feed. $\overline{\text{TALK}}$ and $\overline{\text{DATA-OUT-EN}}$ remain asserted until the 7912AD receives an $\overline{\text{ATN}}$ message, UNT (UNTalk), or MLA (My Listen Address).

Acceptor Handshake. The acceptor handshake logic is shown in the right-center of diagram 28. We will refer to Fig. 3-28 to relate the handshake sequence to the timing of the signals on the bus.

When the 7912AD is addressed to listen, the 6800 asserts $\overline{\text{LISTEN}}$ and DATA-IN-EN through port B of the PIA. At this point, the interface is in the Acceptor Not Ready State (ANRS -- number 1 in Fig. 3-29). Since $\overline{\text{DAV}}$ is not asserted, R-DAV is low and U230A is cleared. The high on the $\overline{Q}$ output of U230A asserts T-NDAC (Transmit NDAC) which asserts the external $\overline{\text{NDAC}}$ line. If the 6800 is not busy, BUSY is low, and the output of U400B is high. $\overline{\text{DAV}}$ is not yet asserted, so $\overline{\text{DATVAL}}$ is high. As a result, the output of U400A is low and $\overline{\text{NRFD}}$ is not asserted. This moves the interface into the ACceptor Ready State (ACRS -- number 3 in Fig. 3-29).

When the talker asserts DAV, DATVAL goes low, interrupting the 6800. The byte is stable on the IEEE 488 bus and, since the bus receivers are enabled, the PIA has the byte on port A. Notice that port A of the PIA is now being used to input data, so the 6800 must turn the lines around by writing zeros into data direction register A. Then the MPU reads the byte from port A. The low on DATVAL causes the output of U400A to go high, asserting T-NRFD and the external NRFD line. This tells the talker that the 7912AD is busy with the current byte and will not accept more input.

When $\overline{\text{DAV}}$ is asserted, R-DAV goes high, releasing the clear input of U230A. When the 6800 has received the byte from the PIA, it pulses $\overline{\text{DATACC}}$ by writing to address 4C00 (HEX). The rising edge of $\overline{\text{DATACC}}$ clocks U230A and its $\overline{Q}$ output goes low, releasing T-NDAC (Transmit NDAC) and the external $\overline{\text{NDAC}}$ line. The high on $\overline{\text{NDAC}}$ tells the talker that the 7912AD has accepted the byte. The interface is now in the ACcept Data State (ACDS -- number 5 in Fig. 3-29).

When $\overline{\text{NDAC}}$ goes high, the talker releases $\overline{\text{DAV}}$. The low on R-DAV clears U230A and $\overline{\text{NDAC}}$ is asserted. Since $\overline{\text{DAV}}$ is not asserted, $\overline{\text{DATVAL}}$ is high. The 6800 continues to assert BUSY until it finishes processing the byte. When BUSY goes low, the output of U400B goes high. Since the output of U400B and $\overline{\text{DATVAL}}$ are high, the output of U400A goes low, releasing $\overline{\text{NRFD}}$. This completes the acceptor handshake.

Attention Messages. When the controller-in-charge of the IEEE 488 bus asserts the $\overline{\text{ATN}}$ line, all devices on the bus must listen regardless of their present status. When $\overline{\text{ATN}}$ goes low (asserted), the negative transition generates an interrupt to the 6800. The 6800 temporarily suspends its current task and prepares to receive input from the bus.

The low on $\overline{ATN}$ causes the output of U600C (bottom-right of diagram 28) to go low. The low on $\overline{PFCA}$ (Power Fail, interface Clear, or Attention) aborts the source handshake in progress. The low on $\overline{ATN}$ also causes the output of U400B (right-center of the diagram) to go high, unasserting T-NRFD and $\overline{NRFD}$.

If the 7912AD was transmitting a byte when $\overline{ATN}$ was asserted and if the attention message did not abort the transmission (e.g., the message was not DCL, MLA, or UNT), the interface begins talking again when $\overline{ATN}$ goes high. The IEEE 488 standard requires that the talker wait at least 1.1 microsecond after $\overline{ATN}$ goes false before talking. One-shot U130A generates this delay (part of the delay is contributed by propagation delay through the gates between U130A and $\overline{DAV}$). On the positive transition of $\overline{ATN}$, R-ATN goes low, firing U130A. The high on its Q output prevents U032A from being clocked and asserting $\overline{DAV}$. If another byte is ready to be sent when U130A times out, U032A is clocked asserting $\overline{DAV}$. The handshake process then continues as previously described.

Interface Clear Latch. When the IEEE 488 bus $\overline{IFC}$ line is asserted, the interface is reset to its idle state. The low on $\overline{IFC}$ asserts R-IFC, setting the interface clear latch, U622C and U622D (bottom-center of diagram 28). The output of the latch, $\overline{IFCL}$, goes low, interrupting the 6800 and disabling the output drivers for the IEEE 488 bus. The high on R-IFC also causes the output of U600C to go low, asserting $\overline{PFCA}$ and clearing the source handshake logic.

The interface clear latch remains set until the 6800 responds by releasing $\overline{TALK}$ or $\overline{LISTEN}$, if either was asserted. Then the output of U620A goes high, clearing the latch.

Memory Controller Transfers. The 2900 memory controller can send waveform data over the IEEE 488 bus at high speeds. The 6800 initiates such transfers by setting up the interface for a data memory transfer and writing a command word to the 2900 port to begin the transfer. The actual process of handshaking data through the interface will be discussed later.

The 6800 configures the interface for memory controller transfers by asserting $\overline{XMT}$ and $\overline{TALK}$ through the PIA control port. The low on XMT enables the 2900 data latch (U420) and the 2900 handshake logic. U420 is an 8-bit latch that captures data from the 2900 and applies it to the IEEE 488 bus.

The low on TALK enables the source handshake logic and the bus output drivers as previously discussed.

Translator

The Translator board (diagram 13) is the interface between the 6800 and many of the instrument control functions. Registers in the Translator give the 6800 control of the front-panel and readout functions. Table 3-15 summarizes the Translator registers and their 6800 addresses.

TABLE 3-15

TRANSLATOR BOARD REGISTERS

Address	Register Name	Register Type
3000	Status Register	Write only
3001	Action Register	Read/Write
3002-3003	Main Intensity Register (10 bits)	Read/Write
3004	Graticule Intensity Register	Read/Write
3005	Focus Register	Read/Write
3006	Front-Panel Request Register	Read only
3007	Duty Factor Register	Read/Write
3020-303F	Intensity Limit Constant ROM	Read only
5000-501F	TV Readout Buffer* (P/O Character Generator)	Write only

*The Character Generator and TV Readout Buffer were previously described.

Address Decoding and Register Select Logic. The Translator board registers (excluding the TV readout buffer) occupy 6800 addresses between 3000 and 303F. When the 6800 places an address in this range on its bus, the select logic on the MPU board asserts $\overline{\text{TLTRSEL}}$ (Translator Select). With $\overline{\text{TLTRSEL}}$ asserted and an address in the range 3000-3007 (BADR5 low), the Register Select Logic (U530 and U540) is enabled. When the 6800 is reading from a register, $\overline{\text{WRITE}}$ is unasserted (high) and U530 decodes the address on the bus, asserting one of its outputs to enable the addressed register. The enabled register places its data on the 6800 data bus. If $\overline{\text{WRITE}}$ is low, U540 decodes the address and enables the appropriate register to accept input from the bus. For example, to set the Focus Register value, the 6800 writes to location 3005. $\overline{\text{TLTRSEL}}$ is asserted and BADR5 is low, so the output of U310A goes low. Since the 6800 is

performing a write operation, $\overline{\text{WRITE}}$ is asserted. When $\overline{\text{STROBE}}$ goes low (near the middle of the phase-2 MPU clock period), the output of U640A goes high, enabling U540. U540 decodes the three least-significant bits of the address and asserts $\overline{\text{WSEL5}}$ (Write-Select 3005). The low on $\overline{\text{WSEL5}}$ enables the write section of the Focus Register.

The translator read/write registers actually consist of two registers: a read-only register and a write-only register. In our previous example of the Focus Register, if the 6800 reads from address 3005, $\overline{\text{RSEL5}}$ (Read-Select 3005) is asserted. This enables the read-only part of the Focus Register, U740.

Intensity Limit Constant ROM. U240 is a 32 X 8-bit ROM that stores constants used by the intensity limit protection routine in the 6800 operating system. When an address in the range of 3020-303F is on the bus, U310D's output goes low, enabling the ROM. We will discuss the purpose of this ROM in more detail in the Duty Factor Register description.

Status Register (3000). The Status Register (U830 -- top-center of diagram 13) controls instrument functions that are set by the front-panel buttons or their equivalent commands in remote state. This register is located at address 3000 in the 6800 address space. The front-panel DECREASE INTENSITY indicator is also driven through this register. In local state, the 6800 reads the front-panel switch settings from the Front-Panel Request Register. It then sets the appropriate bits in the Status Register to change the instrument status as requested from the front-panel. The Status Register bits are defined below:

X	X	INTEN-SITY LIMIT	READOUT OFF	TV/DIG MODE	LOCAL	LOCKOUT	GRAT ONLY	(Write only)
Bit 7	6	5	4	3	2	1	0	

Bit 0 - Graticule Only: When set, the instrument is set to the graticule-only mode. In this mode the sweep is locked out and only the graticule is written on the target. There is no front-panel control for this function; the bit is set when the instrument receives a GRAT ON or DIG GRAT command. When bit 0 is set, the GRAT ONLY line is asserted.

Bit 1 - Lockout: Set when the 7912AD and its plug-ins are set to local with lockout or remote with lockout state. In remote with lockout state, all front-panel controls except BEAMFINDER, ON/OFF and REMOTE are disabled. Bit 1 does not actually control any instrument functions except the front-panel LOCKOUT light.

Bit 2 - Local: Indicates that the instrument is in local state. In this state the instrument responds to all front-panel controls. Device-dependent messages that do not affect the front panel or data memory are also executed. This bit does not control any hardware functions except the front-panel LOCAL light.

Bit 3 - TV Mode: Set when the instrument is in TV mode. The TV/$\overline{\text{DIG}}$ line goes high when the bit is set. TV/$\overline{\text{DIG}}$ controls the ramp and graticule generators and drives the TV and DIGITAL lights. The 6800 sets this bit when the front-panel TV button is pressed or when the instrument executes a MODE TV command in remote state.

Bit 4 - Readout Off: Cleared when the TV scale factors readout is on. Setting this bit disables the readout by unasserting TV READOUT. The bit is set when the TV SCALE FACTORS switch is turned off or the TV OFF command is executed in remote state.

Bit 5 - Intensity Limit: Set if the 6800 is limiting the beam current because the MAIN and/or GRATICULE intensity controls are set too high. When set, DECREASE INT is asserted, turning on the DECREASE INTENSITY indicator.

Action Register (3001). The 6800 controls a variety of instrument functions through the Action Register. U410 (bottom-left of diagram 13) forms the read section of the register. The read register is enabled when $\overline{\text{RSEL1}}$ is asserted. U500, U420F and U600A (top-center of the diagram) comprise the write section of the action register. $\overline{\text{WSEL1}}$ is asserted to enable this register when the 6800 writes to location 3001. The bits in both the read and write sections of the register are:

FAST SCAN	TEST			SS ARMED	SWP GATE DONE	SS MODE	DELIMIT	READ
			DUTY FACTOR RESET	SS ARM			FPI RESET	WRITE
Bit 7	6	5	4	3	2	1	0	

Bit 0 (Read) - IEEE 488 Delimiter: Indicates to the 6800 that the optional line-feed delimiter has been selected for all messages sent and received on the IEEE 488 bus. The bit is cleared when the standard EOI delimiter is selected. The state of the bit is determined by strap P410 on the Translator board (A22).

Bit 0 (Write) - Front-Panel Interrupt Reset: Clears the front-panel interrupt logic. We will discuss the front-panel interrupt logic in more detail in the Front-Panel Request Register description.

Bit 1 (Read) - Single Sweep Mode: Set when the time base plug-in is set to single-sweep mode. The 6800 checks this bit when a DIG SSW command is received and issues an error if the plug-in is not in single-sweep mode. The bit is set or cleared by a line from the horizontal plug-in.

Bit 2 (Read) - Sweep Gate Done: Cleared by the horizontal plug-in when the SWP GATE line is low, indicating that a sweep is in progress. This bit is set when the sweep is complete and cleared when a new sweep begins.

Bit 3 (Read) - Single Sweep Armed: Set by the horizontal plug-in if the single-sweep function is armed.

Bit 3 (Write) - Single Sweep Arm: Arms the time base single-sweep function. When this bit is set, the positive transition on the output of U830 fires U600A, pulsing $\overline{\text{ARM SS}}$. The low on $\overline{\text{ARM SS}}$ goes to the plug-in to set its single-sweep latch.

Bit 4 (Write) - Duty Factor Reset: Asserts $\overline{\text{DFRES}}$ which resets the duty factor circuit. We will discuss the operation of the Duty Factor Generator in more detail in the Duty Factor Register description.

Bit 6 (Read) Test: Enables the diagnostic mode in the 7912AD. The state of this bit is determined by a strap (P300) on the Translator Board. When the diagnostic mode is enabled, the diagnostic commands (PUT, GET and EXEC) are executed. Unrecognized 6800 interrupts are also reported in this mode. The normal operating mode sets bit 6.

Bit 7 (Read) Fast Scan: Set to indicate that the fast scan mode is selected by strap P411 on the Translator board.

Tracking A/D Converters. Four of the Translator board registers drive tracking analog-to-digital (A/D) converters. The 6800 stores binary values that are equivalent to the analog voltages from the front-panel controls. The A/D converters signal the MPU if the values are too high or too low as the result of a change in the front-panel control settings. The 6800 adjusts the values to "track" the front-panel controls. The binary codes are converted back to analog voltages to control the instrument operating parameters. This allows the 6800 to adjust these parameters to, for example, limit main intensity.

Figure 3-30 shows a simplified diagram of a typical tracking A/D converter. The MPU writes a binary word to the input register. The digital-to-analog (D/A) converter accepts this word and outputs an analog current that is proportional to the value of the input word. The buffer amplifier converts this current to a voltage level for comparison with the voltage from the front-panel control. When the voltages are equal within the window set by R_1 and R_2, the outputs of the two comparators are high and the binary value in the input register accurately represents the front-panel control setting. The output of the buffer amplifier also goes to the instrument function that is controlled by the circuit.

If the front-panel control is changed, the voltage fed back to the comparators changes. Now the buffer amplifier output voltage and the voltage from the control do not match, so one of the comparator outputs goes high. If the voltage from the control is higher (more positive) than the voltage from the buffer amplifier, the UP comparator switches and its output goes low. If the opposite is true, the DOWN comparator switches. The output register inverts the outputs of the comparators so that when one of the comparators switches, the corresponding bit in the output register is set.

The 6800 reads the output register either on a regular polled basis or on receipt of an interrupt (only the duty factor circuit is interrupt driven; the others are polled). If either bit is set, the value in the

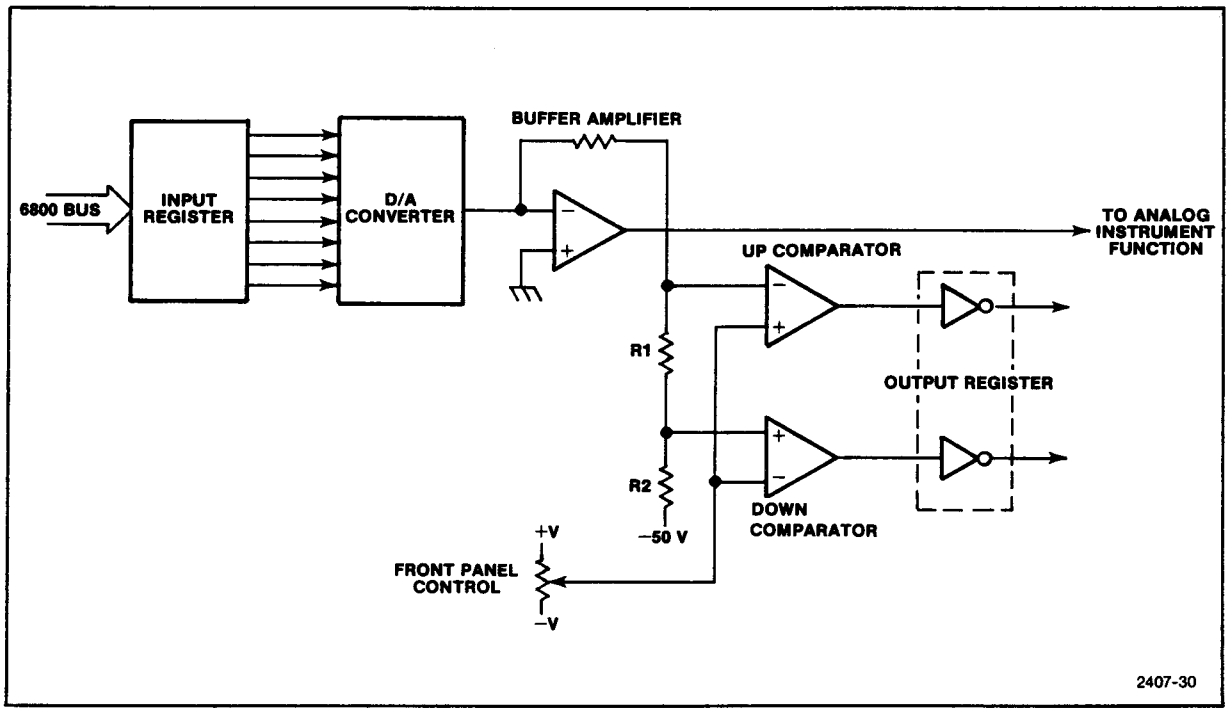


Fig. 3-30. Simplified schematic of a typical tracking A/D converter.

input register must be incremented or decremented to reflect the change in the voltage from the front-panel control.

To illustrate this process, assume that the control setting was increased, causing the control voltage to become more positive. The DOWN comparator is unaffected because more positive voltage on its inverting input drives the output to its low state which is its static state. The more positive voltage is also applied to the non-inverting input of the UP comparator, causing it to switch. The 6800 reads the output register as part of a regular poll and finds bit 7 of the register set. This tells the 6800 that the binary value in the input register must be incremented to "track" the front-panel control. The 6800 begins incrementing the value, causing the output current of the D/A to decrease and the output voltage of the buffer amplifier to increase. When the output voltage of the buffer matches the voltage from the front-panel control, both bits in the output register are cleared and the 6800 stops incrementing the input register. Then the binary value again accurately represents the front-panel control setting. The binary value is only modified if the analog

voltages from the front-panel control and buffer do not match. Thus, the binary value and buffer output voltage track the front-panel knob setting.

This tracking technique allows the 6800 to monitor the settings of front-panel controls and limit their range by not incrementing or decrementing the input register value beyond predetermined limits. When the instrument is in remote state, the 6800 sets the parameters directly by writing the value specified in a command received from the bus to the input register. The comparator outputs are ignored. When the instrument is returned to local state, the 6800 begins to poll the output registers and the instrument operating parameter is adjusted to match the setting of the front-panel control.

Main Intensity Register (3002-3003). The Main Intensity Register consists of a 10-bit write-only register and a 2-bit read-only register. The 10-bit write register occupies two consecutive addresses. The upper six bits of the second byte are unused. The read register uses only the two most-significant bits of the first byte (location 3003) as shown below.

3002	X	X	X	X	X	X	X	X	
3003	INCREASE INTENSITY	DECREASE INTENSITY	X	X	X	X	X	X	READ
3002	X	X	X	X	X	X	MSB	B8	
3003	B7	B6	B5	B4	B3	B2	B1	LSB	WRITE
Bit	7	6	5	4	3	2	1	0	

The Main Intensity Register provides input to a tracking A/D converter similar to the one previously described. A 10-bit register and D/A converter are used to provide a range of intensity values of 0 to 1023 (decimal). U700C and U700D compare the output of the buffer amplifier, U1100, to the voltage fed back from the front-panel MAIN INTENSITY control. If the two voltages do not match within the comparators' window, the output of one comparator goes high, setting the corresponding bit in the read part of the Main Intensity Register, U710.

The 6800 polls this register at regular intervals watching for a set bit. If, for example, bit 7 is set, the UP comparator, U700D, has switched. The 6800 knows that the intensity value in the input register must be increased to track the front-panel setting. First, the 6800 sets the interrupt mask bit and checks that the intensity has not reached the limit value or the maximum (1023). If not, it increments the value in the input register and checks bit 7 again. The value is incremented until either bit 7 is cleared, the intensity limit value or the maximum value is reached. Then the interrupt mask is cleared. Since the front-panel control moves very slowly in relation to the 6800's speed, the MPU can poll the output register and increment or decrement at a fairly low repetition rate. During the time between polls, the MPU is free to perform other tasks.

When the instrument is in remote state, the 6800 sets the D/A input word directly from the value specified in the MAI (MAin Intensity) command, unless that value exceeds the intensity limit.

The output of buffer amplifier U1100 provides an analog voltage to the Z-axis circuit to control the main writing beam intensity. P800 allows the MAIN INTENSITY to be directly controlled by the front-panel control, bypassing the A/D converter and 6800 protection. This configuration is provided for diagnostic purposes only.

CAUTION

Setting the strap to the diagnostic position bypasses the 6800 intensity limit protection. Excessive intensity levels can immediately damage the target.

Graticule Intensity Register (3004). The Graticule Intensity circuit is functionally identical to the main intensity circuit. The input (write) register (U930 -- center of diagram 13) is eight bits wide, providing a range of values from 0 to 255 (decimal). The 600 limits the graticule intensity in a manner similar to the main intensity limit.

IN-CREASE INTEN-SITY	DE-CREASE INTEN-SITY	X	X	X	X	X	X	READ
MSB	B6	B5	B4	B3	B2	B1	LSB	WRITE
Bit 7	6	5	4	3	2	1	0	

The output of buffer amplifier U720 provides an intensity control signal to the Graticule Generator. Bits 6 and 7 of the output (read) register are the decrease and increase flags from DOWN and UP comparators U700A and U700B respectively. Bits zero through 5 of the read register are unused. P700 allows the front-panel GRATICULE INTENSITY control to directly control the intensity, bypassing the A/D converter and the 6800 intensity limit protection. This strap should be set for direct control for service purposes only.

Focus Register (3005). The focus circuit is functionally identical to the Main and Graticule Intensity Circuits except that the input register is a six-bit register. The range of focus values is 0 to 63 (decimal). No protection is necessary at either extreme.

FOCUS UP	FOCUS DOWN	X	X	X	X	X	X	READ
X	X	MSB	B4	B3	B2	B1	LSB	WRITE
Bit 7	6	5	4	3	2	1	0	

The outputs of the write Focus Register (U940) are not inverted, so the binary input word is complemented by the 6800 before it is written to the register. The output of the Focus Register delivers a control signal to the high-voltage circuit to focus the writing beam.

Front-Panel Request Register (3006). The Front-Panel Request Register is the port through which the 6800 reads the status of the front-panel buttons and switches. When any of the front-panel buttons (except ON/OFF and BEAM FINDER) are pressed or the TV SCALE FACTORS switch setting is changed, a front-panel interrupt (FPI) is generated. The bits in the Front-Panel Request Register are defined as follows:

	X	X	READOUT OFF	READOUT ON	TV	DIGITAL	REMOTE	LOCAL	REAI ONLY
Bit	7	6	5	4	3	2	1	0	

Bit 0 - Local: Set when the LOCAL button is pressed. This bit remains set until the 6800 asserts $\overline{\text{FPRESET}}$ through the Action Register.

Bit 1 - Remote: Set when the REMOTE button is pressed. This bit remains set until $\overline{\text{FPRESET}}$ is asserted.

Bit 2 - Digital: Set when the DIGITAL button is pressed. This bit remains set until $\overline{\text{FPRESET}}$ is asserted.

Bit 3 - TV: Set when the TV button is pressed. This bit remains set until $\overline{\text{FPRESET}}$ is asserted.

Bit 4 - Readout On: Set when the TV SCALE FACTORS switch is ON. This bit remains set as long as the switch is ON.

Bit 5 - Readout OFF: Set when the TV SCALE FACTORS switch is set to OFF. This bit remains set as long as the switch is OFF.

Front-Panel Interrupt Logic. When any of the front-panel buttons are pressed or the TV SCALE FACTORS switch setting is changed, the Front-Panel Interrupt Logic (top-left of diagram 13) generates an interrupt to the 6800. In response to the interrupt, the 6800 reads the Front-Panel Request Register to determine the source of the interrupt. Then the MPU asserts $\overline{\text{FPRESET}}$ to clear the interrupt and reset the Front-Panel Request Register.

When any of the front-panel buttons are pressed, the corresponding $\overline{\text{PB}}$ (Push Button) line is asserted and the output of U1120A goes high. The positive transition fires one-shot U600B. The delay generated by U600B debounces the front-panel buttons. When the one-shot times out about 30 milliseconds later, the negative transition on its $\overline{\text{Q}}$ output clocks U1130A. If the output of U1120A is still high, the Q output of U1130A goes high. The positive transition causes U1140 to latch the state of the front-panel buttons. The low on the Q output of U1130A causes the output of U330C to go high, generating a front-panel interrupt. The 6800 temporarily suspends execution of its current task and jumps to a routine that reads the Front-Panel Request Register and asserts $\overline{\text{FPRESET}}$ to clear the interrupt.

When the TV SCALE FACTORS switch setting is changed, an interrupt is generated through U1010B and U1020A. If, for example, the switch is turned from OFF to ON, the Q output of U1010A goes high. At the last $\overline{\text{FPRESET}}$ pulse, the TV SCALE FACTORS switch was OFF, so the $\overline{Q}$ output of U1010B was clocked high. Now both inputs of exclusive-OR gate U1020A are high so its output goes low, generating an interrupt. When the 6800 asserts $\overline{\text{FPRESET}}$, the $\overline{Q}$ output of U1010B will go low and the output of U1020A will go high, clearing the interrupt and setting the flip-flop to generate another interrupt if the switch is turned OFF again. If it is turned OFF, the Q output of U1010A will go low and the output of U1020A will go low until the 6800 asserts $\overline{\text{FPRESET}}$ to clock U1010B's Q output high.

Duty Factor Register (3007). The main intensity protection limit value is determined by the 6800 on the basis of the writing beam duty factor. If a slow sweep speed is selected, the writing beam strikes the target for a greater percentage of time than when a faster sweep speed is selected. The duty factor circuit, shown at the bottom of diagram 13, determines the duty factor value used by the 6800 to access the intensity limit constants stored in the constant ROM.

The Duty Factor Circuit uses a 6-bit tracking A/D converter similar to the one used in the focus circuit. The 6800 controls the circuit through a 6-bit input (write) register and a 2-bit output (read) register as shown below.

DE-CREASE D.F.	IN-CREASE D.F.	X	X	X	X	X	X	READ
X	X	MSB	B4	B3	B2	B1	LSB	WRITE
Bit 7	6	5	4	3	2	1	0	

The tracking A/D in the Duty Factor Circuit does not compare the binary value to a front-panel control setting. Instead, the value is compared to a voltage that is proportional to the duty factor of the main writing beam. The D/A, buffer amplifier, and comparators are similar to the ones used in the other circuits discussed. The comparison voltage is generated by the circuit in the lower-left corner of diagram 13.

Duty Factor Generator. Refer to Fig. 3-31 and diagram 13 as we discuss the Duty Factor Generator. The $\overline{SGE}$ (Sweep Gate Enable) signal is asserted when the time base is generating a sweep and the graticule is not writing a graticule. When $\overline{SGE}$ is low (asserted), Q210 turns off and current through R312, R209, and CR209 charges C633. The voltage on the non-inverting (+) terminal of buffer amplifier U620 rises as the capacitor charges. During each $\overline{SGE}$ pulse, this voltage rises toward the +15-volt supply. CR209 provides charge current for C633 when Q210 is off, while blocking current in the reverse direction when Q210 is on.

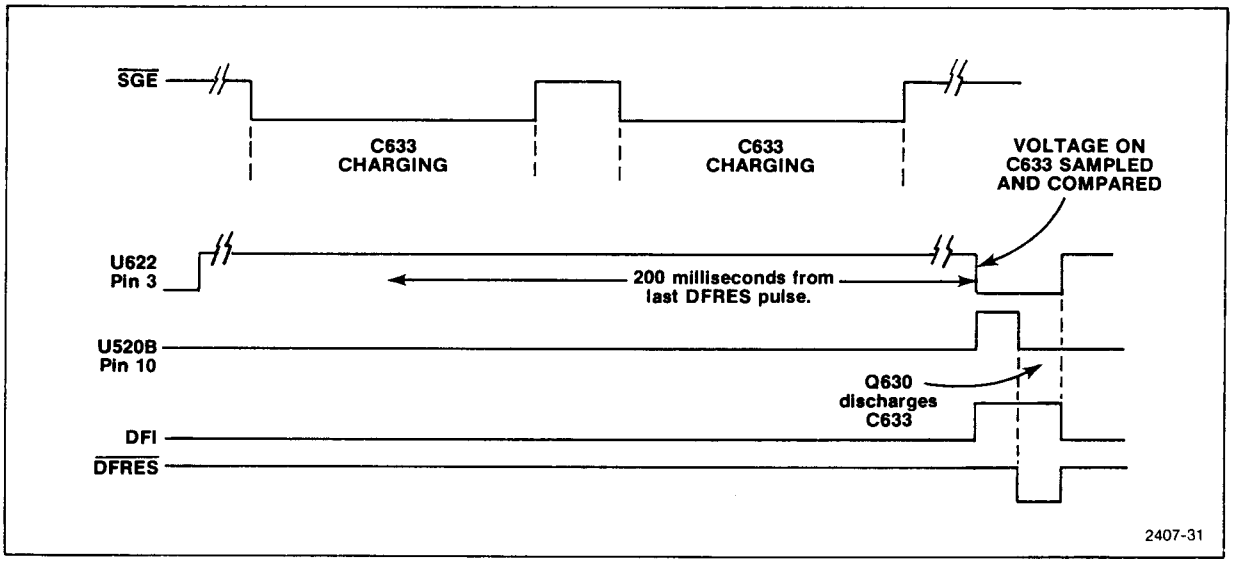


Fig. 3-31. Timing of the duty factor generator.

The $\overline{SGE}$ pulses charge C633 for 200 milliseconds. Then the output (pin 3) of timer U622 goes low. The negative transition also fires U520B, asserting its Q and $\overline{Q}$ outputs. See Fig. 3-31. U730A and U730B compare the output of the buffer amplifier to zero volts. If the output of the D/A converter and the charge on C633 do not match, the output of one of the comparators goes high. When one-shot U520B is fired, the negative transition on its $\overline{Q}$ output clocks U1130B. If either of the comparators' outputs are high at that moment, the output of U640C is high and the $\overline{Q}$ output of U1130B goes high. This generates a Duty Factor Interrupt (DFI) to the 6800. The 6800 temporarily suspends its current task and jumps to a routine that determines a new duty factor value. The 6800 begins incrementing or decrementing the value in the duty factor register, searching for a value that accurately represents the new duty factor.

When this value is reached, both bits in the output register are cleared. Then the 6800 pulses $\overline{\text{DFRES}}$ to clear the interrupt and reset the timing logic.

Recall that when the timer (U622) output went low, one-shot U520B was fired. The one-shot times out about one millisecond later. The timer output stays low for two milliseconds. During the one millisecond when both the Q output of U520B and the output of U622 are low, the output of U640B goes high, turning Q630 on. This discharges C633 in preparation for another 200-millisecond sampling period. When the timer output goes high, Q630 shuts off, and the charge on C633 begins to develop again.

The 6800 uses the duty factor value determined by this process to access the correct value in a table of intensity limit constants stored in the constant ROM, U240. The constants are the limit values for the main intensity limiting routines.

2900/MPU Port

The 6800 controls the 2900 Memory Controller through the 2900/MPU Port shown on diagram 19. The 6800 passes force-branch addresses parameters through this port to initiate memory controller operations, such as DIG DEF (Digitize Defects) or ATC (Average To Center). The 6800 initiates memory controller operations by forcing the microsequencer to the beginning address of the desired routine. This beginning address, passed through the 2900/MPU Port, is called a force-branch address. When the operation is complete, the memory controller signals the MPU by asserting PMCI (Memory Controller Interrupt). The 6800 reads the 2900 status word to determine if the operation was completed successfully.

Four registers comprise the 2900/MPU Port. Two of these registers are 16 bits wide and two are 8-bit registers. Table 3-15 summarizes the registers and their 6800 addresses. Notice that the 16-bit registers require two addresses because they are formed by two 8-bit registers, each with a separate address.

TABLE 3-15

2900/MPU PORT REGISTERS

Register	Address	Read/Write	Purpose
Command	3405	Write	Pass commands to memory controller
Diagnostic	3405	Read	Monitor 2900 lines for troubleshooting
Address/Parameter	3406-7	Write	Pass addresses and parameters to 2900
Status/Parameter	3406-7	Read	Read status and parameters from 2900

Command Register. The 6800 passes commands to control the 2900 and smart clock through the Command Register, U111 and U041A and B. U111 latches all the bits except bits 5 and 7. These bits are latched by separate D-type flip-flops, U041A and U041B at the top of diagram 19. The bits are latched separately to allow the 2900 to clear them without the 6800's intervention. Notice also that bit 5 (REQ) is latched on the falling edge of SIP1 (coincident with the 6800 STROBE pulse). Bit 7 (FBR) is latched on the rising edge. This timing relationship is necessary for proper operation of the 2900's smart clock.

The bits in the command register are briefly described below. A more complete description of these bits is provided in the Microsequencer and Smart Clock descriptions.

FBR	RUN	REQ	NSG	CLMPI	MPUFLG2	MPUFLG1	SLOSWP	3405 (Write)
7	6	5	4	3	2	1	0	

Bit 0 - SLOSWP (Slow Sweep): The 6800 sets this bit to tell the 2900 memory controller that the time base sweep speed is set for 5 microseconds/division or slower. When set, the 2900 uses a slow-sweep algorithm to merge data detected on the target during a digitize operation.

Bit 1 - MPUFLG1: Unused.

Bit 2 - MPUFLG2: Unused.

Bit 3 - CLMPI (Clamp Interface State Machine): This bit is set by the 6800 to clear the Output Interface Control State Machine (part of the memory controller system). The state machine is cleared before beginning any transfers from data memory to the IEEE 488 bus or XYZ monitor.

Bit 4 - NSG (No Sweep Gate): If a DIG DEF (DIGitize DEFects) or DIG GRAT (DIGitize GRATicule) command is received in remote state, the digitize operation should begin without waiting for a sweep gate to occur. The 6800 sets this bit to tell the 2900 to begin the digitize operation without waiting.

Bit 5 - REQ (Request): The 6800 sets the request bit to control the 2900's smart clock. When set, the clock jumps to a single-step loop. The 6800 passes force branch addresses and parameters to the 2900 with the clock in this loop. Each time the request bit is set, the smart clock goes through the loop once and clears the REQ and FBR (Force BRanch) latches, U041A and U041B.

Bit 6 - RUN: When set with REQ, the smart clock goes back into its run loop and begins executing the task assigned by the 6800.

Bit 7 - FBR (Force Branch): When set with REQ, the microsequencer in the 2900 system loads the address from the 16-bit Address/Parameter register. The 6800 initiates a memory controller operation by force branching the 2900 to the beginning address of the appropriate routine in the 2900's microprogram memory.

Diagnostic Register. The Diagnostic Register is the read part of the command register. These two registers have the same 6800 address. The Diagnostic Register is provided for diagnostic purposes only.

Address/Parameter Register. The 6800 passes force-branch addresses and parameters through this 16-bit register. The register is formed by two 8-bit latches, U123 and U141. When the 6800 initiates a memory controller operation, it loads the beginning address of the routine to be executed into the Address/Parameter Register and sets REQ, FBR, and RUN in the Command Register. The microsequencer loads this address and the smart clock clears the REQ and FBR latches. For more information on the use of this register refer to the Smart Clock description.

Status/Parameter Register. The 2900 passes parameters and status information through the Status Register, U043 and U121. At the completion of a memory controller operation, the 2900 asserts a Memory Controller Interrupt (PMCI) and places a status byte in the Status/Parameter Register. If the operation was successfully completed, status 0000 is reported. Otherwise, an error code is returned.

The 2900 passes values back to the 6800 through the Status/Parameter register in two cases. The first occurs when the 6800 force-branches the 2900 to a routine that reports the maximum number of points interpolated by the last ATC (Average-To-Center) or SA (Signal Average) operation. The number of points is passed through this register.

The second case occurs at power-up. The 2900 loads the version number of its firmware into this register. The 6800 reads the value and saves it for responding to the ID? query.

Address Decoding Logic. U023 and the associated components (at the left edge of diagram 19) decode the 6800 bus addresses and enable the appropriate register. When $\overline{\text{STROBE}}$, $\overline{\text{WRITE}}$, and $\overline{\text{PMCSEL}}$ are asserted, the output of U021C goes low. The status of BADR0 and BADR1 determine which register is enabled. For example, to write to the Command Register, the 6800 places 3405 (HEX) on its address bus. $\overline{\text{PMCSEL}}$ and $\overline{\text{WRITE}}$ are asserted. BADR0 is high and BADR1 is low so when $\overline{\text{STROBE}}$ is asserted, SIP1 goes low, latching the byte from the 6800 data bus into U111.

The 2900 Memory Controller

One of the two processors in the 7912AD, the 2900 memory controller, is dedicated to data handling. It stores, processes, and transfers the data recovered from the scan-converter video. It operates in a slave mode, executing routines called by the 6800 MPU in response to front-panel buttons or IEEE 488 bus commands.

The memory controller system is based on TTL microprocessor components in the 2900 family. It is a bit-slice microprocessor in that the CPU is built up from 2901 ICs that each operate on a four-bit slice of the data word. In this sytem, four slices are cascaded for a 16-bit CPU. Other 2900-family components required to support the CPU as well as other logic complete the system. This custom microprocessor resides on the Memory Control and Data Memory circuit boards (A16 and A18).

Anatomy of a Computer

Why is it called the 2900 memory controller rather than a processor or microcomputer? To understand this is to understand the nature of a computer.

The block drawing in Fig. 3-32 is a common conception of a computer, any computer. Instructions and data reside in memory. Various input/output ports provide data paths to external devices. The ALU (Arithmetic-Logic Unit) is where the computing gets done. And the control unit as the executive officer keeps the computer operating in an orderly manner.

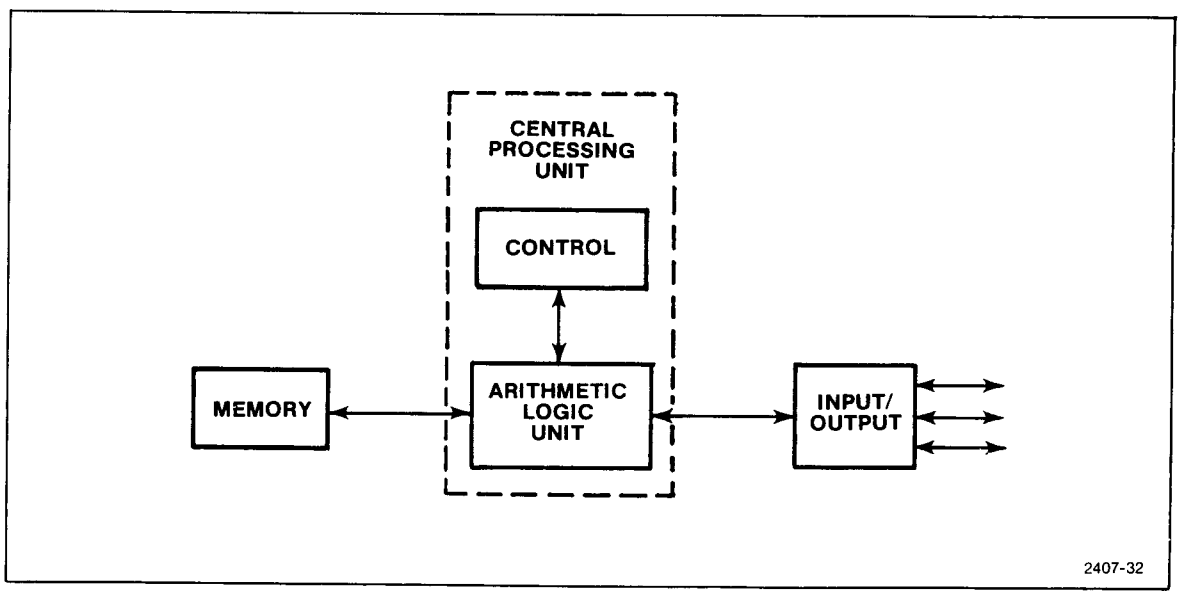
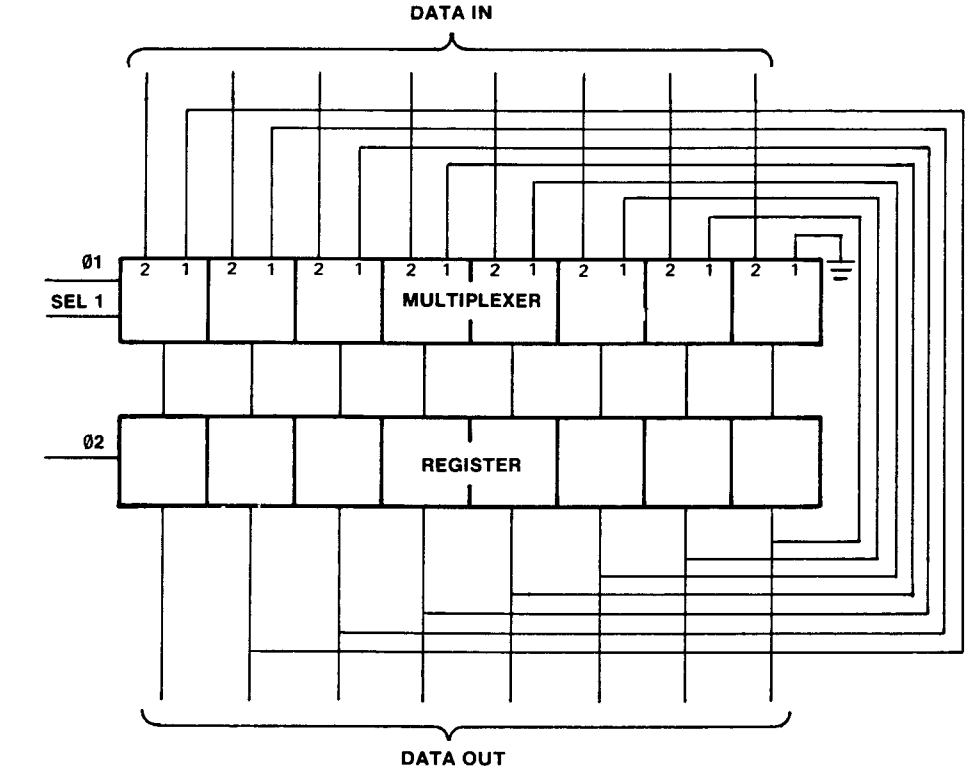


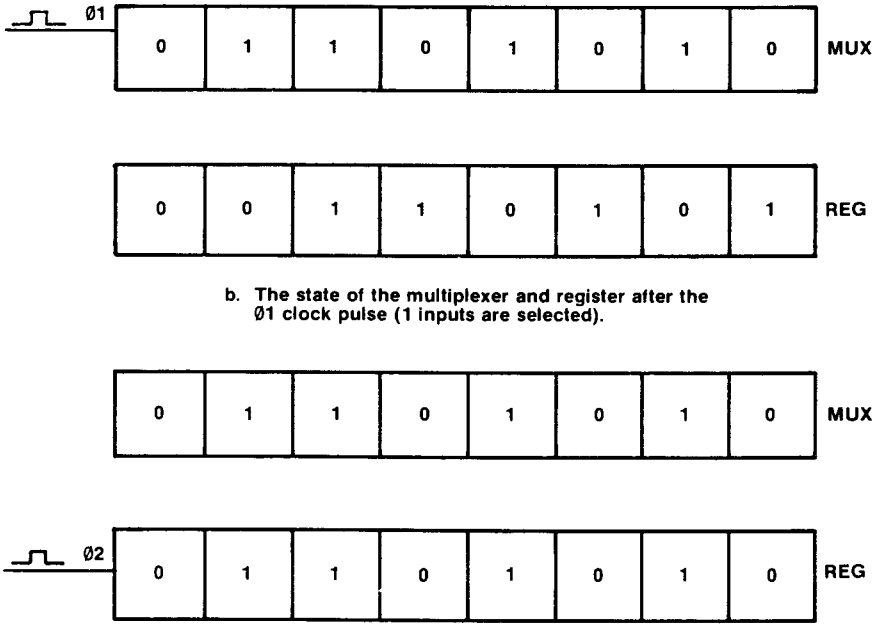
Fig. 3-32. A simple block drawing of a computer.

As the central block, the ALU seems the most important, hence the name, computer. Any computer, however, is really just a memory controller, moving and combining data available in its memory or through its inputs.

Most of a computer's work is actually some form of data handling: transfers in and out of memory, reordering data elements, or modifying data going to or from memory. Even the arithmetic in a computer turns out to be data manipulation. Multiplying by two, for example, requires only a shift-left. If the data resides in a register in the CPU, the shift can be done by a multiplexer connected to the register as shown in Fig. 3-33.



a. A multiplexer selects either the input data or feedback from the register shifted left one bit.



b. The state of the multiplexer and register after the Ø1 clock pulse (1 inputs are selected).

c. State of the multiplexer and register after the Ø2 clock pulse.

2407-33

Fig. 3-33. A multiply-by-two circuit made from a multiplexer and register.

Let's revise our block drawing, then, realizing that the computer is a memory controller, moving and combining data (Fig. 3-34). This concept applies to a wide variety of computers, the differences among them relating to their size and speed of memory, efficiency in moving and modifying data, and the number and speed of I/O channels. These are chosen in different combinations to match the computer's expected workload.

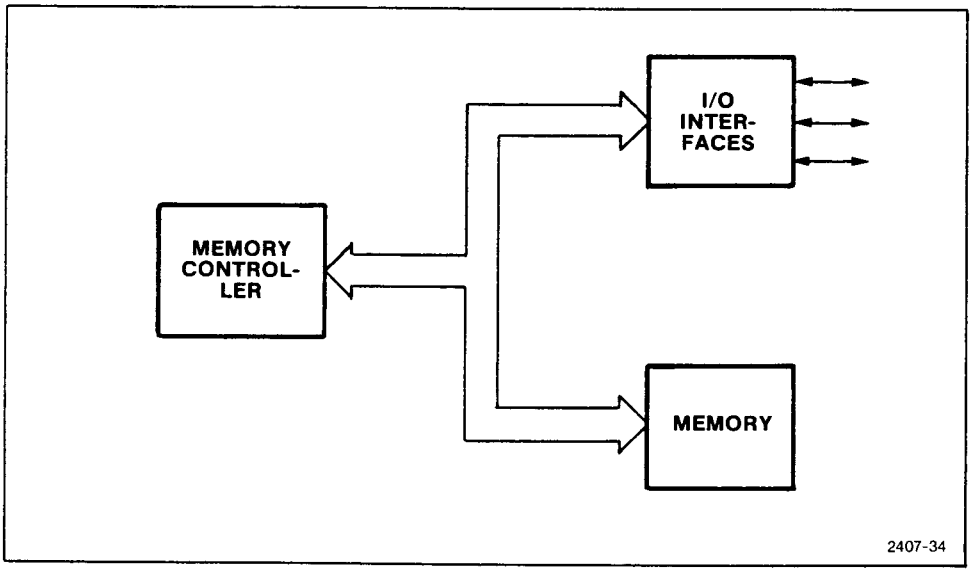


Fig. 3-34. The computer as a memory controller.

The workload of the data memory controller in the 7912AD is primarily fast storage and output of data in parallel with control of several functions in the data acquisition. By virtue of its speed and flexibility, the 2900-family is well-suited to a custom-designed memory controller matched to these tasks.

2900 speed and flexibility derive from several characteristics:

1) A bipolar process (TTL) is used. This allows cycle times considerably faster than MOS.

2) The building blocks in the 2900-family can be put together as desired to handle the unique requirements of the 7912AD. The instruction word can be as wide as necessary to handle data as well as events (Fig. 3-35).

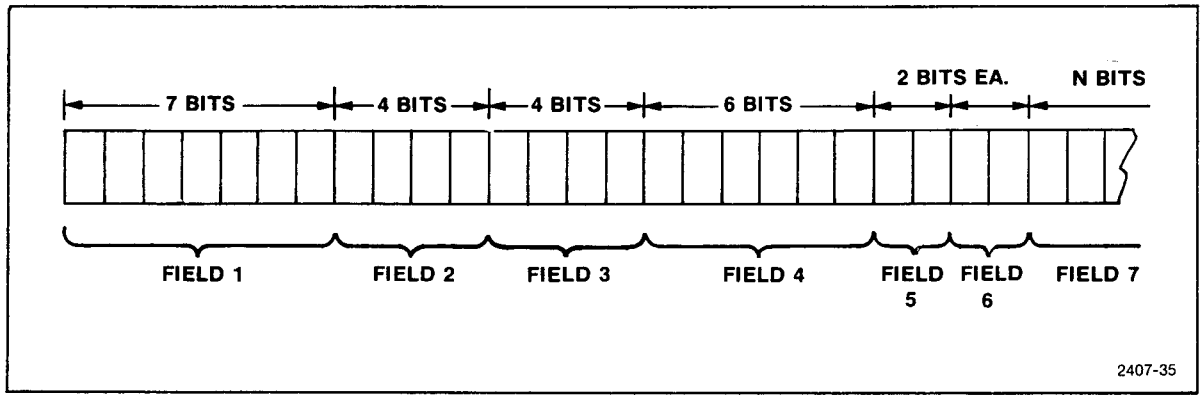


Fig. 3-35. The microprogram instruction word can be as wide as necessary to control microprogram sequencing, ALU modes, and data acquisition events. For instance, field 1 could be defined as a branch address, field 2 as a jump condition select, field 3 as the data source, field 4 as the ALU operation, field 5 as the ALU input select, field 6 as the ALU output select, and field 7 as external control lines.

3) The 2900 system is microprogrammed. The designer is free to create the cycle-by-cycle steps the machine takes to control and manipulate the data.

4) System speed can be boosted by pipelining. This technique fetches the next instruction from the microprogram while the current instruction is executing. As a result, microinstruction access time (time wasted while the memory is addressed) is overlapped with execution time (Fig. 3-36) so that access time does not slow execution cycle time.

What does this 2900 memory controller look like? For a simple block drawing, see Fig. 3-37. The I/O interfaces are not shown -- just the main data paths from the Data Buffer and to the IEEE 488 Interface.

Although many details are omitted, an important difference between this dedicated processor and a general-purpose computer is evident. The program that controls the operation of a computer is often stored in the memory. Program (macro) instructions call short blocks of microcoded instructions that are executed to accomplish the program instruction. In the 2900 system, however, there is no path from the data memory to the control inputs of the CPU. Rather, the memory controller program is stored in microinstruction ROMs. These ROMs are not in the same address

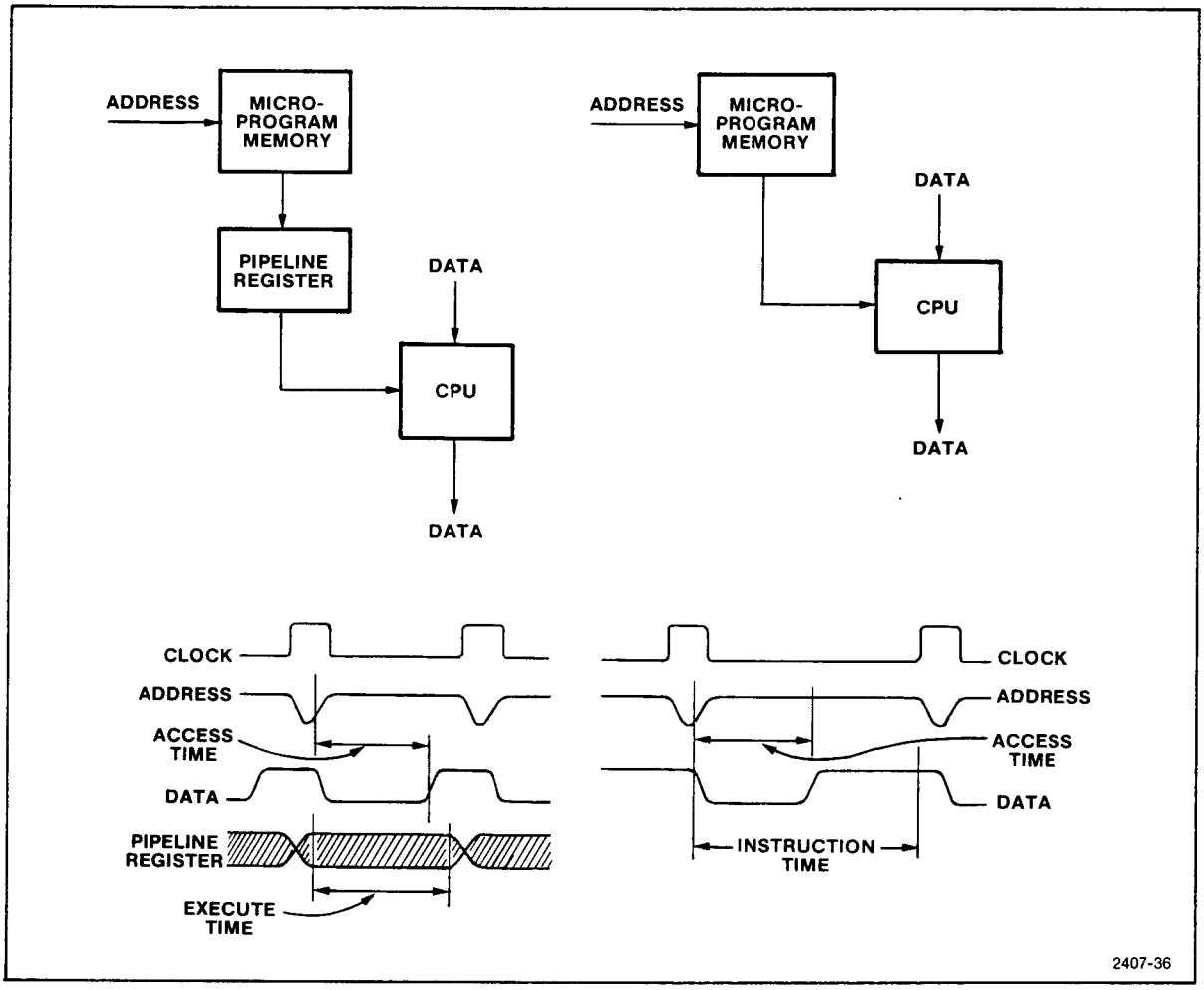


Fig. 3-36. Adding a pipeline register overlaps access and execution time. A new instruction is fetched from memory and made available at the pipeline register inputs while the instruction on the pipeline register outputs is executed.

space as the data memory. The microinstruction program stored in them is accessed under the control of a Microsequencer, which is controlled by part of each microinstruction read out of the ROMs.

The Microsequencer and microinstruction ROMs are not a closed loop, however. Results of CPU operations can modify the microsequencer operation through control logic to branch within the program. Also, different memory controller operations are initiated by the 6800 MPU. The microinstructions can be thought of as a set of subroutines run on the

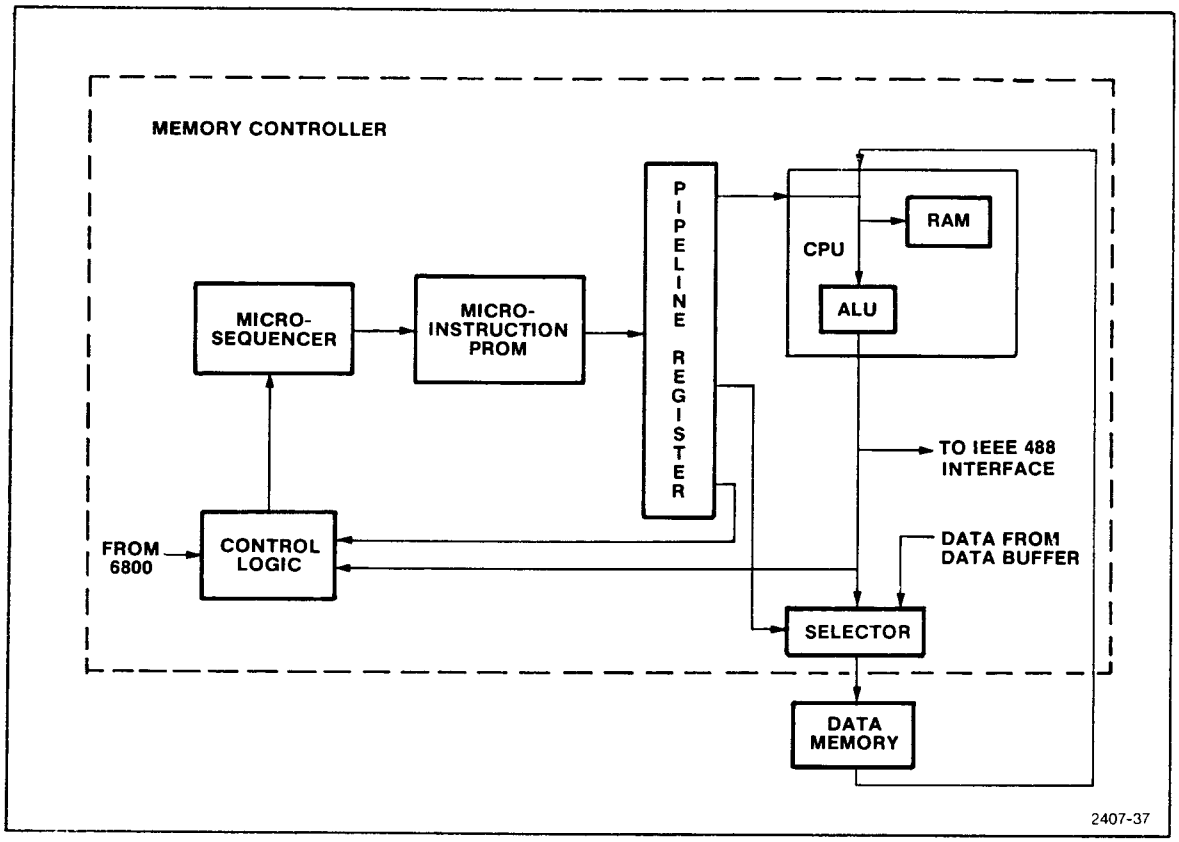


Fig. 3-37. A simple block drawing the the 2900 memory controller system.

2900 system, called by the 6800, and run in parallel with 6800 operations.

The Microsequencer

If we are going to fathom the mysteries of the 2900 system, we must plumb the depths of the microsequencer. It is the microcode sequencer that supports the programming tools used with the memory controller. The microsequencer's job is to select the next address, the address of the next microinstruction to be fetched from ROM. What are the programming tools supported by the microsequencer?

We've already mentioned branching, that is, jumping within the program to a microinstruction other than the one in the very next ROM address. In an unconditional branch, the program jumps without question

to the new address. Similar is the handy jump-to-subroutine. In this case, though, we remember whence we came and return there when done. This allows the program to use, as needed, common sets of microcode without repeating them.

The faculty of the memory controller that sets it apart from lower-order machines, however, is the conditional branch. It is in deciding whether and where to branch that the memory controller becomes a computer. The program can branch to an appropriate point depending on the results of an ALU operation or an external condition.

The microsequencer, shown in Fig. 3-38, supports these functions. It also includes an incrementer that merely bumps the current instruction address by one to make the next address. This is a continue -- the opposite of a branch.

The 2909. Let's look more closely at the microsequencer. It includes a microprogram counter (uPC), stack, and multiplexer. It selects the next address from the uPC, stack, or one of the external sources -- the 6800 or a field in the microinstruction word -- to control program execution.

The internal organization of the microsequencer is shown in Fig. 3-39. Input and output pins are labeled as they are on the schematic diagrams. Only one 4-bit wide slice, a single 2909 IC, is shown. Three are used to select the 12-bit wide address of the next microinstruction. The slice shown provides bits 4 through 7 of the address.

The microsequencer slice shown in the figure is U643 on the Memory Control board (A16), diagram 20. The direct inputs to the multiplexer, DD4 through DD7, come from latches addressed by the 6800 MPU (called the Address/Parameter Register). This is the path used by the 6800 MPU to initiate memory controller operations. The data can be thought of as a vector: it is a ROM address containing a jump instruction to get the memory controller into the routine for the desired operation. It takes more than this address, however, to initiate a memory controller operation as we shall see.

The address register inputs, BRA4 through BRA7, are fed back directly from a microinstruction field for branch addresses. The branch address is latched in the microsequencer (bypassing the pipeline register) and applied to the multiplexer R inputs.

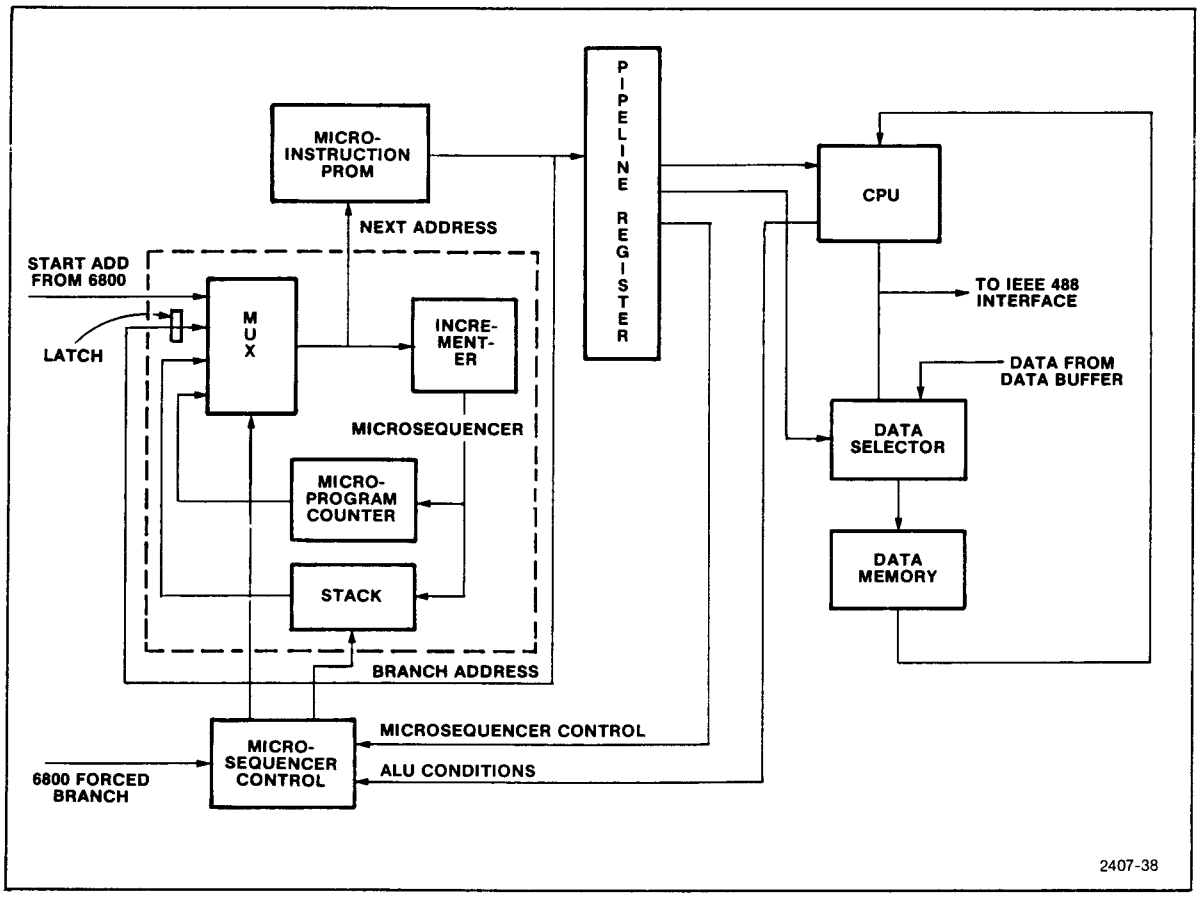


Fig. 3-38. A block drawing of the 2900 memory controller showing the microsequencer.

S inputs to the multiplexer come from the chip's internal stack. The stack can hold up to four files (a file is a microinstruction address stored as part of a branch operation) for subroutine nesting -- subroutines within subroutines. The address comes from the microprogram counter register and is automatically stored and read under control of the clock and the microsequencer control lines. The stack pointer remembers which address was stored last.

The uPC inputs to the multiplexer are the next address (one plus the current address) from the microprogram counter register. The next address is generated by the incrementer, which merely adds one to the current address output by the microsequencer when clocked. Incrementer carry lines are provided to cascade the three 2909s.

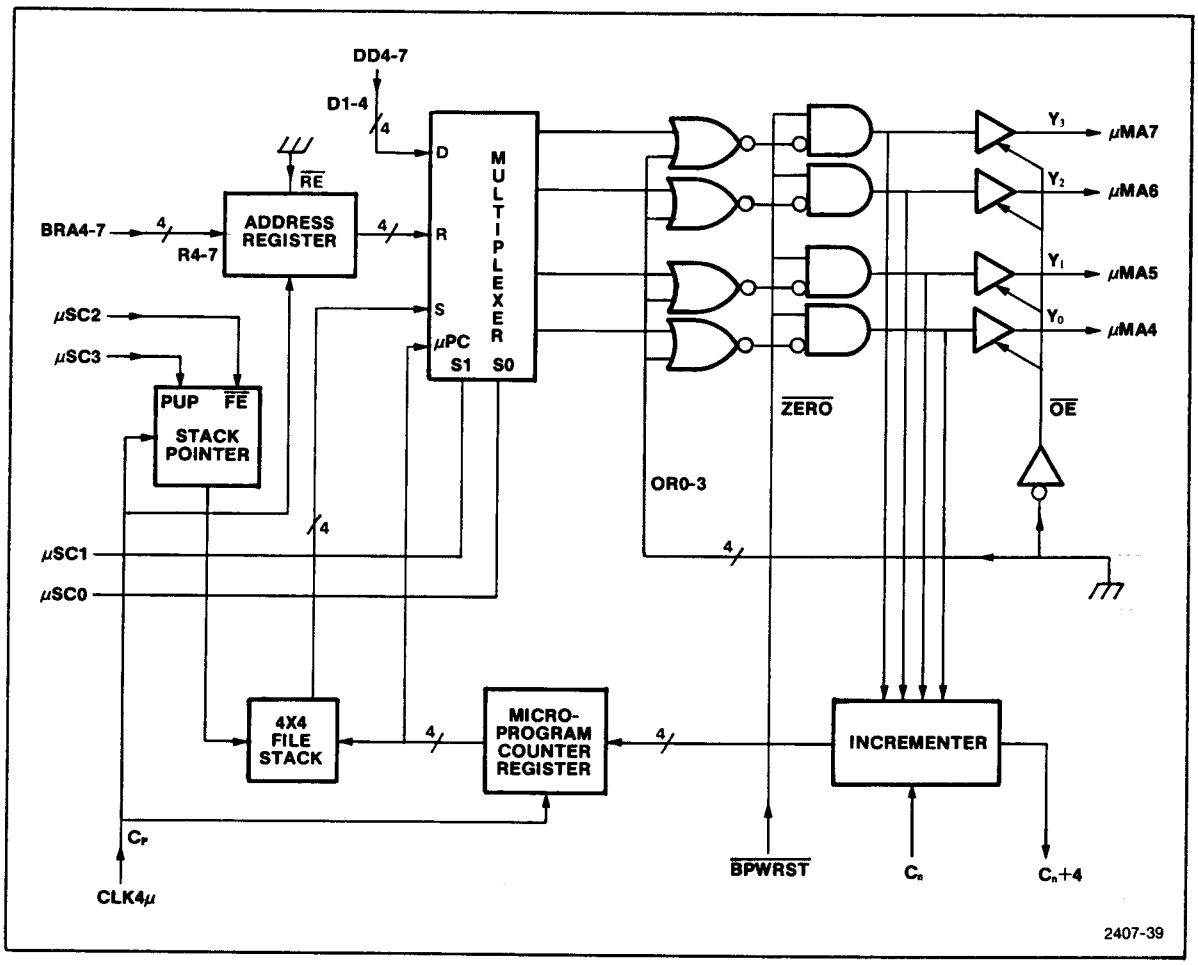


Fig. 3-39. The 2909 microsequencer.

With four inputs to select from, the multiplexer can channel the desired next address to the microinstruction ROMs depending on the microsequencer control lines. The outputs are gated onto the microinstruction address lines because control lines OR0 through OR3 and output enable are grounded. This assumes power is up, so that $\overline{\text{BPWRST}}$ is not asserted.

Microsequencer Control. The microsequencer control lines gate the proper input through the multiplexer and control the stack; the control code is shown in Table 3-16. The lines are set by the outputs of a microsequencer control ROM addressed by a field in the microinstruction word and two other lines. One line is set by the 6800 MPU to force-branch the microsequencer at the beginning of a memory control operation. The

other line comes from the condition code selector. It indicates whether the condition is fulfilled for a conditional branch.

TABLE 3-16

MICROPROCESSOR CONTROL

S_1	S_0	Multiplexer Input	$\overline{FE}$	PUP	Stack Operation
L	L	Microprogram Counter	H	X	No change
L	H	Address Register	L	H	Increment pointer, push
H	L	Stack			current count onto stack
H	H	Direct Inputs	L	L	Pop stack, decrement pointer

The control ROM is U721 on the Memory Control board (A16), shown on diagram 20. Its MSB address line, FBR, overrides the other address inputs when set. FBR is set when the 6800 MPU sends a byte to the Command Register (6800 address 3405) with bit seven equal to one. The bit is clocked into U041B (diagram 19) by the 2900/MPU port decoding logic. FBR true causes the ROM to output the control signals for a branch, selecting the branch address from the direct inputs.

If FBR is not true, the mode control bit in the Pipeline Register (P43) overrides the other address inputs when cleared. P43 equal to zero signals a CPU, rather than microsequencer operation, and causes the ROM to output the code for a continue. This selects the microprogram counter as the next address and causes no change to the stack.

The pipeline register microsequencer control field and the COND line control the ROM addressing when FBR is clear and microsequencer mode bit is set. P32 in the pipeline register indicates how the COND line is to be treated: when cleared, branch if COND is true; when set, branch if COND is not true.

Synchronous Conditions. Selectors U701 and U703 control the COND line. The selector inputs are synchronous conditions: changes occur either in step with the microsequencer or while the 2900 memory controller is halted.

Conditions SYNCXDR, SYNCYDR, and SYNCRDY are synchronized at U441 (also on diagram 20) by the microsequencer clock. HRDY is a 2900 memory controller output flag from the output interface control state machine.

YDR and XDR are outputs from the data buffer output state machine that alert the 2900 memory controller that data is available.

SLOSWP is a bit in the Command Register that can be set by the 6800 MPU in the same manner as it sets FBR. SLOSWP alerts the 2900 memory controller that the time base sweep is 5 microseconds/division or slower. When set, the 2900 uses a slow-sweep algorithm to merge the data detected on the target during a digitize operation. The two MPU flags are not used by the 6800 MPU and are ignored by the 2900 memory controller routines.

ALU status flags are selected by U703. Combinations of these flags are also gated to the selector as signed conditions. For instance, the exclusive OR of N (negative) and V (overflow) is sensed as the A less than B condition; ORed with Z by U713D, it becomes the A less-than-or-equal to B condition.

Bit 31 of the microinstruction word enables either U701 or U703. The value of bits 28 through 30 in the microinstruction word determines which input condition is selected.

To review: whether a condition is to be tested, the condition to be tested, and the microsequencer response to it are determined by bits in the microinstruction word. These bits address the condition selectors and the microsequencer control ROM to put the desired code on the microsequencer control lines. Thus, the decision-making power of the 2900 memory controller is contained in two fields in the microinstruction ROM word -- the microsequencer control field and the condition select field.

The Microinstruction Word

Now that we are acquainted with the microsequencer, let's proceed to consider the other blocks in the 2900 memory controller system. These are shown in the pullout block drawing in the diagrams section. Central to the drawing and central to the memory controller system is the pipeline register. Although it appears to be a long, narrow pipe, it is really a short, wide conduit connecting the microinstruction memory and the other blocks in the system. It is this conduit that applies the concept of pipelining introduced earlier.

Pipeline Register. The pipeline register is clocked by the same signal as the microsequencer. When clocked, the pipeline register has the current microinstruction on its outputs and the next instruction on its

inputs. The next instruction on its inputs is set up by the microsequencer, which always supplies the next address (address of the next microinstruction). Following the clock pulse, the microsequencer changes its outputs to address the succeeding instruction according to its control lines. Meanwhile, the pipeline register transfers the next microinstruction from its inputs to its outputs, effecting pipelining.

Since the microinstruction word is available to the system only at the pipeline register outputs, the microinstruction word and pipeline register are commonly used to mean the same thing.

Located on the Memory Control board (A16), the pipeline register is shown on diagram 20 connected to the outputs of the microinstruction ROMs. The ROMs are easy to spot by their address lines labled as uMA0-uMA7 and uA8-uA11. The bottom four bits of the 44-bit wide microinstruction word are not used. The other bits are shown with a variety of names relating to their function or their position in the word.

Microinstruction Format. Although the pipeline register is wide, it is not wide enough to dedicate a field for every purpose. Many bits do double duty; their meaning depends on the mode control bit, the pipeline register MSB. When this bit is set, the microinstruction controls a microsequencer operation; when clear, the microinstruction controls a CPU operation. The fields in the microinstruction for each mode are shown in Fig. 3-40.

Some of these fields have already been discussed. Others, such as the CPU mode fields and the external variables, remain; they are discussed with the circuitry they control -- the CPU, data memory, and Data Buffer. More detail on the bits in these fields is given in the pullout Pipeline Register Format drawing in the diagrams section. The bits are grouped according to an assembler format used to develop the microcode.

The Smart Clock

Up to this point, a valid clock signal has been assumed. In a complex system such as the 2900 memory controller, however, the clock is neither simple nor singular; a number of clock signals are used. Let's see where they are generated.

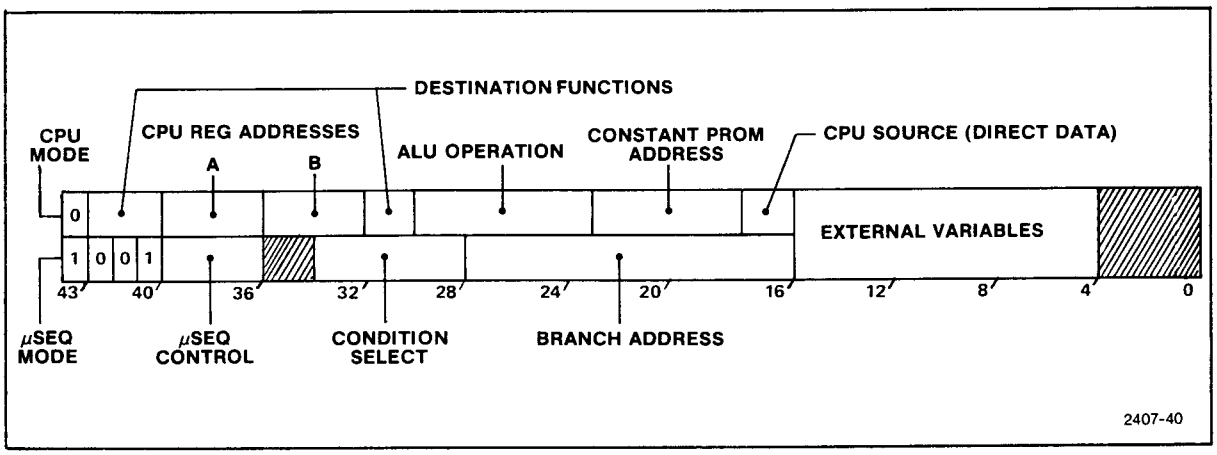


Fig. 3-40. 2900 memory controller microinstruction fields.

All clock signals used by both processors in the 7912AD originate in an 80 megahertz crystal oscillator on the Data Buffer board (A20) shown on the bottom of diagram 25. The clock that drives the 2900 is first divided by four by two cascaded D flip-flops, U446A and U446B, on the same diagram. CLK20 then drives the state machine on the Memory Control board (A16) that occupies most of the left half of diagram 21. Here the clock is divided by five for the microsequencer and CPU. This state machine must perform much more than a simple divide-down, however. To understand this, we must realize that although the 2900 runs faster than most microprocessors, its clock rate of 4 megahertz is still not fast enough when it responds to external events.

One component of the 2900 system that increases its speed, the pipeline register, slows it down when responding to a change in an external condition. Consider first of all that the 2900 can react only on the following clock cycle. With a 4-megahertz clock, that is a delay of up to 250 nanoseconds. Because microinstructions are pipelined, it takes two clock cycles for the first microinstruction addressed in response to an event to reach the pipeline register output. This adds up to a response time as great as 500 nanoseconds.

For some events, such as data ready from the Data Buffer, the 2900 must respond much faster. Otherwise, storage of data acquired from the scan converter would be slowed; since the target is read under control of the clock, delay in storing the data can not be allowed. A faster

response time can be achieved by shifting the burden to the clock, rather than the processor.

Enter the smart clock. The smart clock in the 2900 memory controller system, then, does more than divide down the clock rate. It provides fast response to asynchronous conditions and also synchronizes the system when it shifts gears for a forced branch.

The State Diagram. To understand the operation of the smart clock state machine, let's analyze the state diagram in Fig. 3-41. It may be useful to refer to the 2900 Memory Controller pullout diagram while studying the smart clock state machine to relate it to the other blocks in the system.

First, a word about the state diagrams in this manual. They resemble a flowchart. Diamonds represent decision points; a label indicates the qualifier. Boxes represent machine states; a label indicates that the machine signal with that label is asserted, while a blank box indicates the signal is not asserted. Values of the state variables are shown to the upper right of each box.

In the smart clock state machine, the X, Y, Z, and T outputs of the random logic at the left of diagram 21 form the state variables. These variables are combined by the gates at the J input of U511A as HECLK and clocked into the flip-flop by CLK20 to set CLK4, the main output of the smart clock state machine. CLK4 is made available as CLK4u for the microsequencer and CLK4CP for the CPU. The other signal, called HECLR on the state diagram, is decoded and applied to U415D to assert $\overline{\text{CLRREQ}}$.

In states **a** through **c**, the CLK4 input is high, going low during states **d** and **e**. These states compose the run loop, dividing down CLK20 by five for a 4 megahertz clock that is high for 150 nanoseconds and low for 100 nanoseconds. Because the smart clock outputs come from flip-flips (not directly from HECLK and HECLR), they lag one state behind HECLK and HECLR: CLK4CP, for instance, is high during states **b** through **d** and low

A trip around the run loop starts with the state variables at 0000 and HECLK high. The random logic that generates the state variables guarantees that the machine makes state transitions according to Fig. 3-41. This logic senses the values of the variables and the smart clock inputs to assign each variable's next value.

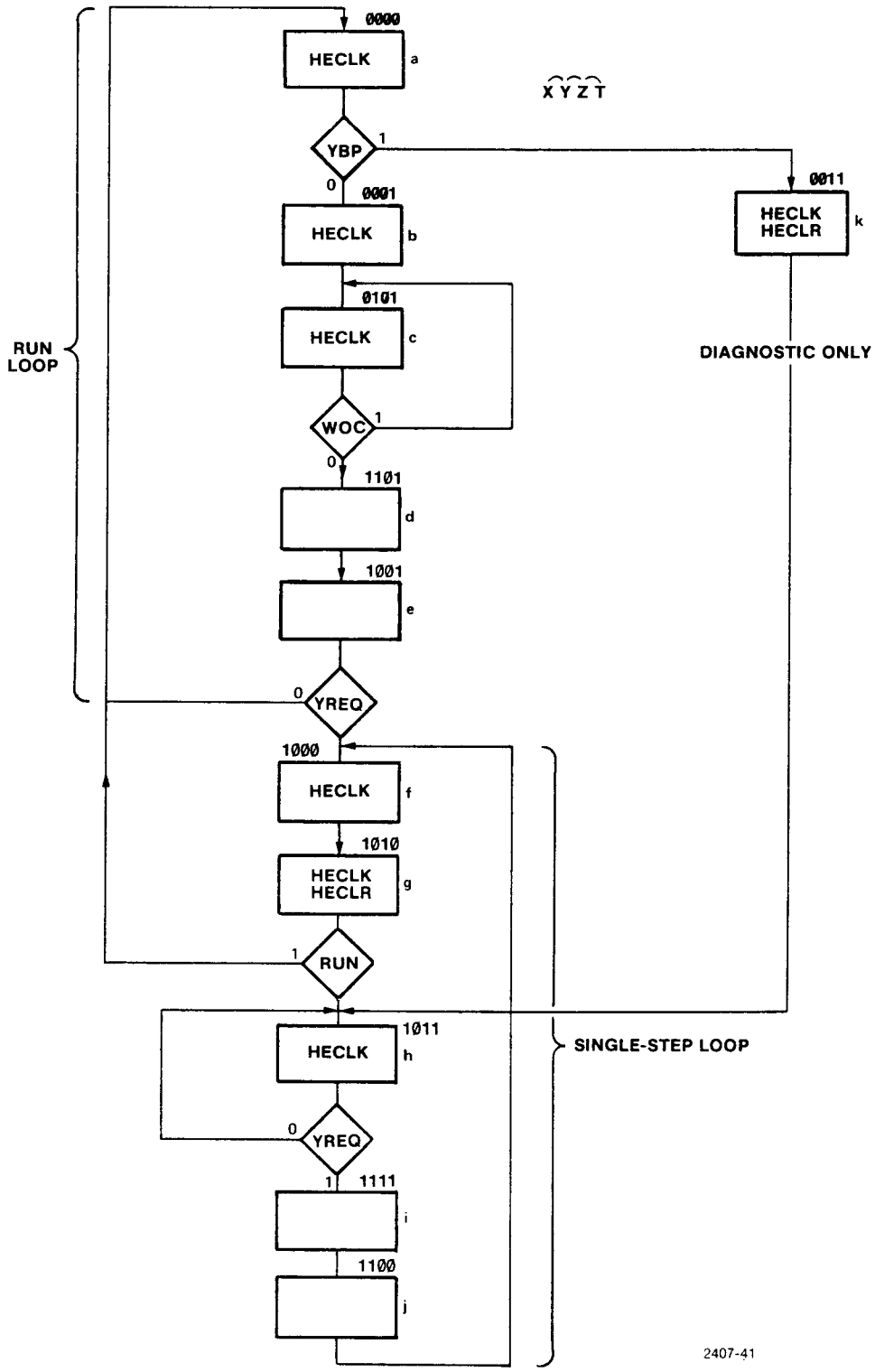


Fig. 3-41. The 2900 memory controller smart clock state machine diagram.

To move from state **a** to **b**, U231C senses BP (breakpoint). Since BP is hardwired false during normal operation, a high is placed on one input of NAND gate U221A. U221A is enabled to pass the condition of BP because the X variable is low, placing a high on pin 1 of U221A. Thus, BP low puts a low on the J input to U233A while the inputs combined at U233A's other input keep the Q output high (assuming a run condition). This results in no change in Z on the next clock, the correct value of Z to advance to state **b**. A change in Z to a value of 1 would have branched the machine to the diagnostic path. The zero values of the state variables X, Y, and Z are combined with input RUN to form the inputs to U233B that force T to change from 0 to 1. Similar analysis shows that X and Y do not change given our present state, so the state variables assume the value 0001, and, therefore, the machine moves to state **b**.

The next decision point is reached in state **c**. The wait-on-condition input true puts the smart clock on hold. This is the trick used for fast response to events sensed by the asynchronous condition selector. The smart clock loops until the event occurs and then proceeds to state **d** when the event occurs. X is the controlling variable; it is 0 in state **c** and remains 0 until wait-on-condition is unasserted. When U211A senses both its inputs high, its output goes low. this is gated to the J input of the X flip-flop because Z is false, and X changes to 1 on the next rising edge of CLK20. Meanwhile, U311B's other input is held high because Z is false and Y is true.

Successive clock pulses move the state machine to the next decision point where the request bit in the Command Register is tested. With all inputs high at U103B, X changes from 1 to 0 on the next clock; the smart clock loops to state **a** because the values 1001 force Y, Z, and T to 0. If the request bit is set, pin 13 of U103B is low so X does not change state. In this case, the smart clock branches to the single-step loop used for diagnostics and for passing branch addresses and parameters to the 2900 system.

The 6800 MPU controls the smart clock in the single-step loop with the request bit; the state machine hangs in state **h** each time through the loop until this bit, cleared by U415D in state **g**, is reset. When the 6800 MPU finishes the task requiring single-step, it sets both the run and request bits, and the smart clock jumps from state **g** to **a** to enter the run loop.

Asynchronous Conditions. The smart clock depends on the asynchronous condition selector to call the signals when it reacts to an external event. This selector is U603 on diagram 20. Its inputs are the true and false conditions of X data ready, Y data ready, output interface ready (HRDY), and data handshake complete ($\overline{\text{BYSENT}}$). The selector is addressed by the condition select bits in the pipeline register and its output is enabled when NOP (not operation cycle) is false and the wait bit in the pipeline register is set during a microsequencer operation (bit 43 set).

2900 memory controller routines that use the asynchronous selector first execute all instructions up to the first instruction handling the event. A wait-on-condition instruction is then executed that enables the selector and addresses the desired condition. For instance, the 2900 memory controller in preparing to store X data would address input D4 (P30 high, P29 and P28 low). The selector in turn would assert wait-on-condition (pin 5 high and pin 6 low) until the X data became available. At that point, pin 5 would go low, unasserting wait on condition, and the smart clock would move from state **c** to **d** so the memory controller could execute the service routine.

Stop and Go -- FBR. To start a memory controller operation, the 6800 force-branches the microsequencer to the starting address. To do this, it sets the request bit in the Command Register, shunting the smart clock into the single-step loop. There it hangs in state **h** as explained earlier while the 6800 MPU loads the starting address into the latches at 6800 addresses 3406 and 3407. The 6800 then sets the FBR and REQ bits and the smart clock proceeds around the single-step loop to the RUN test. If the 6800 MPU has also set the RUN bit, the smart clock jumps back into the run loop.

The 6800 may have a parameter to pass for the memory controller operation, such as how many waveforms the DIG SA, <NR1> command requests be averaged. If so, RUN is not set and the smart clock hangs again while the 6800 MPU loads the parameter, then sets RUN and REQ to restart the smart clock.

However, if two parameters are to be passed, such as the trace width and rate of change allowed for EDGE processing, the 6800 MPU again clears RUN when it sets REQ. The previous REQ would have caused the clock to go low and then high before hanging high. During this single-step, the microsequencer would have jumped from the start address to the first microinstruction in the routine, and the CPU would have stored the first parameter in an internal register. At that point, the smart clock waits

again for the 6800 to load the second parameter. When ready, the 6800 MPU sets both RUN and REQ and the memory controller is off and running as the smart clock jumps back into the run loop.

These sequences for forced-branch are summarized in Fig. 3-42.

Strictly speaking, FBR is asserted before REQ and RUN as far as the 2900 system is concerned. FBR is latched on the leading edge of the 6800 MPU strobe pulse, while RUN and REQ are latched on the trailing edge. The delay arises because decoder U023 on diagram 19 asserts a negative signal when the Command Register (6800 address 3405) is addressed and the negative-going strobe is asserted. The negative transition at pin 5 of U023 is inverted by U031A on the same diagram and applied to the clock input of the FBR latch, U041B. However, U041A where REQ is latched and U111 where RUN is latched are not clocked until the negative-going address select line returns to its off (high) state.

The 100-nanosecond delay this causes makes sure FBR can assert NOP through U203C on diagram 21 before the smart clock can switch low in state i. NOP prevents the CPU from writing into any of its registers by asserting a destination code of 001 on I8, I7, and I6 of the CPU chips on diagram 23. This is equivalent to the code in bits 42 through 40 of all microsequencer operation microinstructions (with the same end in mind): the CPU does not have to be shut off during microsequencer operations, such as forced branch, because the ALU outputs are not saved. In the case of forced-branch, NOP lets the clock's single step flush the pipeline register while advancing the microsequencer and pipeline register. This sets up the pipeline register output with the microinstruction from the starting address by the time the clock enters the run loop. Note that power-up (PON) is sensed on diagram 21 for the same purpose.

A variation on this forced-branch sequence is necessary for data memory output to the IEEE 488 interface and is discussed as part of that topic.

The 2900 CPU

The 2900 memory controller CPU is based on the 2901 high-speed, bipolar, bit-slice microprocessor. Four slices are cascaded to make the 16-bit CPU. Each contains a four-bit slice of the 16 general purpose registers and the arithmetic-logic unit (ALU), along with shifters, decoders, and multiplexers used with the registers and ALU. Fast carry look-ahead is implemented outside the 2901s to take advantage of their speed.

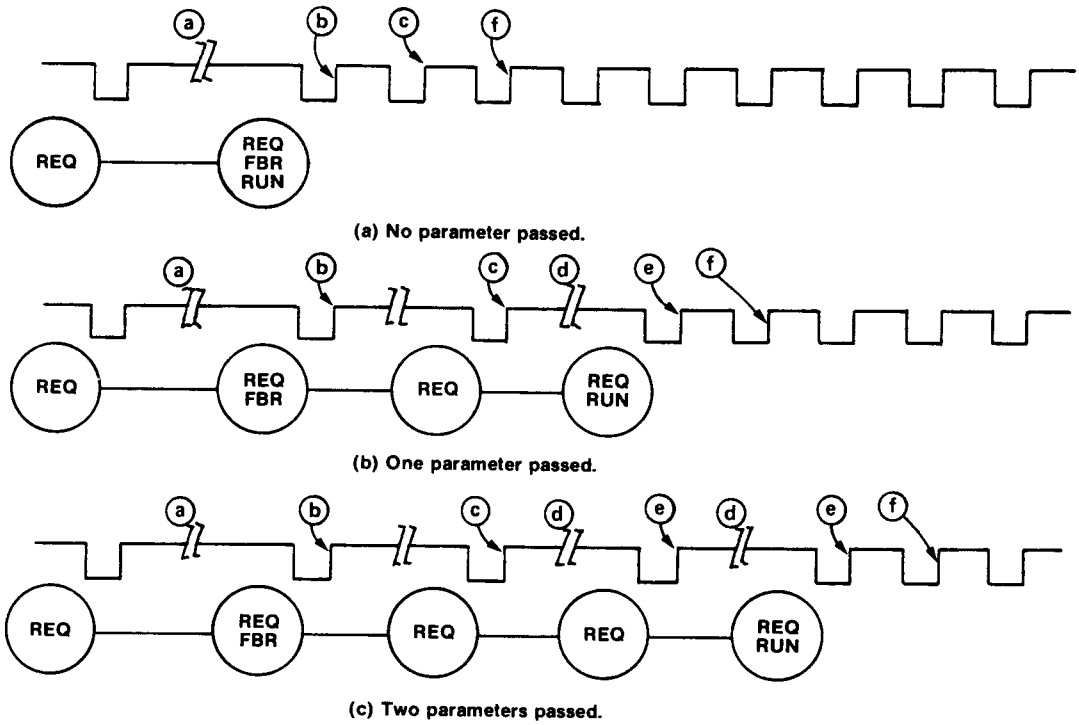


Fig. 3-42. 2900 memory controller forced-branch sequence.

Nine-bit microinstruction words select ALU source operands, ALU function, and destination of the ALU results. The ALU sets various status flags after an operation.

This is a bare-bones microprocessor with a simple instruction set. However, a powerful processor can be built on the 2901 architecture. This potential exists because the 2901 is microprogrammable. Its power can be exercised when the instruction word is embedded in the full 2900 system microinstruction and the CPU is supported by the rest of the 2900 memory controller system.

ALU Data Sources. Let's look inside the 2901; refer to Fig. 3-43 for a block drawing of the microprocessor slice. A less detailed view is shown on the 2900 Memory Controller pullout diagram that relates the four 2901s as a 16-bit unit to the rest of the system.

Data for the ALU operands can be selected from five sources. These sources are: external (direct), internal registers addressed by the A and B ports, all zeros, and the internal Q register. The source-select bits are combined with the ALU function codes to make the assembler ALU operation field shown on the Pipeline Register Format pullout diagram. These are bits 29 through 24, called I5 through I0.

ALU operations supported by the assembler are shown to the right of the bracket under ALU Operation on the pullout diagram. Each operation is converted by the assembler using the codes to the left of the bracket. For instance, to add the contents of the registers at the A and B addresses (A+B) requires that A be the address of the source for the ALU R input and B be the address of the source for the ALU S input. The code is 001 in bits 26 through 24. To add R and S requires 000 in bits 29 through 27. The CPU carry input, CN, is cleared by bit 23 in the pipeline register. To increment A would require 0001100: select zeros for the source of R and the register addressed by A for the source of S, then carry one and add the R and S inputs.

The internal registers addressed by A and B are used to store parameters passed from the 6800 MPU, pointers to data arrays, and temporary variables. The Q register can be used as a 17th general purpose register, but in addition it has unique shift capabilities. The Q register can shift a word in parallel with, or in conjunction with, the other RAM in the CPU; more on this under ALU Outputs.

External data is input through a selector controlled by bits 17 and 16 in the pipeline register, PCPSRC1 and PCPSRC0. These bits control dual four-to-one selectors across the top of diagram 23 that connect to the 2901 direct data inputs. This allows the microprogram to input data to

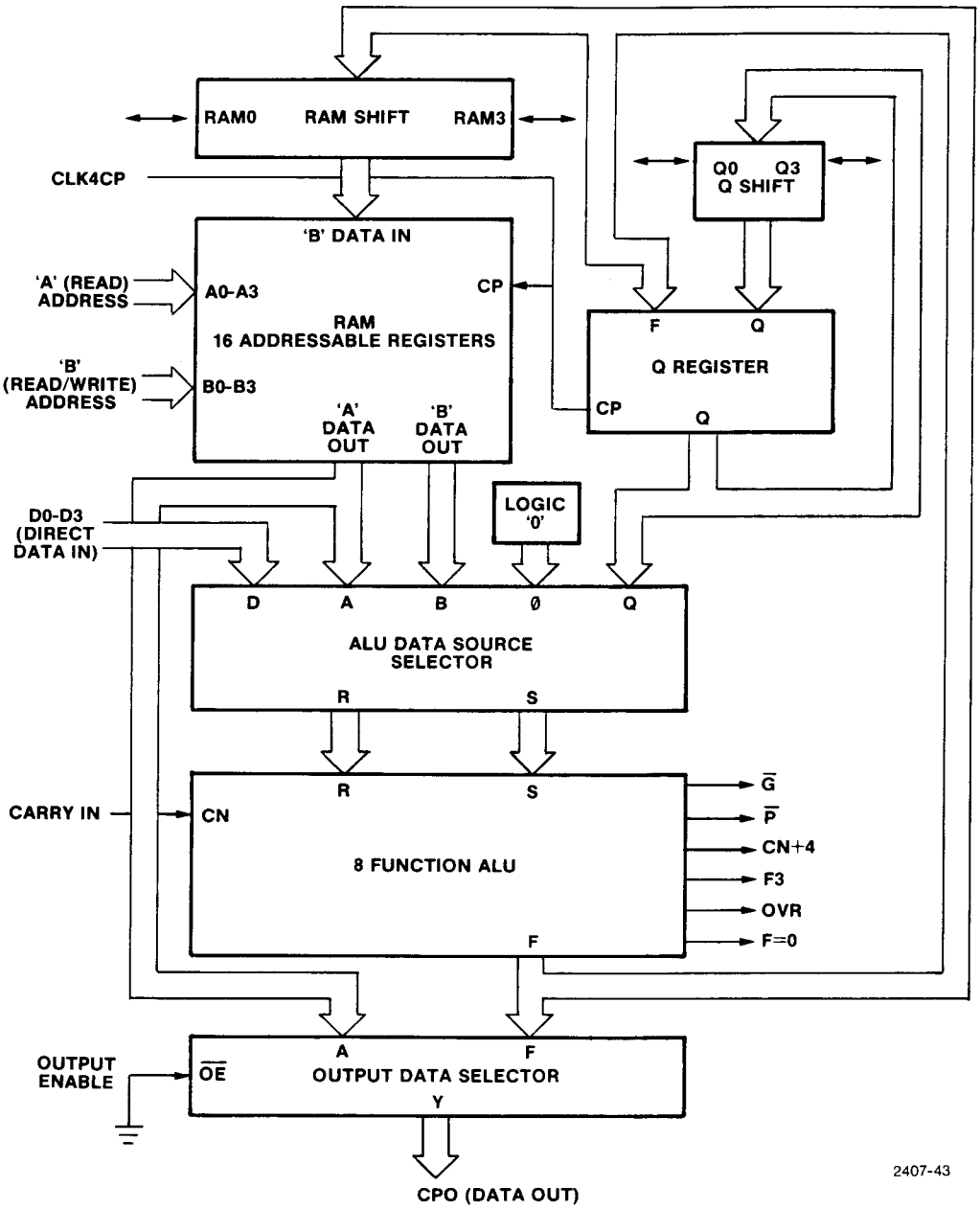


Fig. 3-43. The 2901 microprocessor slice.

the ALU from the data buffer (TDØ-7), the data memory (DMIØ-15), the constant ROMs (KDØ-15), or the 6800 MPU (DDØ-15).

The path from the 6800 MPU is used to pass parameters to the 2900 and to input the defects array (LOAD command). The constant ROMs hold numbers such as the starting addresses of the data memory arrays, the 2900 firmware version, and error codes.

ALU Outputs. The destination functions field in the pipeline register directs the ALU output to an internal register and/or the CPU output. This field combines bits 42 through 40 (control lines I8 through I6) and bits 31 and 30 (shift mode).

Pipeline register bits I8 through I6 are gated with NOP at the bottom of diagram 23 as explained earlier (near the end of the discussion of FBR). I8 through I6 control the ALU output and CPU register shifts. For instance, 000 is coded in these bits by the assembler instruction FTOQ; this loads the ALU output (F) into the Q register. 100 in the SRQBO instruction shifts right both the ALU output (storing it in the register at address B) and the Q register.

While I8-I6 go directly to the CPU, shift mode bits PSHIFT1 and PSHIFT0 control external selectors. These selectors, U832 and U824 on diagram 23, handle the end points of the cascaded CPU registers. Four modes are implemented for either left or right shifts: shift in 1, shift in 0, rotate, or arithmetic shift.

Within the 16-bit word, CPU shift lines Q3, Q0, RAM3, and RAM0 are organized to shift bits in or out automatically at the edge of each register slice. Q3 becomes an output while Q0 becomes an input to shift the Q register left. They reverse roles to shift Q right. RAM3 and RAM0 perform similar roles when one of the 16 registers is selected by the destination function during a shift operation. The shift lines are tri-state; when not selected, they go to their high-impedance state. The selectors at the end points ensure the full register is treated correctly; also, the selectors allow a 32-bit shift to be accomplished by cascading the Q and B registers.

Let's try a 16-bit shift before tackling 32 bits. I7 in the destination field points the direction of the shift; it is set by the shift-left code and cleared by the shift-right code. Say a zero is to be shifted into the B register from the right. The full destination field would be 11100, the SLBØ assembler instruction. I7 set disables U832 and enables U824. With PSHIFT1 and PSHIFT0 cleared, ground is selected as the input for the low-order bit slice (U922) RAM0 input -- the LSB.

If a rotate had been selected, PSHIFT1 would have been set and PSHIFT0 cleared, selecting ES3 as the U922 RAM0 input. ES3 is the high-order slice (U1322) RAM3 output, so the selected register's MSB is rotated into its LSB. And so on.

When an arithmetic shift is selected, the Q register and the register at address B are linked for a full 32-bit shift. The B register contains the upper 16 bits and the Q register the lower 16 bits. Let's look at a 32-bit divide by two, for example. This is the SRQBA (shift right Q and B) instruction, 10011. The F output is shifted right and stored at the B address while the Q register is also shifted right with the LSB of the B register transferred to the MSB of the Q register. Of course, B must have been selected as the ALU output by 0000011 in the ALU operation field.

Both the A and B shift selector lines are set high by the pipeline register to correctly relate the B and Q registers. This enables U832 to shift U1322's F3 output into its RAM3 input, preserving the MSB sign bit. U1322's Q3, the midpoint in the 32-bit word, shifts in the ES2 output of U832, which is asserting the state of the U922 RAM0 line. Q0, the 32-bit LSB, is lost.

The CPU output (Y) is always enabled. It asserts F, the result of the last ALU operation, for all instructions except FTOBA (F to B, output A). This instruction uses the path from the register addressed as A to the output Y; it bypasses the ALU.

The active edge of the CPU clock, CLK4CP, is low-to-high. The registers are enabled for writing during the low time and latch the data when the clock goes high.

Status Flags. The zero (F=0) flags of the CPU slices are tied together in an open-collector OR; all must be high to indicate the result of the last ALU operation is zero.

F3, MSB of the most-significant CPU slice, is used for the sign (N) of 16-bit 2's complement arithmetic.

OVR from the most significant slice is used for the CPU V (overflow) flag. The exclusive-OR of the carry in and carry out of U1322's F3 bit, it indicates the result of a 2's complement arithmetic operation overflowed into the sign bit.

CN+4 (carry out) from U1322 is output as the CPU carry flag. Special carry-propagate outputs from the other CPU slices are sent to the look-ahead carry generator, U822. This IC generates the carry inputs for the

three higher-order CPU slices to save the time it would otherwise take for a carry to ripple through the CPU.

Memory Controller I/O

The 2900 system engages in four kinds of I/O: 1) 6800 MPU I/O, 2) data memory transfers, 3) output to the IEEE 488 bus, and 4) output to the XYA display.

6800 MPU I/O. Input from the 6800 MPU to kick off memory controller operations is received by the microsequencer and the smart clock and has already been discussed with those topics. Another case of input from the 6800 occurs when the 7912AD LOAD command is executed. The 6800 handshakes the defects array from the IEEE 488 bus and assembles each byte pair into a defect value. It force-branches the 2900 to a routine that stores each value when available. The 2900 reads the value in the manner described in the FBR discussion for passing a single parameter; the value is stored by the sequence later described for data memory input.

2900 output to the 6800 MPU occurs at the end of a memory controller routine when it reports its status. The 2900 loads a status word (Table 3-17) into the 16-bit MPU port and interrupts the 6800. At the end of operations completed successfully, status 0000 (hex) is reported; otherwise, an error code is returned instead of the zero status. Another case of output occurs when the 6800 force-branches the 2900 to a routine that reports the maximum number of points interpolated by the last ATC or signal-average operation. This routine is so fast, however, no interrupt is necessary; the value is ready by the time the 6800 can read it. Also, at power-up the 2900 loads its firmware release number into the MPU port for the 6800 MPU to read and store; the 6800 uses this parameter when responding to the ID query.

TABLE 3-17

2900 STATUS WORDS

VALUE (HEX)	DESCRIPTION
0000	Operation completed normally
0001	Defect array overwritten
0002	Horizontal array overwritten
0004	ATC or upper edge array overwritten
0008	SA or lower edge array overwritten
0010	Defect array full
0020	No data or all defects during average
0080	Data memory error during self-test
0100	CPU or constant ROM error during self-test

The status word or parameter is clocked into the 2900/MPU port Status/Parameter Register (U043 and U121 on diagram 19) by CLKMPUR, gated at the bottom of diagram 21 by U303A. CLKMPUR inputs are an enabling bit in the pipeline register (ENMPUR), the CLKSTRB state machine output, and the inverted 4-megahertz clock. Because the clock is inverted, it goes low to set U303A's output high on the CPU clock active transition -- low to high. This clocks the data into the MPU port at the end of a CPU cycle, the same as for CPU internal registers.

Since the CLKSTRB state machine plays a role in this and other memory controller I/O, now is a good time to study its part. The Q outputs of U313A and U313B on diagram 21 are the CLKSTRB state variables, R and S; U313B is R and U313A is S. The CLKSTRB output is taken from R. As shown on the state diagram (Fig. 3-44), the output goes high for two cycles of CLK20 only after the smart clock enters state **d** or **i**. These are the points in the run and single-step cycles of the smart clock when HECLK goes low. This interlocking of the smart clock and CLKSTRB state machines guarantees the MPU port is clocked only at the end of a CPU cycle.

When finished setting the status word, the memory controller interrupts the MPU with PMCI, a bit in the pipeline register, and hangs itself back on a hook -- a wait loop.

Data Memory Transfers. Reading and writing to the data memory is controlled by two state machines on the Memory Controller board (A16), write flag (WFLG) and data memory control (DMC).

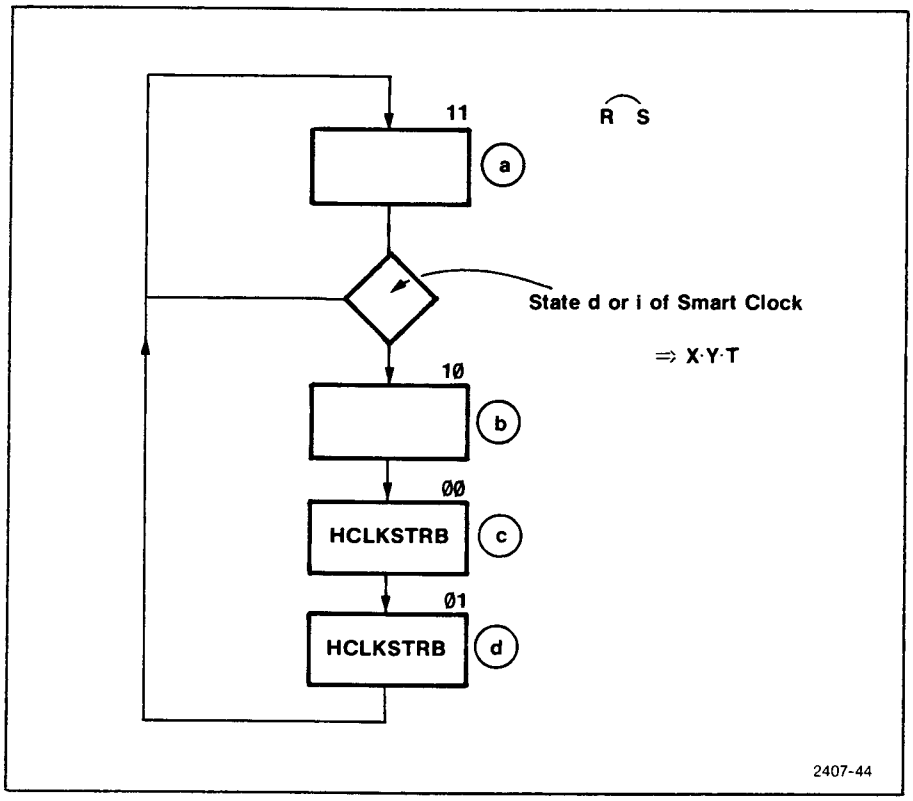


Fig. 3-44. The CLKSTRB state machine.

A read or write cycle is initiated when either the read or write enable bit is set in the pipeline register. These bits are sensed by the WRFLG state machine through U611C and U503C on diagram 21. WRFLG state machine outputs set the direction of the data transfer, high for a write, low for a read, according to the state of the pipeline register bits when ENMCYC, the memory cycle clock, goes high. (ENMCYC is set by U611D by ANDing the inverted clock with CLKSTRB.) See Fig. 3-45 for the state diagram; it is implemented with one flip-flop, U511B, and associated gates. Output WFLG is an input to the DMC state machine, while ILWE is inverted on diagram 22 to become the read control line for the memory ICs.

Other data memory control lines are generated by the DMC state machine (Fig. 3-46), whose state variables U and V are asserted by flip-flops U401A and U401B on diagram 21. (Q of U401A is asserted for U=1; Q of U401B is asserted for V=1.) The state machine waits in state **a** until either ENREAD or ENWRITE initiates a memory cycle. When either is set, the value of V changes to one on the next ENMCYC clock, and the machine

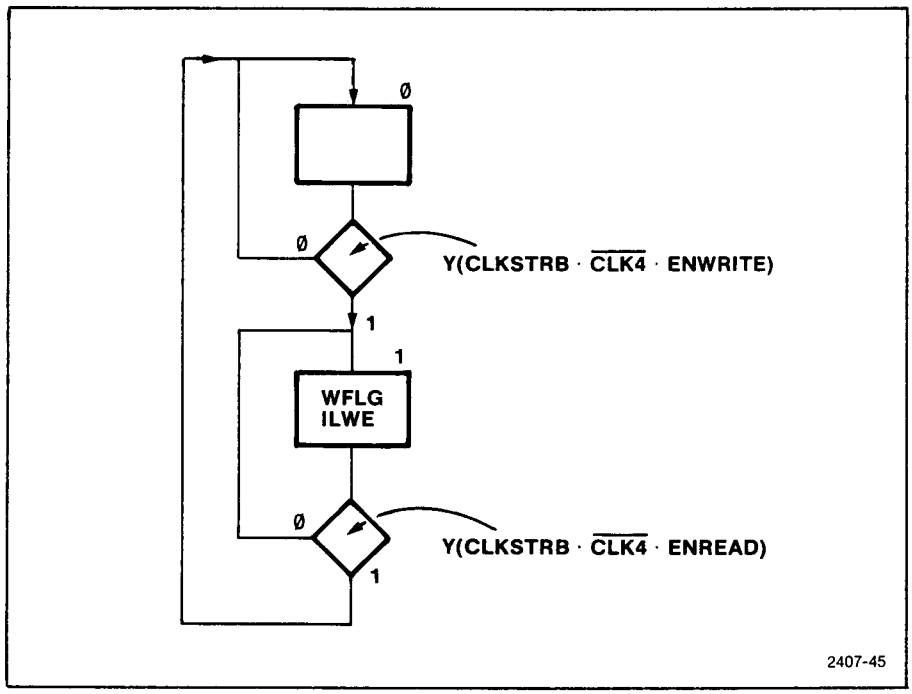


Fig. 3-45. The WRFLG state machine diagram.

moves to state **b**. In state **b**, the load data (ILLD) output presets binary counter U411 to state 1, clearing YECE8.

The DMC state machine waits to enter state **c** until the smart clock goes low, sensed as the inverted clock high at U611B. In state **c**, ILLD and IHCE (memory chip enable) are set; the input to U415C is also set if WFLG is set. This causes $\overline{\text{MDRON}}$ to be asserted in state **d** to pass data through latches U622 and U632 on diagram 22. IHCE and $\overline{\text{MDRON}}$ remain asserted until U411 counts to eight and are then cleared as the DMC machine returns to state **a**. A timing diagram of this sequence is shown in Fig. 3-47.

The data memory is addressed by a CPU write to the memory address register (MAR), U522 and U532 on diagram 22. The address is latched by CLKMAR, generated in a manner similar to CLKMPUR described earlier. The high-order address bits are decoded to be used as the memory chip select lines.

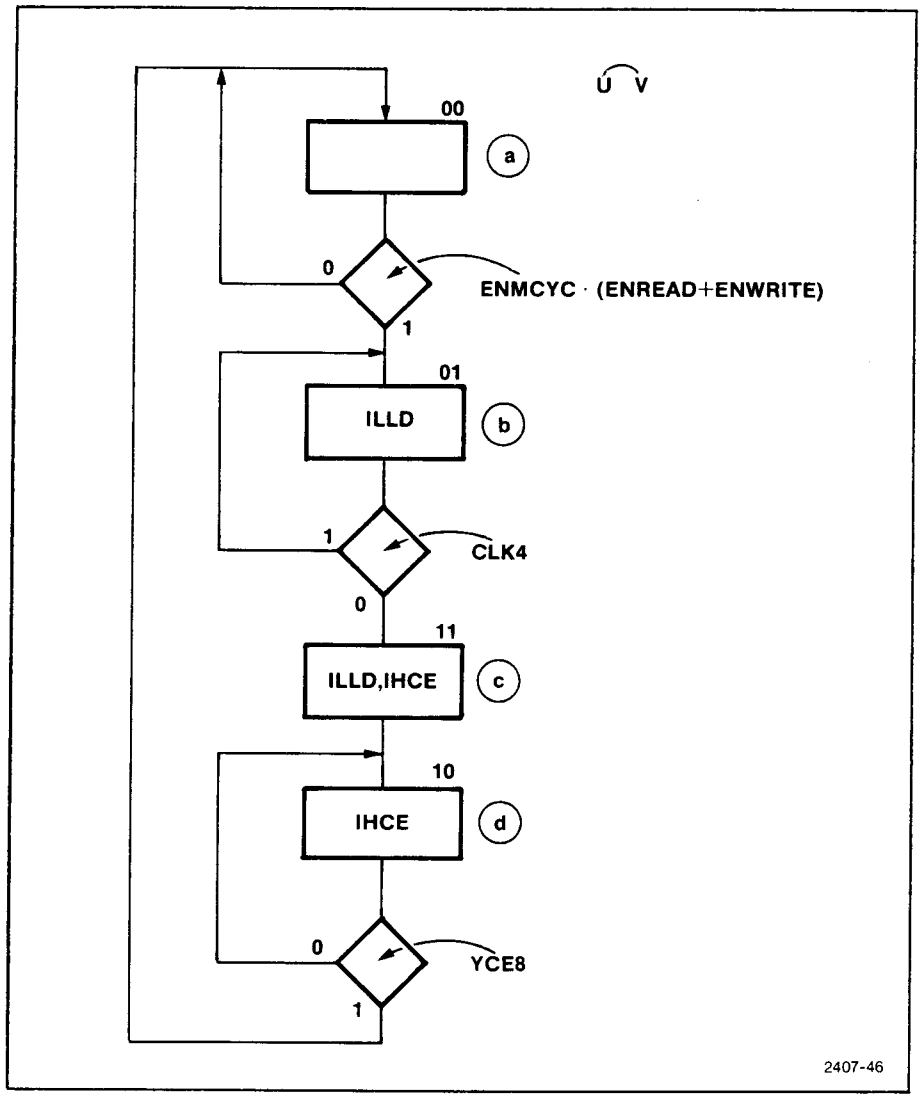


Fig. 3-46. The data memory control (DMC) state machine.

For a write cycle, U732, U724, and U722 select data either from the data buffer (TD inputs) or the CPU (CPO inputs) according to dual-purpose pipeline register bit B2M/ZEN. A high selects buffer data (buffer to memory), a low selects the CPU.

Because the lower 4K of data memory is only 10 bits wide (see Fig. 3-2 near the beginning of the circuit description), U002 at the bottom of diagram 22 is enabled on read cycles of this area of memory. The chip select line is asserted and the write enable line (ILWE) cleared so U702A enables U002, which puts all zeros on the high order bits of the data memory output.

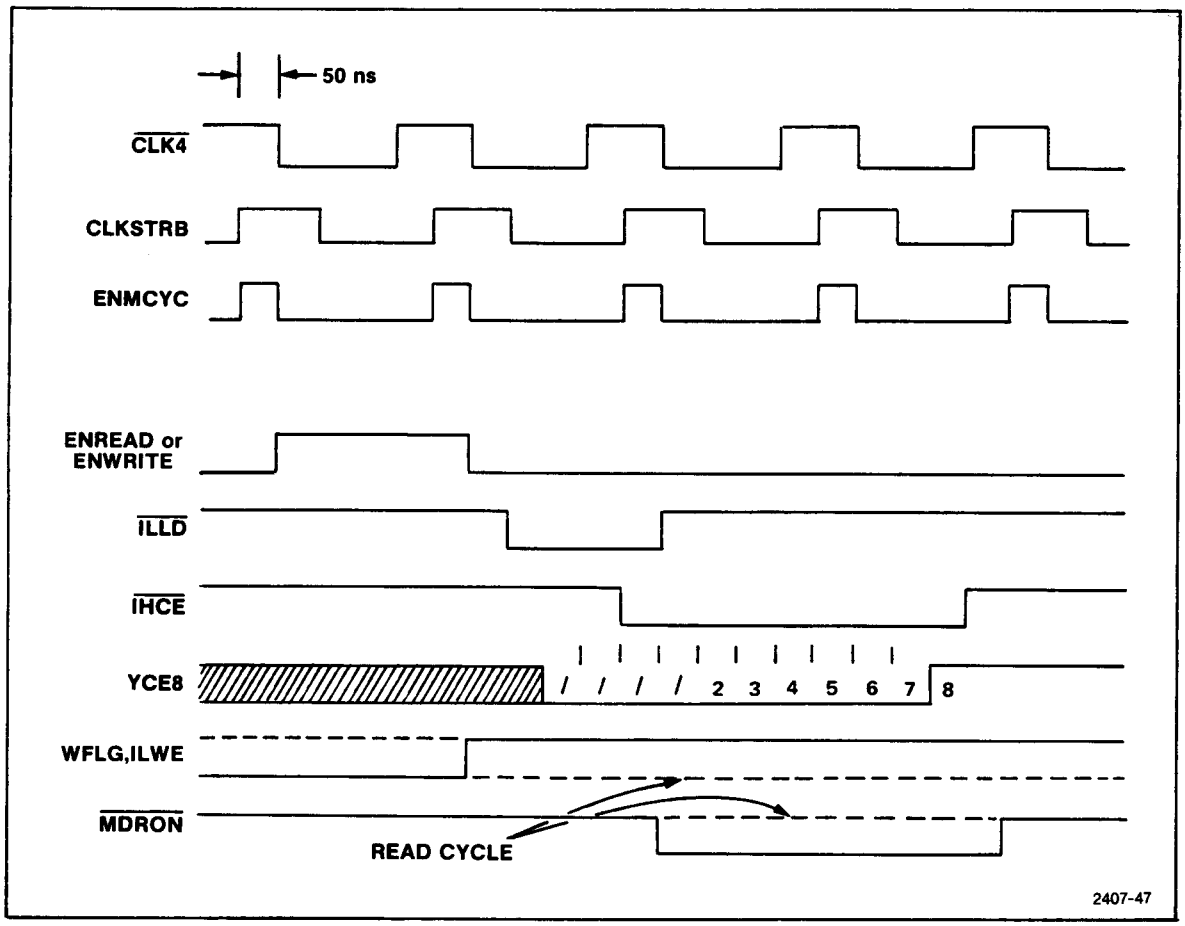


Fig. 3-47. A timing diagram of the data memory control lines.

IEEE 488 Bus Output. The memory controller sends data to the IEEE 488 Interface board (A56) over a high-speed data (HD) bus. This bus connects the 2900 output data register (U143 and U101) on diagram 19 to latches on the interface board. Separate latches are provided there for the IEEE 488 bus (U420 on diagram 28) and for the XYZ display (U430 on diagram 29). Data is handshaked by the output interface control state machine on diagram 21.

To initiate a data transfer, the 6800 MPU clears the state machine with the CLMPI bit in the 2900/MPU port Command Register (U111 on diagram 19). The 6800 sets CLMPI at the same time it sets REQ to begin the forced branch (FBR) sequence described under The Smart Clock. CLMPI clears the output interface control state machine (U301B and U301A on diagram 21). To clear the interface handshake logic, the 6800 addresses 4E00 through U522 on diagram 27, clearing U022A on diagram 28.

Data is transferred to the interface with a two-wire handshake: the output interface control state machine sets $\overline{\text{LSEND}}$ and the IEEE 488 interface sets YSENT. Because the 6800 MPU initializes the state machine and handshake logic, the two handshake lines are cleared ($\overline{\text{LSEND}}$ high and YSENT low) when the handshake of data to the IEEE 488 bus begins.

The output interface state machine (Fig. 3-48) waits in state **a** to output a byte. When the 2900 starts a state machine cycle, it sets ENODR, a bit in the pipeline register. This is ANDed with ENMCYC (both CLKSTRB and the inverted clock high) and HRDY (state machine ready) by U501C on diagram 21. The state machine moves to state **b** (HRDY still asserted) and state **c** (HRDY low) on succeeding pulses of CLK20.

The state machine waits in state **c** if YSENT is high (the last byte sent on the bus is not yet accepted). YSENT is inverted and ANDed with state variable B (Q of U301B) to set pin 3 of U301A low when YSENT goes low. State variable C is then cleared on the next clock to enter state **d** and assert $\overline{\text{LSEND}}$ through U203B. When the IEEE 488 interface responds with YSENT, it is sensed by U203A to set pin 13 of U301B low. On the next clock, the state machine returns to state **a**, unasserting $\overline{\text{LSEND}}$ and asserting HRDY.

On the interface side of the handshake, $\overline{\text{LSEND}}$ clocks the data on the HD bus into U420 on diagram 28. It also sets U022A ($\overline{\text{XMT}}$ is asserted at U122A by the 6800), which sets YSENT high through U232C. The positive transition on Q of U022A triggers the $\overline{\text{DAV}}$ delay one-shot, U130B, through gates that check for $\overline{\text{TALK}}$ and $\overline{\text{XMT}}$ set by the 6800, $\overline{\text{ATN}}$ not asserted on the IEEE 488 bus, and reset line PFCA not set.

When U130B times out (about 500 nanoseconds), it clocks U032B to assert $\overline{\text{DAV}}$ (the IEEE 488 bus $\overline{\text{DAV}}$ line) by clocking U032A through U012B. U012B checks that the hold-off after $\overline{\text{ATN}}$ is unasserted (about 1100 nanoseconds) has elapsed and no one on the bus is asserting $\overline{\text{NRFD}}$. The interface continues to assert YSENT until R-NDAC goes low to signal that data on the bus has been accepted. R-NDAC low clears the YSENT flip-flop through U520B and unasserts $\overline{\text{DAV}}$ through U620C.

To output an array from data memory, the 2900 first sends the ASCII percent character (%) and the byte count. It then reads the array one value at a time and jumps to a subroutine that sends the value one byte at a time, high byte first. The subroutine first checks that the interface is ready, then masks the low byte and loads the high byte into the output data register. This starts the output interface control state machine. Because the data is pipelined, that is, it is latched both on the Memory Control board (A16) and the IEEE 488 Interface board (A56),

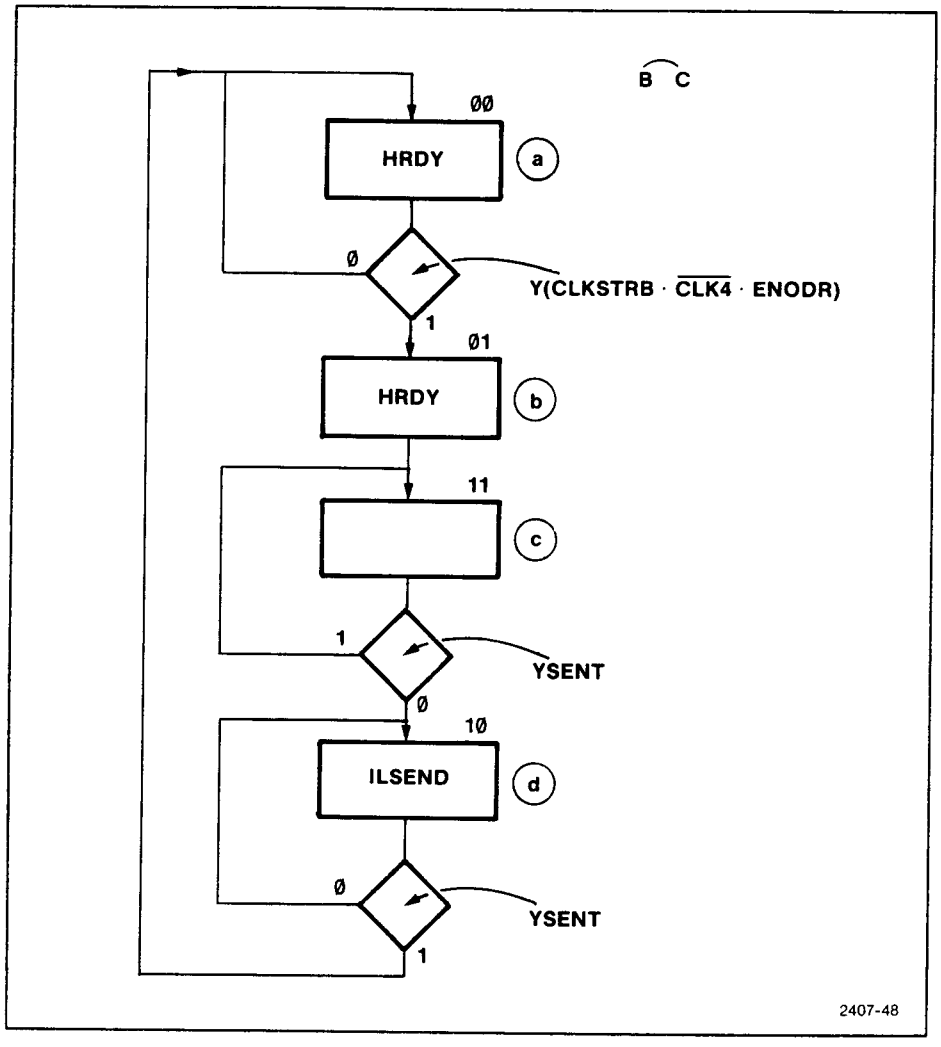


Fig. 3-48. The output interface control state machine.

the 2900 can perform other tasks while waiting for the data to be handshaked. The memory controller updates the checksum while waiting. It then loads the low byte into the output data register, restarting the output state machine. This instruction simultaneously updates the checksum by adding the byte to an internal register. The memory controller is then free to return from the subroutine without waiting for the low byte to be accepted on the IEEE 488 bus.

This sequence is shown in Fig. 3-49 with bold lower-case letters that label the smart clock and output interface state machine states. When the sequence begins, $\overline{\text{NDAC}}$ is still asserted on the bus, so the output interface state machine is still engaged in moving the last byte

sent to the output data register by the 2900. This is state **c**. WAIT is shown asserted; the smart clock is halted, waiting for the state machine to signal it is ready for another byte with HRDY high. When the data is accepted, the interface clears YSENT and the state machine asserts $\overline{\text{LSEND}}$. The interface latches the byte on the HD0-7 lines and, a few gate delays later, responds to $\overline{\text{LSEND}}$ by setting YSENT high. When the state machine senses this transition, it returns to state **a**, unasserting $\overline{\text{LSEND}}$ and asserting HRDY.

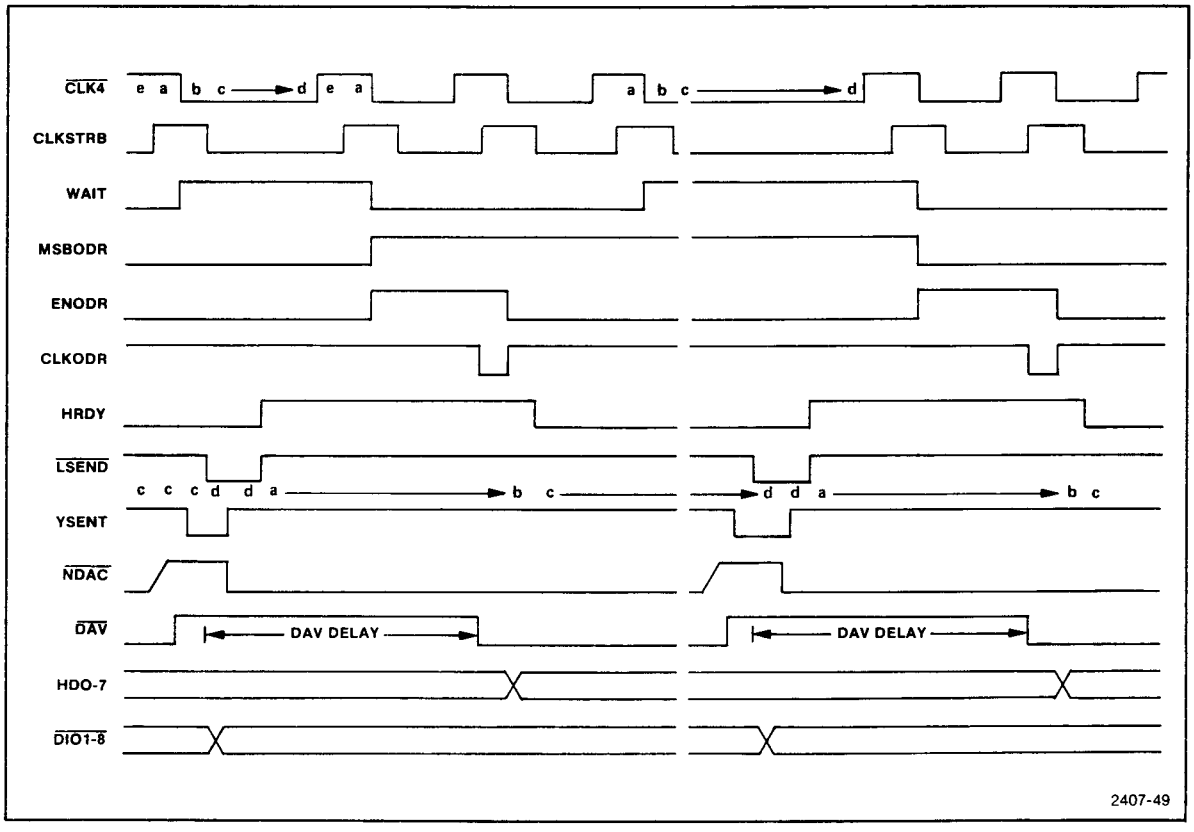


Fig. 3-49. A data transfer sequence by the output interface control state machine. Data is sent from the 2900 to the IEEE 488 bus.

The smart clock, seeing HRDY high, restarts. The next instruction transfers the value from the 2900 to the output data register (ENODR) with the low byte masked and enables output of the high byte on the HD bus (MSBODR). The following instruction updates the checksum, and the next again halts the smart clock to wait for the byte to be accepted on the IEEE 488 bus. The YSENT high-to-low transition allows the state machine to return to state **a** so the 2900 can load the value into the output data register again. This time, the low byte is enabled (MSBODR low) for transfer on the HD bus. Because the data is pipelined, the 2900

can then return from the subroutine and let the output interface state machine finish the task of sending the byte.

XYZ Display Output. This operation is initialized by the 6800 as described above for output to the IEEE 488 bus. The 6800 then sets DISPLAY on diagram 27, leaving it set for the duration of the display routine to enable the handshake of XYZ data.

The 2900 performs two kinds of output cycles to generate the XYZ display. One is an advance cycle to move the XYZ monitor beam one point to the right. The other is a data point display cycle to position the beam vertically and turn on the monitor's Z-axis. Both kinds of cycles are shown in Fig. 3-50; the end of a display cycle is shown at the left, followed by an advance cycle, then another display cycle.

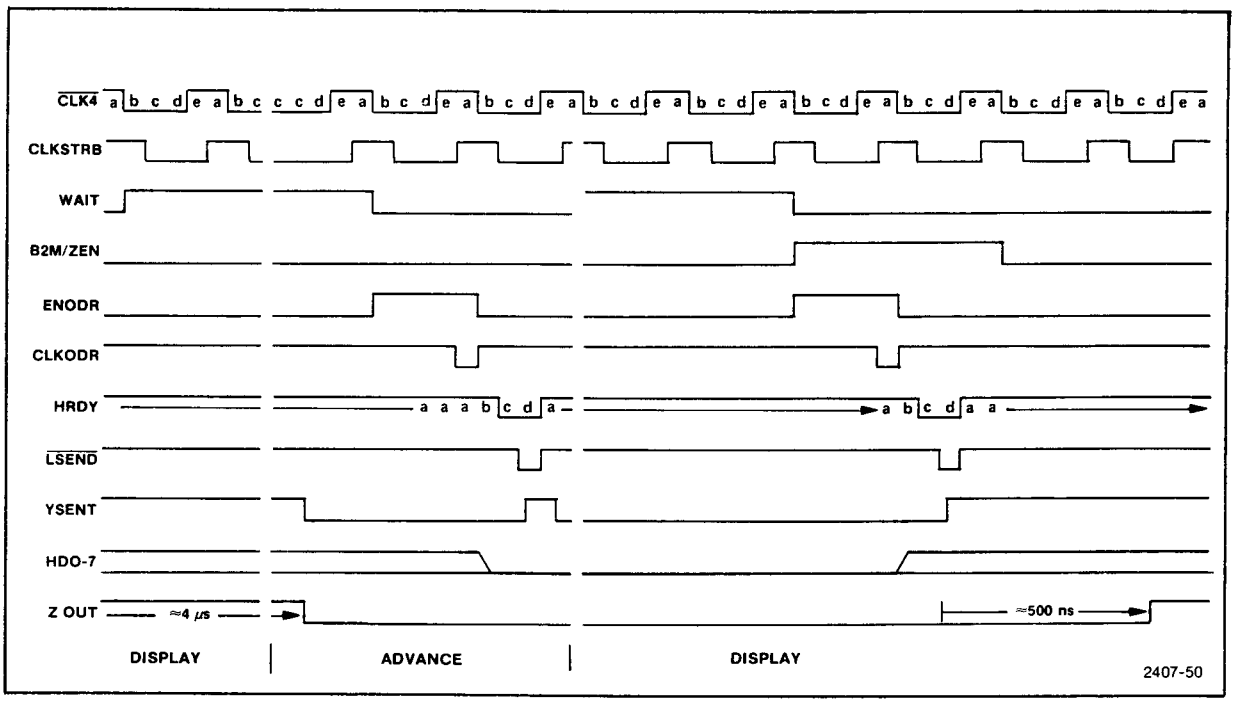


Fig. 3-50. XYZ display sequence.

At the left, the 2900 falls through a when-interface-ready instruction because HRDY is already high. WAIT remains asserted, however, in the next cycle by a when-YSENT-not-asserted instruction, and the smart clock halts. This instruction selects the inverted $\overline{\text{BYSENT}}$ input (D3) to asynchronous condition selector U603 on diagram 20 so the wait-on-condition input to the smart clock is asserted until $\overline{\text{BYSENT}}$ goes high (YSENT goes low). This happens when the Z-enable one-shot, U120B on

diagram 29, times out, unasserting $\overline{\text{DSENT}}$, which causes U232C on diagram 28 to clear YSENT. The state machine proceeds to states **b** and c after it senses ENODR asserted; the 2900 CPU puts out all zeros to be latched in the output data register by ENODR.

The state machine does not halt in state **c** because B2M/ZEN is low for an advance cycle, inhibiting U110C on diagram 29. DAC/ADV, another bit in the pipeline register, is high to cause the advance. SEND (derived from $\overline{\text{LSEND}}$) causes YSENT to be asserted briefly because it is one of the inputs to OR gate U100D. YSENT remains asserted only for the gate delays required for the state machine to sense YSENT high and return to state **a**. In state **a** it unasserts $\overline{\text{LSEND}}$; $\overline{\text{LSEND}}$ high translates to SEND low, clearing $\overline{\text{DSENT}}$ (high) and, as a result, YSENT (low) because pin 12 of U100D is no longer high. The positive transition of SEND clocks the X counter (U210A, U212B, and U212A) through U132D.

The 2900 may perform several instructions following the advance cycle before it begins a point display cycle. The smart clock normally falls through the pair of wait instructions that follow to check that the interface is ready and YSENT is not asserted. Pipeline register bits B2M/ZEN and ENODR are asserted on the following cycle to begin output of a data point; B2M/ZEN remains asserted on the following cycle, as well. This allows U120B to set the Z output high after a delay for DAC U320 settling time and the slew-rate limit of Y output driver U200; this delay is about 500 nanoseconds, set by U120A. The two one-shots are ANDed by U600B for a net Z-axis on-time of about 4 microseconds.

After initiating the output interface control state machine cycle, the 2900 is free to read the next value from memory and prepare either to advance the X counter or send the next value. Each value is shifted right so only the most significant eight bits are latched in the output data register low byte. Therefore, the 2900 need send only one byte per display point. The 2900 ordinarily performs 512 refresh operations of the XYZ display before interrupting the 6800 MPU; the 6800 then restarts the display routine, if desired.

The Data Buffer

The Schmitted video output by the Video Processor and Scan Control board (A28) contains the waveform information recovered from the scan converter. This information is converted to data on the Data Buffer board (A20) by detecting changes in the video level (the trace edges) and storing data that represent the reading beam's position on the target when the video changes; the data are then transferred to Data Memory by the 2900 memory controller. Although fast, the 2900 is not fast enough to keep up with this flow of data. So all points detected during a single vertical scan of the target are stored temporarily in half of a dual high-speed cache memory; they are read by the 2900 while data from the succeeding vertical scan is stored in the other half of cache memory.

For a brief review of how the Data Buffer relates to the rest of the 7912AD system, refer to the Digital Mode discussion in Section 1 and the block diagram description at the beginning of this section.

To do its job, the Data Buffer generates the clocks it needs and some other clocks used throughout the 7912AD, as well. To maintain fidelity of the data, the Data Buffer also synchronizes the reading gun ramps in digital mode (but not in TV mode).

Even though the 7912AD may be in digital mode, the Data Buffer remains in an idle mode until the 2900 memory controller begins a digitize operation. In idle mode, the Data Buffer continues to generate clocks and synchronize the ramps, but does not buffer data.

State machines perform the Data Buffer tasks. These state machines are implemented (in all but one case) with Emitter-Coupled Logic (ECL) to allow high clock rates. This requires ECL/TTL translators for signals coming to and leaving the Data Buffer. Refer to the pullout Data Buffer diagram to help relate the state machines and I/O buffers during the following discussion; a summary of Data Buffer signal names is located beside the diagram.

Clocks

Clock circuits on the Data Buffer circuit board fall under three headings: the 80 MHz clock; the Clock Generator state machine that supplies the data buffer clocks; and the clock divider that supplies clocks to the rest of the 7912AD.

80 MHz Clock. OR-gate U436D at the bottom of diagram 25 provides the fundamental 7912AD clock. A crystal sets the precise delay between when the output changes and when the input senses the change; this controls the clock period. A tank, L428 and C428, reinforces the oscillation. Another gate, U436A, acts as an inverting amplifier to maintain the bottom of the tank at AC ground. U420B buffers and distributes the 80 MHz clock.

Clock Generator State Machine. A pair of flip-flops near the center of diagram 25 is the state counter for the Clock Generator state machine; the flip-flop outputs are the state variables, V0 and V1. The flip-flops are wired to divide the 80 MHz clock by four. (One flip-flop with its output fed back to its input divides its clock by two; cascading two flip-flops in this manner divides the clock by four.)

About ECL 10231 D flip-flops: each $\overline{CE}$ (Clock Enable) input is ORed with the CC (Common Clock) input in each half of the IC. If one of the ORed inputs is low, a positive transition on the other clocks the flip-flop. With the common clock input tied low, each clock enable input can be used to clock the two flip-flops in each package independently.

The main state machine output drives the Y counter at a 20 MHz rate; this clock is also an input to other Data Buffer state machines. A second output (asserted only in idle mode) causes the Toggle state machine to loop at a 20 MHz rate.

The inputs to the flip-flops that assert these clocks are shown in the state diagram, Fig. 3-51. U440D supplies DEYC, which appears as a negative pulse, $\overline{EYCA}$ or $\overline{EYCB}$ (Enable Y Count A or B) at the outputs of U346B and U230A. This is the main data buffer clock; it synchronizes the state machines that control the reading ramps to the Y counter and the state machines that buffer data. The other output is a conditional output. U440B supplies this signal (called DCT1 on the state diagram) in state a when the Data Buffer is in idle mode (BD is low). It appears as a negative pulse, $\overline{CT1}$ (Cache Toggle 1), at the output of U346A.

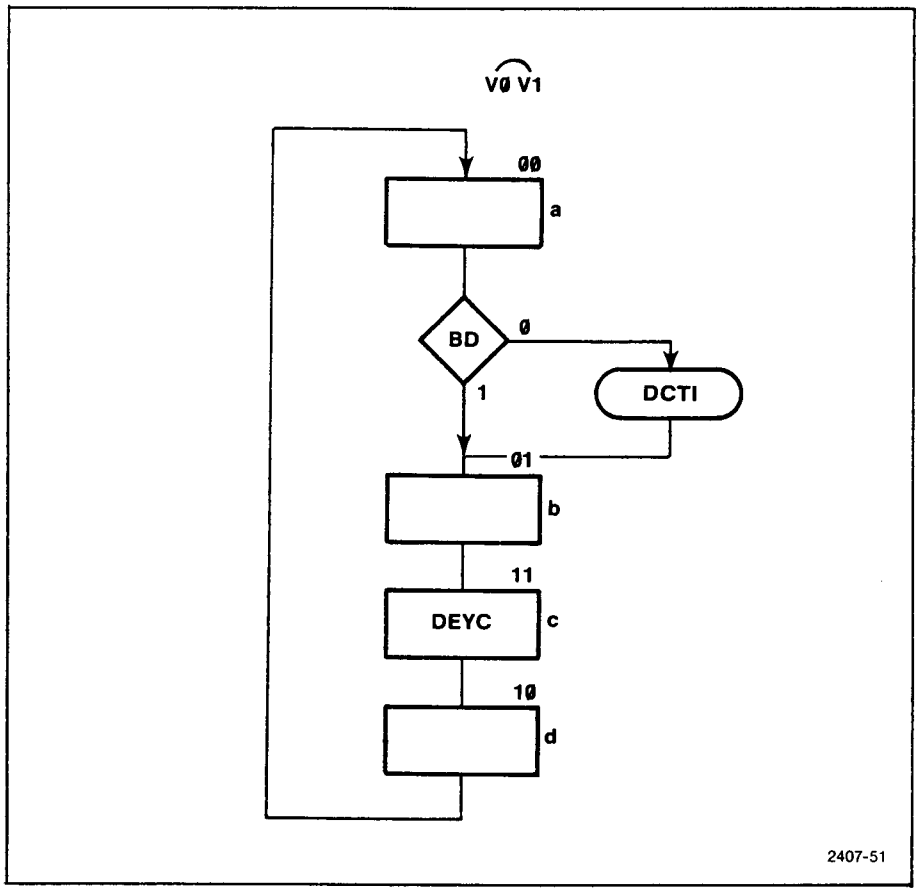


Fig. 3-51. The clock generator state machine diagram.

Clock Divider. The Clock Generator state machine variables, which run at a 20 MHz rate, are buffered and divided for use elsewhere in the 7912AD. V0 is translated to TTL levels by U430D for use by the 2900. $\overline{V1}$ is halved by U946A to drive the 6800 MPU clock. It is halved again by U946B for use on the Graticule Generator board (A24) and by the TV sync generator on the Video Processor and Scan Control board (A28).

Ramp Control

Two state machines, YVAL (Y VALue) and XVAL (X VALue), control timing of the reading ramps and allow only data from within the digital storage area of the target to be buffered. These state machines run continuously. However, in TV mode, their ramp gate pulses are ignored by the Video Processor, which supplies its own TV scan timing. And in digital mode when the Data Buffer is idle (not digitizing), data is

thrown away by the Cache Control state machines, even if it was detected within the digital storage area.

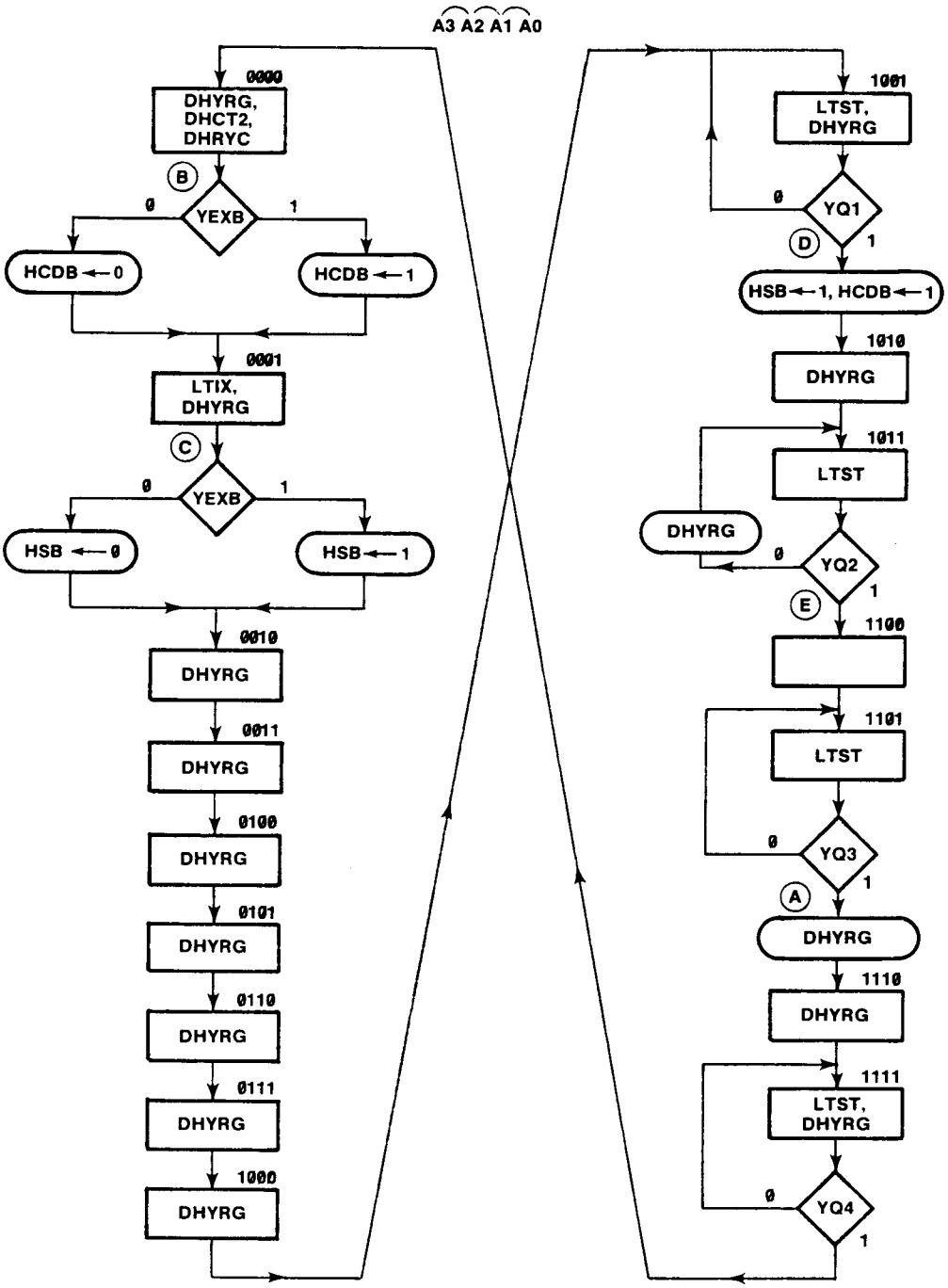
YVAL State Machine. The YVAL state machine generates the reading gun Y ramp gate ($\overline{YRG}$). When the reading beam enters the data area of the target, the machine increments the X counter, resets the Y counter, and causes the Toggle machine to reverse the data flow through the cache memories. When the reading beam leaves the data area of the target, the machine asserts SB (storage blanking).

The YVAL state machine occupies most of the right side of diagram 25 below the Clock Generator state machine. U316 is the state counter, U306 is the match ROM, U400 and U410 are qualifier comparators, and U326 is the output ROM; four D flip-flops to the right of U326 latch the state machine outputs. The Y counter is shown on diagram 24; it comprises three four-bit counters at the top of the diagram, U618, U628, and U638.

This state machine is controlled by numbers in the match ROM; the machine compares a number from this ROM with the Y count to determine when to change one or more outputs during the Y ramp. These decision points are shown in diamonds on the state diagram, Fig. 3-52, as YQ1, YQ2, etc.; the numbers in the ROM are shown in a table at the bottom of the figure. State machine outputs shown with names that begin with D are inputs to the output D flip-flops and are high in the state shown. Outputs LTST and LTIX are low in the states where they appear. LTST indicates $\overline{TST}$ (Q5 of U326) is asserted to enable the comparators, and LTIX indicates TIX is set low to get ready to increment the X counter.

YVAL state machine operation can be better understood by relating it to the Y ramp shown in Fig. 3-53. Numbers below the ramp refer to Y counter transitions at points on the ramp where state machine outputs change. For example, $\overline{YRG}$ is asserted at point A on the transition from count 567 to 568 (in normal scan mode). Four rows of numbers are shown on both the state machine diagram and the ramp diagram because the ramp can be adjusted for two options: option 4 compresses the scan to a 256 X 256 matrix; option 13 changes the TV scan from 525 lines to 625 lines.

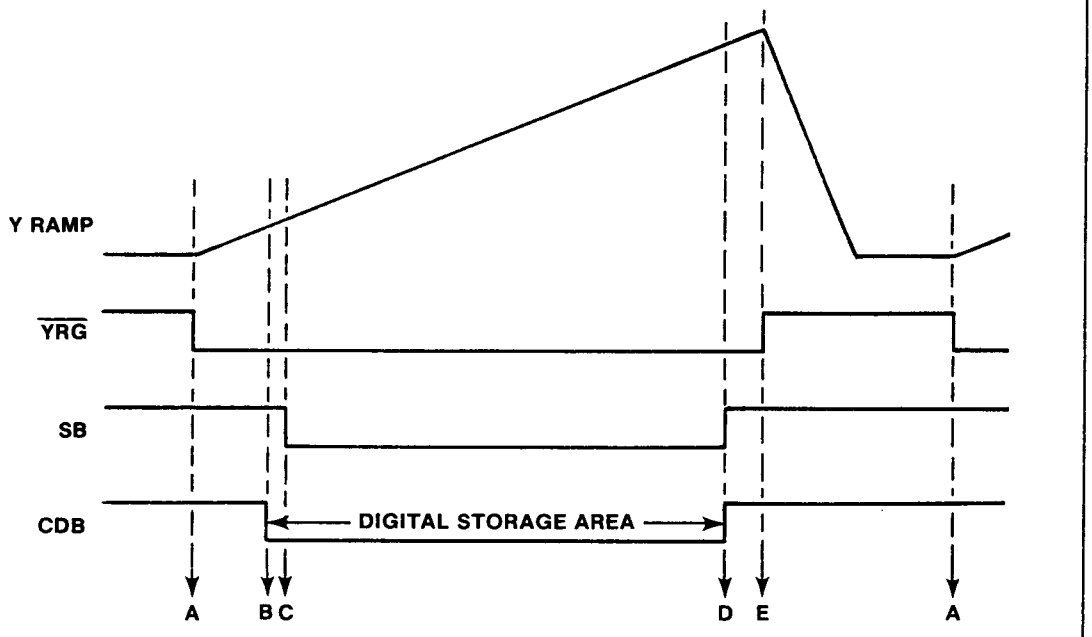
The effect of option 4 is obvious: it reduces the area scanned by one-fourth. The effect of option 13 is less obvious: it changes the area scanned by a negligible amount, but to assure that unblanking (data buffering) occurs over the same portion of the digital scan as over the TV scan, the Y counter range is increased and the ramp decision points moved accordingly.



	OPTION 13 NORM SCAN	OPTION 13 OPTION 4	525 LINES NORM SCAN	525 LINES OPTION 4
YQ1	510	254	510	254
YQ2	8	259	11	260
YQ3	60	311	55	304
YQ4	79	320	79	316

2407-52

Fig. 3-52. The YVAL state machine diagram. Timing of Y ramp events in digital mode is noted by capital letters.



EVENTS A THROUGH E OCCUR AT THESE Y COUNTER TRANSITIONS

	A	B	C	D	E
OPTION 13 NORMAL SCAN	572/573	592/593	593/0	510/511	520/521
OPTION 13 OPTION 4	311/312	321/322	322/0	254/255	259/260
525 LINES NORMAL SCAN	567/568	592/593	593/0	510/511	523/524
525 LINES OPTION 4	304/305	317/318	318/0	254/255	260/261

2407-1

Fig. 3-53. The reading gun Y ramp in digital mode and YVAL state machine outputs.

Although the tables at the bottom of the two figures are not the same, they are related by the way comparator U410 is wired; this can be understood after we learn more about the state machine. To aid in relating the two figures, events A through E on the Y ramp figure are indicated on the state machine diagram.

Let's take a trip around the state diagram loop, assuming a normal scan and a TV raster of 525 lines. In state 0, the reading beam is about to enter the data area; the output ROM is placing a high on the D input of U336B to prepare to buffer data from a new digital vertical scan. The flip-flop is clocked at the end of the negative $\overline{\text{EYCA}}$ pulse by the 80 MHz clock, causing RYC (Reset Y Counter) and $\overline{\text{CT2}}$ (Cache Toggle 2) to be asserted. ($\overline{\text{YRG}}$, asserted earlier, continues to be asserted during the vertical scan.)

If the vertical scan is occuring within the unblanked X digital scan, EXB (wired-OR of Q2 of the output ROM and XVAL state machine enable X blanking output) is low, so the CDB machine output is set low when the machine is clocked from state 0 to 1. This is event B on the Y ramp figure. The flip-flop's clock is enabled by $\overline{\text{EYCA}}$ because $\overline{\text{TST}}$ is not asserted in state 0, disabling the comparator wired-OR outputs. The resulting low from U420A is combined with the low on Q0 of the output ROM at another wired-OR at the clock enable. CDB (Composite Digital Blanking) low indicates data detected at the present reading beam position is buffered.

About ECL wired-OR nodes on the data buffer: outputs shown with external pull-down resistors are open emitter -- when active, they pull toward their positive supply (ground), and when inactive, they allow the pull-down to set the output to a logic low.

Because $\overline{\text{CT2}}$ is asserted in state 1, TIX is set low by U430C; this prepares TIX to clock the X counter when it goes high in the next state. Meanwhile, RYC asserted causes the Y counter to reset; it remains reset until the transition to state 3 because RYC is asserted when the counter is clocked to state 2.

At the end of state 1, U420A again goes low as in the previous state. This time Q0 is high, but Q1 of the output ROM is low, enabling U330A's clock. If EXB is low as explained above, SB is set low, causing the Edge state machine to detect data; this is Y ramp event C. SB low follows CDB low by one count because the data is pipelined, so it takes two clocks to get data into the machine. Both SB and CDB remain unchanged until their clock is again enabled in state 9.

The state counter continues to be clocked at 20 MHz until it reaches state 9 because each $\overline{\text{EYCA}}$ generates $\overline{\text{ECNT}}$ from U420A. States 2 through 8 are fillers to make a 16-state cycle for the 4-bit state counter. $\overline{\text{TST}}$ is again asserted in state 9 so the machine pauses, looking for the YQ1

qualifier. This is where the machine spends most of its time during a vertical scan.

In the case of the standard instrument, the YVAL machine is waiting in state 9 for a Y count of 510. Since the match ROM is only eight bits wide, its output data range is limited to 255. This limit is overcome by doubling up on Q4: it is wired to both bit 4 and bit 5 of the comparators. Thus, for YQ1, the ROM puts out 254, but the comparators see 510 and when the Y counter reaches state 510, the comparators indicate equality on pin 7 of U420A with a low. This advances the state counter when $\overline{\text{EYCA}}$ is asserted and enables the clock on both the CDB and SB flip-flops (Q0 and Q1 of the ROM are both low). EXB is asserted by Q2 in this state, causing both CDB and SB to be set high as the Y counter is clocked to 511 (positive transition of $\overline{\text{EYCA}}$). This is event D on the Y ramp figure and marks the lower boundary of the data area on the target. CDB and SB remain high until their clock is again enabled as explained above.

The next $\overline{\text{EYCA}}$ rolls the counter over from 511 to zero. Because the comparators are not enabled in state 10, $\overline{\text{EYCA}}$ also generates another $\overline{\text{ECNT}}$ and the machine moves to state 11. Here, $\overline{\text{TST}}$ is asserted and the machine waits for a Y count that matches the YQ2 qualifier (11 in the case of the standard instrument). When a match occurs, the wired-OR node at the comparator outputs goes low, so U420A enables the state counter clock input during the next $\overline{\text{EYCA}}$ pulse; the trailing edge of $\overline{\text{EYCA}}$ advances the counter to state 12.

U336A is clocked at the same time as the state counter because its clock has also been enabled by U420A. Because Q4 of the output ROM is zero in state 11, $\overline{\text{YRG}}$ is unasserted by U336A when it is clocked. This is event E on the vertical ramp -- the start of vertical retrace; it happens, according to the table at the bottom of the Y ramp figure, on Y counter transition 523/524. This is actually Y counter transition 11/12; remember the Y counter ran through 512 counts (zero to 511) and rolled over to zero, so 11 is Y count 523 as far as the ramp is concerned.

Because $\overline{\text{TST}}$ is not asserted in state 12, the comparators are not enabled, and the wired-OR node at their outputs is low; this allows the state machine counter to be clocked to state 13 where the machine tests for YQ3 ($\overline{\text{TST}}$ is asserted). When a match occurs (Y counter state 55 for the standard instrument), the low on the outputs of the comparators again allows U420A to enable the state counter. U420A also enables the U336A clock input; this time a one is clocked into U336A to assert $\overline{\text{YRG}}$. This is event A on the Y ramp figure -- the beginning of the vertical scan.

The machine falls through to state 15 in a manner similar to that for state 13. In state 15, the machine waits with $\overline{TST}$ asserted for a match between the Y count and the YQ4 qualifier (79 for the standard instrument). When a match occurs, the machine returns to state 0 to prepare to start a new vertical scan. State 0 corresonds to Y count state 80 and ramp count 592 (512 + 80 = 592); ramp events B and C follow on succeeding counts.

Different match values are addressed in U306 if the jumpers on P306 select option 4 and/or 13. (See Section 4 for instructions for setting these jumpers.) These jumpers select the most significant two bits of the ROM address to access one of the four quadrants in the ROM. The quadrant addressed by the standard jumper positions, for instance, is 10000 to 10111. The top four addresses in each quadrant hold the numbers for YQ1 through YQ4; $\overline{TST}$ is not asserted when the bottom three addresses are selected by the state counter, so they are ignored.

Y ramp events can be observed with the Tektronix 7D01 Logic Analyzer with this setup:

1) Connect the logic probes at the following points on the Data Buffer board (A20):

CH0	U336-2 (YRG)
CH1	U336-15 (RYC)
CH2	U330-2 (SB)
CH3	U330-15 (CDB)
C (external clock)	U346-14 (EYCA)

2) Set the front-panel controls for:

Threshold Voltage	Variable (set for ECL, -1.3 volts)
Sample Interval	EXT
External Clock Polarity	Down
Data Channels	0-3
Data Position	Posttrigger
Trigger Source	Word Recognizer
Word Recognizer:	
CH0	HI
CH1	LO
CH2	LO
CH3	LO
CH3-CH15	X
Word Recognizer Mode	Asynchronous
Word Recognizer Filter	Minimum

Move the cursor control to observe the transitions of the signal lines connected to the logic probes. The cursor counts at signal transitions should match the numbers in the table at the bottom of the Y ramp figure.

XVAL State Machine. The XVAL state machine generates the reading gun X ramp gate ($\overline{XRG}$). Receiving a clock from the YVAL state machine each time the target is scanned vertically, the state machine asserts $\overline{XRG}$ (except during horizontal retrace), unasserts EXB to allow buffering of data within the target's data area, and unasserts $\overline{XOB}$ (X Output Blanking) to allow readout of the data. The state machine also resets the X counter so X data value zero represents the first (left-most) vertical scan of the data area. The XVAL machine waits for the last (right-most) vertical scan of the data area to assert EXB; it then asserts $\overline{XOB}$ and then unasserts $\overline{XRG}$ for horizontal retrace.

The XVAL state machine occupies most of the lower half of diagram 26. U508 is the state counter; U510 is the match ROM; U518 and U528 are qualifier comparators; and U500 is the output ROM (U500 also provides two bits of the qualifier in parallel with U510). The X counter comprises the three four-bit counters above: U610, U620, and U630.

The state machine is controlled by qualifier numbers stored in ROM in much the same manner as the YVAL state machine. These numbers determine when to change one or more outputs during the X ramp and are

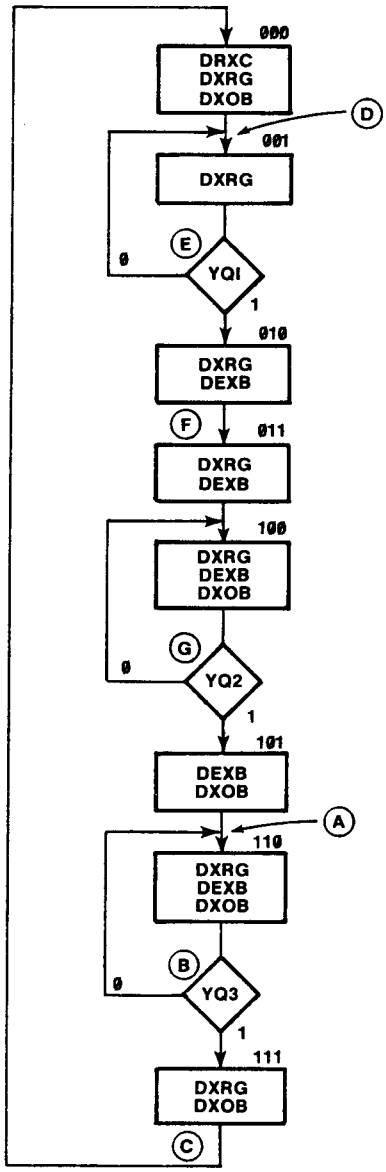
shown at the bottom of the state diagram, Fig. 3-54. State machine outputs are shown on the figure; they are inputs to the D flip-flops to the right of the output ROM. The ROM output that enables the comparators, D04, is not indicated on the state diagram, but is low during each state just above a diamond.

The X ramp is shown in Fig. 3-55 so it may be compared to the state diagram as was done with the YVAL state machine. Only two rows of numbers are shown at the bottom for the X ramp because it is affected only by option 4, which compresses the X scan from 512 to 256 points. As was the case with the YVAL diagram, X ramp events are noted on the XVAL state diagram.

In state 0, the reading beam is about to enter the unblanked digital scan area. The output ROM is placing ones on the inputs to U600A, U600B, and U600D. On the next positive transition of the clock (TIX), these flip-flops assert $\overline{\text{TRXC}}$, $\overline{\text{XRG}}$, and $\overline{\text{XOB}}$. These signals set up the X counter reset input, continue gating the X ramp, and continue locking out data readout. The transition to state 1 corresponds to event D on the X ramp figure. The X counter does not reset at this point, however; its reset is synchronized with the next positive clock transition. Because the XVAL machine unasserts EXB in state 0, the YVAL machine initiates buffering with CDB low, assuming BD is asserted (not in idle mode).

Only the ramp gate flip-flop input is high in state 1, so $\overline{\text{XOB}}$ and $\overline{\text{TRXC}}$ are unasserted (event E) after the next clock. The X counter resets anyway because $\overline{\text{TRXC}}$ was low during the setup time before the clock pulse. ($\overline{\text{TRXC}}$ is fed back through U406D so the flip-flop would be cleared regardless of the ROM output.) $\overline{\text{XOB}}$ high allows the output state machine to alert the 2900 to read the X count and data, if available. The X count (zero) matches any data stored in the previous vertical scan, which was the first (left-most) vertical scan in the data area.

In state 1, D04 of U500 is low to enable the comparators, whose outputs pull down until all pairs of inputs sense equality. While low, the comparators disable state counter U508. Meanwhile, U510 and U500 put the YQ1 qualifier on the comparator inputs (for the standard instrument the qualifier is 508). As a result, the machine waits in state 1 with $\overline{\text{XRG}}$ asserted until the reading beam approaches the right boundary of the digital area on the target (511 for the standard instrument). This wait is where the machine spends most of its time.

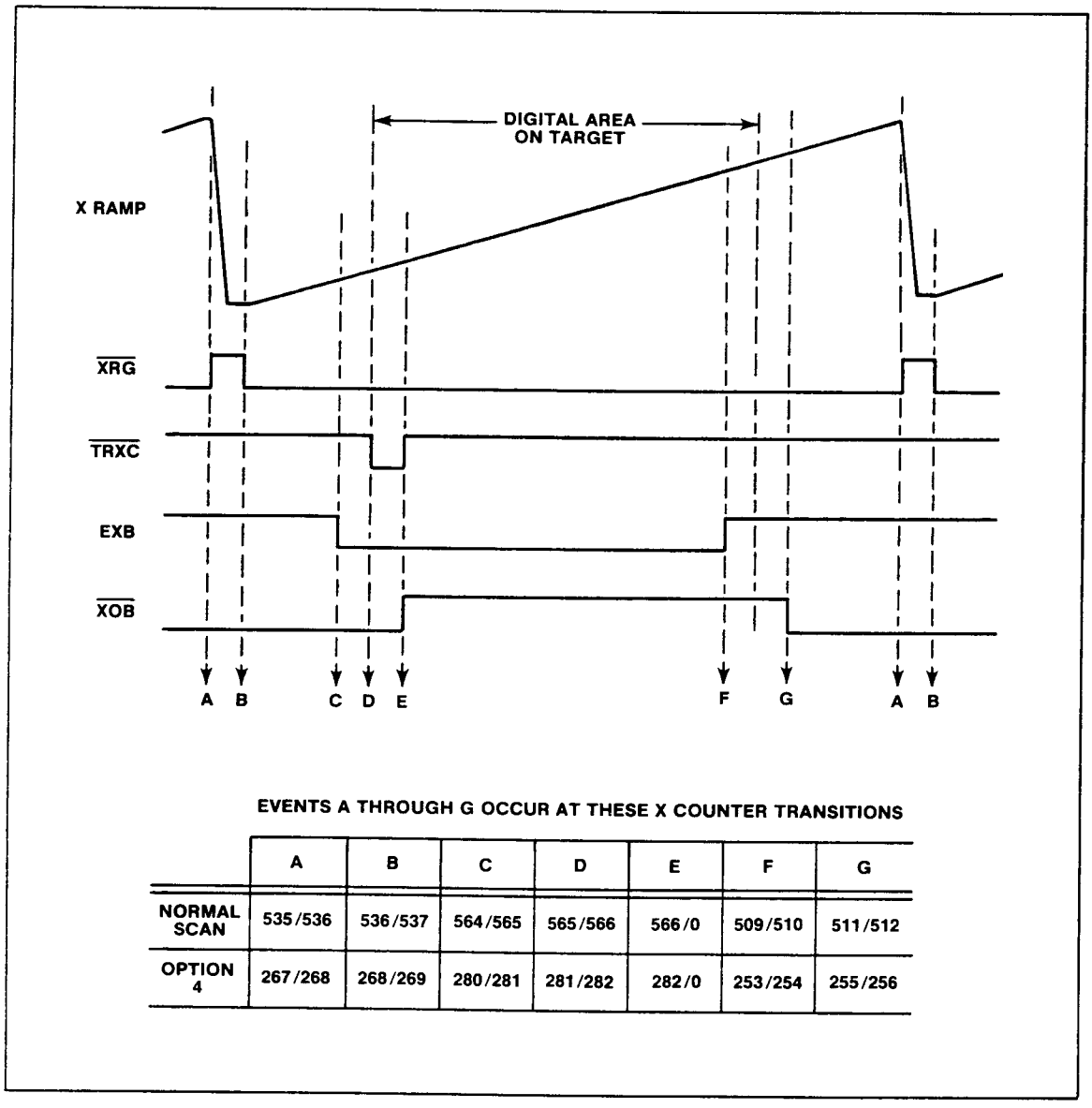


(B), (E), (G) OCCUR ONLY FIRST TIME THROUGH THE LOOP

	NORMAL SCAN	OPTION 4
YQ1	508	252
YQ2	534	266
YQ3	563	279

2407-2

Fig. 3-54. The XVAL state machine. Timing of X ramp events in digital mode is noted by capital letters.



EVENTS A THROUGH G OCCUR AT THESE X COUNTER TRANSITIONS

	A	B	C	D	E	F	G
NORMAL SCAN	535/536	536/537	564/565	565/566	566/0	509/510	511/512
OPTION 4	267/268	268/269	280/281	281/282	282/0	253/254	255/256

Fig. 3-55. The reading gun X ramp in digital mode and XVAL state machine outputs.

When a match occurs, $\overline{U508}$ advances to state 2, and the output ROM asserts the input for EXB (XRG remains asserted). On the next clock EXB is latched (event F on the ramp figure), and the state machine advances to state 3. This marks the end of the digital scan; EXB is an input to the YVAL machine that causes SB to be asserted.

The following clock pulse advances the machine to state 4 where the $\overline{XOB}$ input is asserted as well. $\overline{XOB}$ prevents output of data detected outside the digital area of the target; it is latched on the following clock pulse (event G), but D04 of the output ROM is again asserted, so the machine waits for the YQ2 qualifier (534 for the standard instrument). When a match is found, the comparators again release the counter enable inputs and the counter advances to state 5. In state 5, the $\overline{XRG}$ input is no longer asserted. This change is latched on the next clock pulse, but $\overline{XRG}$ remains high for one clock cycle only (one vertical scan).

Since the comparators are again enabled in state 6, the machine waits for the YQ3 qualifier (563 for the standard instrument). With the $\overline{XRG}$ input again asserted in state 6, the output is asserted (event B) after the first clock pulse following entry into state 6 and remains asserted while the machine waits. When the comparators indicate a match, they enable the state counter to advance to seven. Here the EXB input is unasserted so when the state counter rolls over from seven to zero, EXB is unasserted (event C), and the XVAL machine gets ready for the reading beam to enter the digital area of the target. When EXB is next sampled (at event D on the ramp figure) by the YVAL machine, buffering begins.

Data Buffering

Data buffering comprises detecting waveform data contained in the Schmitted video signal, storing the data in temporary (cache) RAM, and reading the data out to the 2900 memory controller system. The data are detected by the Edge state machine; the data are stored by the Cache Control state machines, which are selected alternately by the Toggle state machine; and the data are handshaked by the Output state machine.

Data buffering occurs only by 2900 memory controller command; to buffer data, the 2900 sets the DIG bit in the pipeline register. The resulting low on the set input of U240A (diagram 25) allows the next sweep gate to clear the flip-flop, placing a high on the input of U134B. BD (Buffer Data) is asserted during the next on-time (low) of the data buffer clock, $\overline{EYCB}$. The input of U134B can also be set high by clearing U240A when DIG is set if the 6800 MPU first sets NSG in the Command Register. When the 2900 finishes acquiring a waveform, it sets DIG low, resetting U134B.

Since the XVAL state machine may be at any point on the target when DIG is set, the 2900 must keep track of the vertical scans to know when the target has been fully scanned. Thus, the data may be stored starting at any point on the target; storage continues to the right boundary of the data area on the target, then continues again after horizontal retrace until the reading beam returns to where it started. Because the 2900 reads the corresponding X value for each group of Y values obtained from a vertical scan, it can reorder the data for left-to-right readout.

Edge State Machine. The Edge state machine waits until $\overline{BD}$ is asserted and the YVAL state machine indicates the reading beam is in the data area of the target. The Edge machine then detects each edge of a trace, that is, each time SVID changes state. For each change, the Edge machine causes the current Y count to be stored in cache memory.

The state diagram is shown in Fig. 3-56; state variable V4 is asserted by U038A on diagram 25. This flip-flop is cleared until $\overline{BD}$ is asserted to initiate data buffering and remains cleared as long as SB is asserted. When $\overline{BD}$ is asserted and SB is not asserted, the machine is ready to test the state of the Schmitted video line. Note that the Schmitted video signal is double-buffered, so the Edge state machine tests the video state latched during the previous cycle of $\overline{EYCB}$. This explains the one-count offset between CDB and SB positive transitions on the Y ramp figure.

In state 0, when the Edge machine senses video high and SB low, it asserts the D input of U134A, which asserts WIC (Write Input Cache). The D input is a wired-OR node; a high on the output of any of the three NOR gates pulls the node high. In state 0, this high is supplied by U048C whose output goes high as soon as it senses one of two conditions: 1) Schmitted video is already high and storage blanking has changed from asserted to unasserted; or 2) storage blanking is unasserted and Schmitted video changes from low to high.

Let's take case 1 first. Schmitted video may already be high when SB is unasserted (the reading beam is within the edges of a trace on the target when the beam enters the digital area of the target). Then pin 13 of U048C is low, and pin 12 must be low because SB high placed a low on the input of U038A during the last clock cycle. When SB goes low, all three inputs to U048C are low, and its output goes high, resulting in $\overline{WIC}$ asserted for the following clock cycle. On the following clock cycle, both inputs to U144A being low, U038A goes high and U048C no longer causes the input to the $\overline{WIC}$ flip-flop to be high.

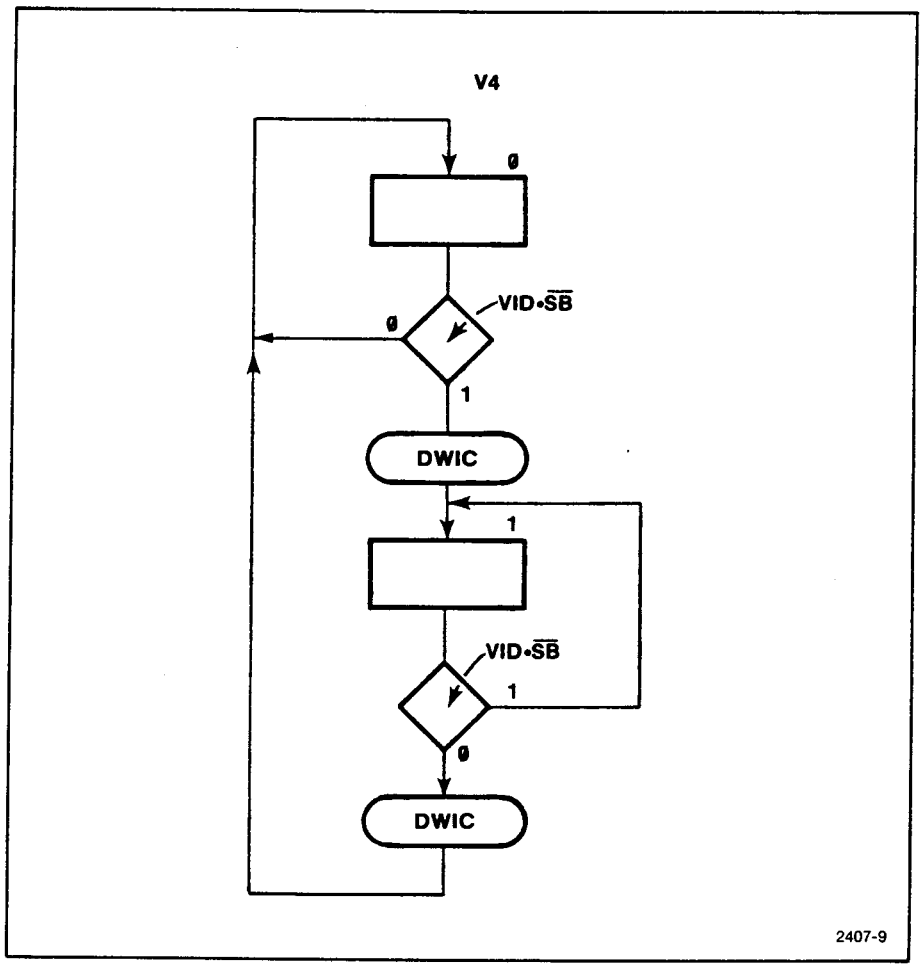


Fig. 3-56. The edge state machine diagram.

Now case 2. If SB is unasserted and the video is low, U038B is cleared and only the high it places on pin 13 of U048C is keeping the NOR gate output low. When U038B senses video high, it is set, putting a low on pin 13 of U048C and the NOR gate output goes high. On the following clock, the two lows at the U144A inputs cause U038A to be set, and U048C's output again goes low.

Whether through the logic of case 1 or case 2, conditional output $\overline{\text{WIC}}$ is asserted for one cycle of the 80 MHz clock, and the Edge machine moves to state 1. In state 1, it again tests video and storage blanking; a change in either causes another $\overline{\text{WIC}}$ and a return to state 0. Again, either of two cases is possible.

To avoid confusion, let's call one of these case 3. If SB is low and Schmitted video changes from high to low (the reading beam exits a trace), both U144D inputs are low, and it supplies the high on the input to the $\overline{\text{WIC}}$ flip-flop. (Remember pin 13 of U144D would be low beause U038A is set in state 1.)

Now for the last possibility, case 4. If Schmitted video is high, but the reading beam reaches the bottom of the digital area on the target, pin 6 of U144B goes low; pin 7 is already set low by U038A in state 1, hence U144B asserts the high on the $\overline{WIC}$ flip-flop input. Either case results in a high on one of the U144A inputs, clearing U038A and returning the edge machine to state 0.

The logic of this state machine causes it to assert $\overline{WIC}$ only for changes in the state of Schmitted video or when storage blanking changes while the reading beam is inside the trace. Thus, data are detected in pairs; what goes up (Schmitted video) must come down.

Cache Control State Machines. The Cache Control state machines control writing and reading of the cache memory. Each machine controls one-half of the memory; while one is writing, the other is reading, so each machine has an input and an output mode.

The Cache 1 Control state machine is shown in Fig. 3-57. U028A and U028B on diagram 25 implement state variables V2 and V3, respectively. In state **a**, the machine is waiting for either $\overline{WIC}$ or $\overline{ROC}$, depending on the state of I1 (a toggle state machine output). If I1 is high, cache 1 memory is selected for input, and the Cache 1 Control machine is waiting for $\overline{WIC}$ to be asserted.

U124B places a high on the D input of U028B when $\overline{WIC}$ is asserted to move the machine to state **b** on the next clock. Meanwhile, $\overline{WIC}$ and I1 asserted in state **a** cause U124A to set U210A on the next clock; U210A then asserts $\overline{WE1}$ (Write Enable 1) to load the current Y count into cache memory.

Because of the way the state variables are connected to drive the wired-OR at the input to U028B, the machine counts 0, 1, 3, 2, etc. Because V3 is asserted in both states **b** and **c**, neither state machine output is asserted. In state **d**, however, V3 and V2 both place lows on the inputs of U114C, which asserts ICA1 (Increment Cache 1 Address). The machine returns to state **a** on the next clock and repeats the cycle, testing $\overline{I1}$ for input or output.

When $\overline{I1}$ is not asserted, the Cache 1 Control state machine enters the output mode. In this mode, it is driven by ROC from the output state machine. Only ICA1 is asserted during a state machine cycle in the output mode; $\overline{I1}$ high keeps $\overline{WE1}$ unasserted. ROC asserted equals $\overline{ROC}$ low at pin 14 of U124C; pin 12 (V3) and pin 13 (I1) are both low in state **a** during output mode, so U124C provides the high to set U028B. The state machine then clocks through its states, asserting $\overline{ICA1}$ in state **d** as in input mode.

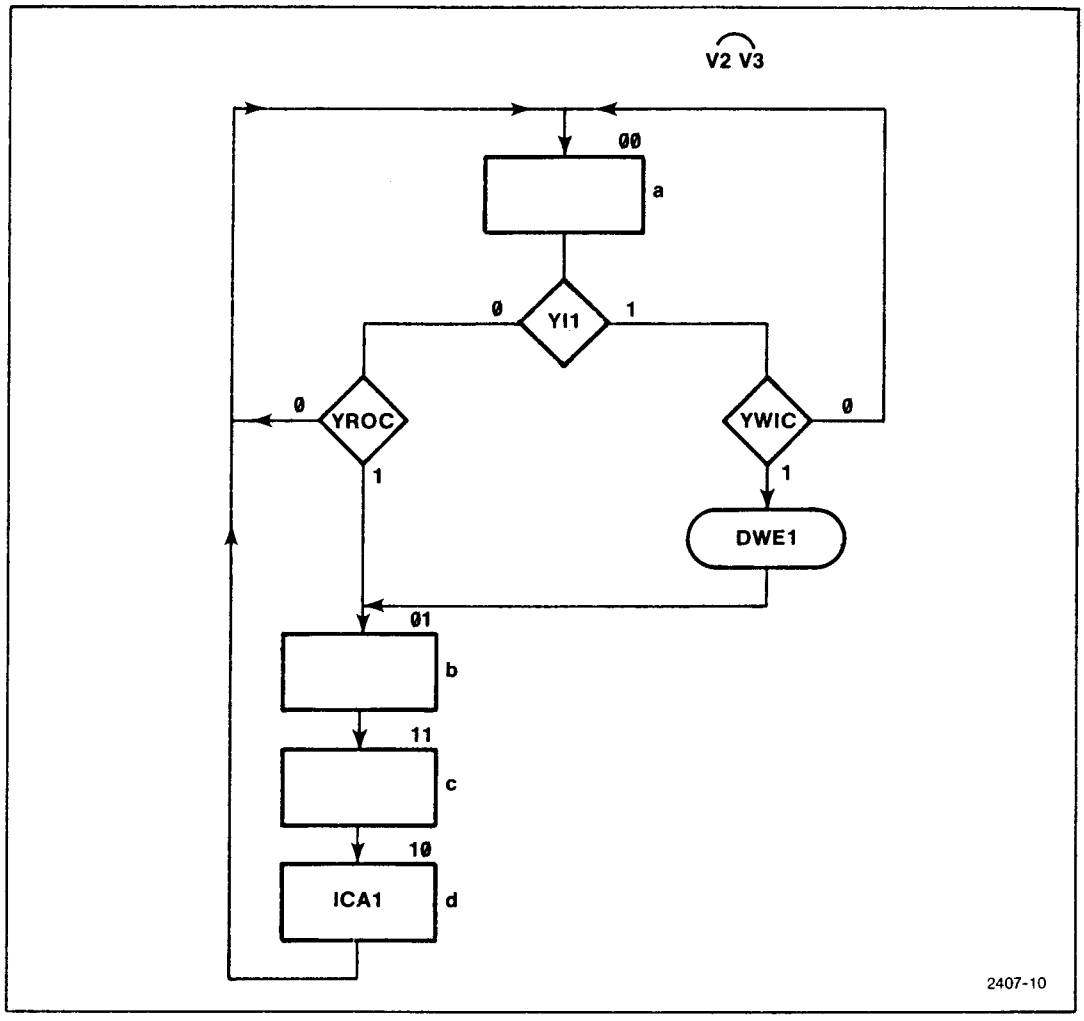


Fig. 3-57. The cahe 1 control state machine diagram.

Cache 2 control is a replica of the Cache 1 Control state machine and is shown next to the cache 1 machine on diagram 25. The sense of input I1 is reversed so the cache 2 machine output and input modes are reversed, compared to the cache 1 machine. The cache 2 control outputs are also changed so they direct traffic in the cache 2 half of buffer memory.

Toggle State Machine. The Toggle state machine sets the input/output mode of the two cache control state machines with the I1 (Input 1) signal. Two other outputs synchronize buffer memory I/O: $\overline{\text{LCA}}$ (Latch Cache Address) and RCA (Reset Cache Address).

The Toggle machine state diagram is shown in Fig. 3-58. Variables V5 and V6 are the states of flip-flops U246B and U246A, respectively. The machine waits in state a until a cache toggle input is received. $\overline{\text{CT1}}$ is a 20 MHz pulse asserted in idle mode by the Clock Generator state machine

to reset the cache memories. $\overline{CT2}$ is asserted by the YVAL state machine when the reading beam enters the digital area on the target. Either toggle signal causes a high at the wired-OR node at the input to U246A; when clocked into the flip-flop, the state machine moves to state **b**.

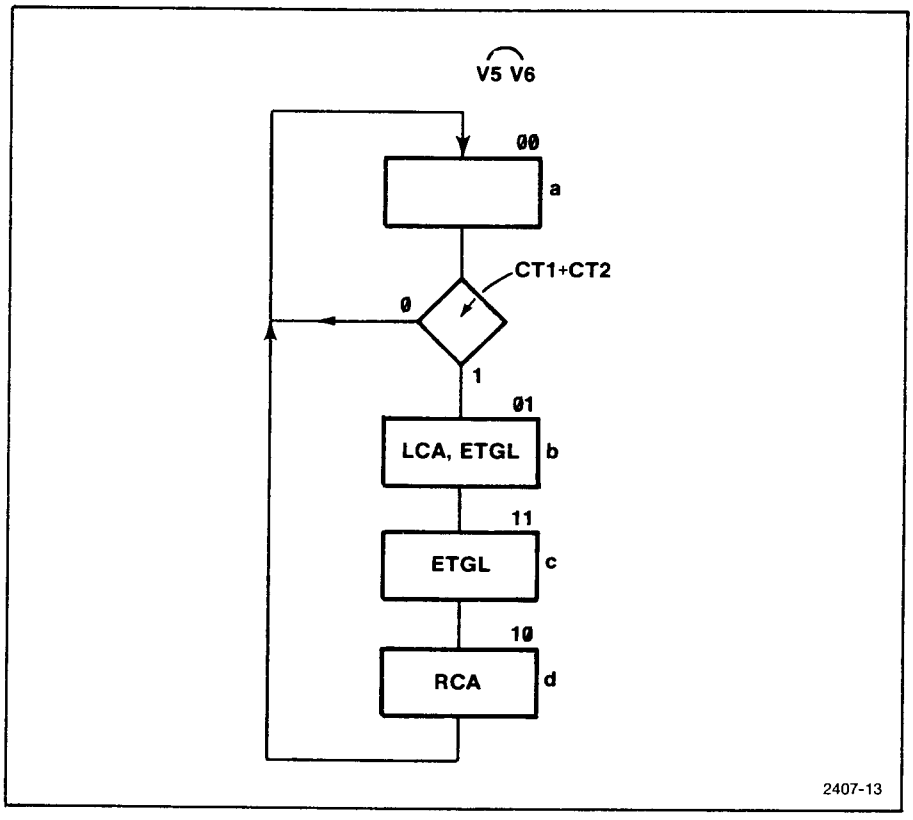


Fig. 3-58. The toggle machine state diagram.

In state **b**, the state variables combine to assert $\overline{LCA}$ and change the clock enable input of U240B from low to high. The latter state machine output (called ETGL -- Enable ToGgLe -- on the state diagram) causes U240B to change state, reversing the cache control state machines. ETGL remains asserted in the next state, but goes low in state **d** to allow setup on the clock enable input for the next toggle machine cycle.

In state **d**, the state variables combine to place lows on both inputs to U340C, which asserts RCA. With state variable V6 equal to zero, a low is placed on the input to the V5 flip-flop (U246B), which is cleared on the next clock. This returns the machine to state **a**.

By asserting $\overline{LCA}$ and RCA just before buffering of data from a new vertical scan begins, the Toggle machine prepares for readout of the previous scan and storage of the new scan. $\overline{LCA}$ saves the number of Y values stored during the vertical scan, and RCA resets the cache address counter for the next scan.

Buffer Memory. The buffer memory is shown on diagram 24, cache 1 in the top half of the diagram and cache 2 in the bottom half. The memory is addressed by cache address counters U608 and U740, both of which are controlled by the cache control state machines. Each cache counter is augmented by a flip-flop to make a five-bit counter. When reset, the flip-flop supplies the counter clock-enable until the counter overflows; then the counter's terminal-count output goes low to change the flip-flop state and then high when the counter rolls over to zero, enabling the counter clock input. When the counter again overflows, the terminal-count output changes, disabling the counter so it does not exceed the buffer address range (31).

Each cache memory is structured so two 16 X 4 memory chips and the 128 X 1 chip are addressed for each word. The MSB of the address (supplied by the flip-flop associated with the counter) selects two of the four 16 X 4 chips and bit 4 of the 128 X 1 chip address.

Output State Machine. The Output State Machine waits in state 0 until X data is available. It then outputs an X value, followed by vertical values, if any, that correspond to that X value. When finished, the machine waits for another X value to repeat the cycle.

The state diagram is shown in Fig. 3-59. The state counter is U226 on diagram 25; U310 is the state ROM; flip-flops to the right of the ROM latch state machine outputs; and selector U216 and associated logic control jumps within the state machine loop.

The state counter master-reset input holds the macnine in state 0 until a digitize operation begins (BD is asserted). The machine then tests for RYC; RYC is asserted by the YVAL machine to reset the Y counter just before the reading beam enters the digital area during a vertical scan. In state 0, Q3 of the counter is zero and Q0 through Q2 of the state ROM are also zero. Q5 of the state ROM is asserted, but Q6 and Q7 are not, so RYC is selected as the U216 output. As a result, each clock ($\overline{EYCB}$) causes the parallel-enable input of the state counter to be asserted, loading zeros into the counter and holding the counter in state zero. When RYC is asserted, $\overline{EJMP}$ stays high and the counter advances to state 1.

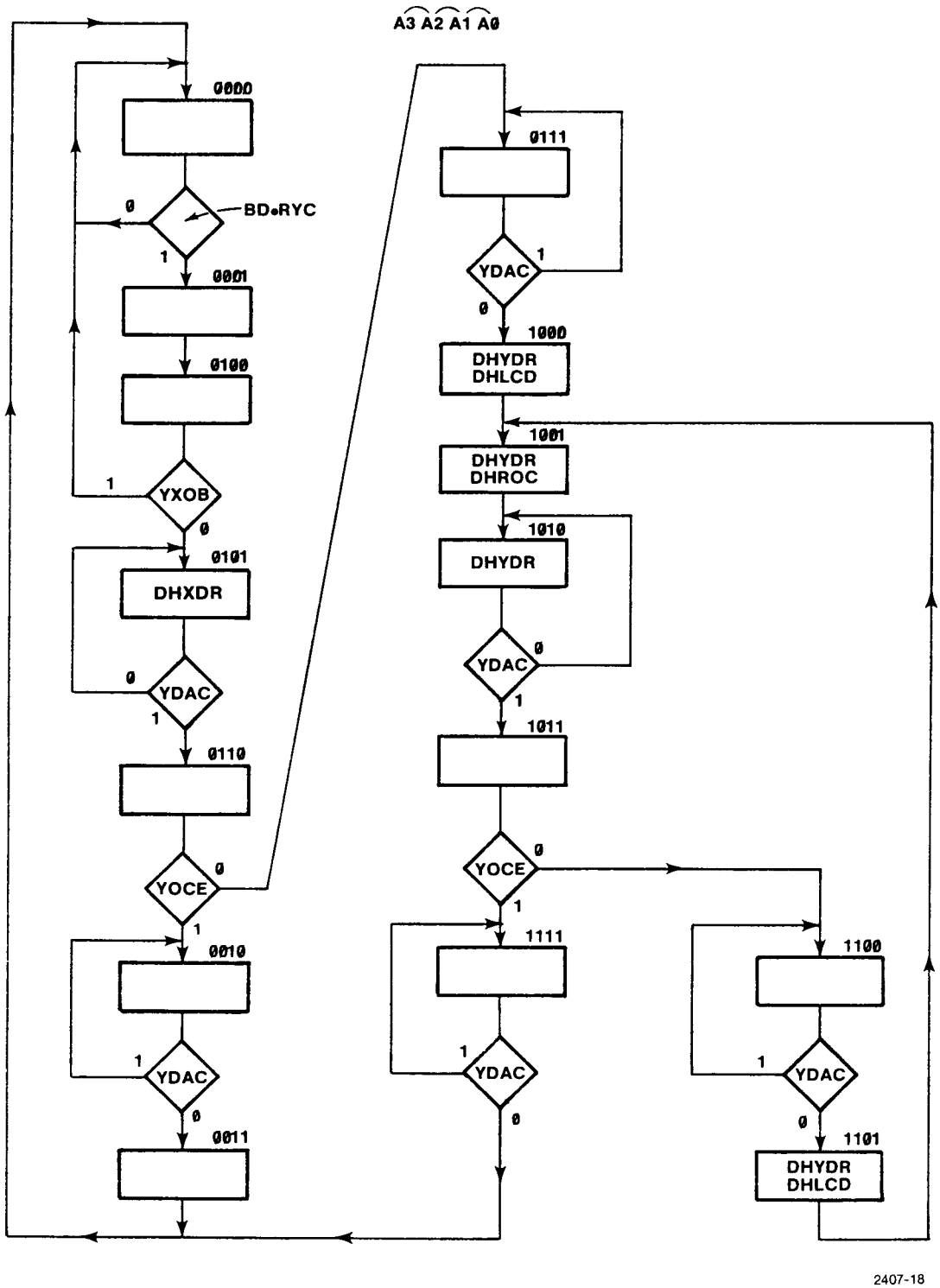


Fig. 3-59. The output state machine diagram.

In state 1, $\overline{EJMP}$ is again asserted by selecting the X0 input of U216; this parallel-loads a four into the counter to advance to state 4. In state 4, $\overline{XOB}$ is tested to determine if data in the cache was read from the digital area of the target. If not, $\overline{EJMP}$ is again generated, and the machine loops back to state 0.

In state 5, Q3 of the state ROM is asserted and latched on the next clock by U220B as $\overline{DR}$. Combined with $\overline{XD}$ (X Data), which is Q3 of the state counter, it is asserted as XDR. This is an input to the 2900 smart clock, which was waiting for X data ready, causing the clock to restart so the 2900 can store the X value. Meanwhile, XD sets TYD (Y Data) low through U236D, selecting the X counter inputs of the output selectors (on diagram 26) to transmit to data memory.

The state ROM then selects the state of the DAC/ADV (Data ACcepted or ADVance) line to control $\overline{EJMP}$ and waits for the 2900 to handshake the X value. After the 2900 stores the value, it asserts DAC/ADV to indicate it was accepted, allowing the Output state machine to advance. In state 6, the $\overline{OCE}$ (Output Cache Empty) input is selected to control $\overline{EJMP}$; if $\overline{OCE}$ is asserted, the state machine waits for DAC/ADV to be unasserted and then returns to state 0. If $\overline{OCE}$ is unasserted, the machine proceeds to read out Y data.

Let's review the Toggle machine before tackling how and why $\overline{OCE}$ is asserted or unasserted. After the Toggle machine switches the data flow through the cache memory, it asserts $\overline{LCA}$ to latch the state of the cache address counters and asserts RCA to reset both counters. So when the Output machine begins to read out Y data the counter is at zero, and the latch holds the number of Y values to be read. If no Y values were stored, the comparator (U700 on diagram 24 for cache 1 and U846 for cache 2) output goes low. If Y values were stored, the comparator output stays high until all inputs indicate equality.

Let's take cache 2 for an example to learn how $\overline{OCE}$ is asserted. $\overline{ROC}$ (Read Output Cache) is asserted by the Output machine after it reads each Y value. The Cache Control state machine, in turn, asserts ICA2 to step the cache counter ahead. If its state then matches the number in the latch, the comparator unasserts ALTL2 (Address Less Than Latch 2). This is sensed by U648C (lower-right of diagram 25); ORed with the cache selector line, which is asserted, ALTL2 low asserts $\overline{OCE}$ through U648A. The other OR gate is disabled by the state of the cache select line; it is active when cache 1 is in output mode (I1 is low).

Note that the LSB of the cache address latch is not tied to the comparator LSB input. This guarantees that the Output state machine only reads an even number of Y values for any vertical scan. The Edge state machine is designed to detect data only in pairs, so an odd number of vertical data should never be stored. If it should happen, however, that an odd number, say five, are stored, then the comparator would indicate equality on four, and the fifth would be discarded. (This also limits the number of Y data output for any vertical scan to 30, rather than 31.)

To read out Y data, the Output state machine first checks in state 7 that DAC/ADV has been reset by the 2900. It then advances to state 8 where the $\overline{DR}$ input is again asserted, as well as the $\overline{LCD}$ (Load Cache Data) input. $\overline{DR}$ combines with $\overline{XD}$ unasserted at U008B to assert YDR, requesting that the 2900 read the Y value. $\overline{LCD}$ latches the buffered data selected by the state of I1 at U910 and U920 on diagram 24. $\overline{XD}$ unasserted gates this data through the selectors on diagram 26 to be read by the 2900.

In state 9, the Q output of the LCD flip-flop is applied to U220A, causing $\overline{ROC}$ to be asserted; $\overline{ROC}$ prompts the cache control machine presently in output mode to increment the cache address counter. The machine then waits for the data to be accepted in state 10. After the value is accepted by the 2900, the machine checks to see if it has output the last Y value. If so, it waits for the 2900 to unassert the DAC/ADV line and then returns to state 0. If more values remain, the machine goes from state 9 to state 12 where it waits for DAC/ADV to be unasserted before repeating the Y output cycle.

During the digitize operation, the 2900 has been keeping track of the number of vertical channels read by counting the number of X values read. When the reading beam has wrapped arond, that is, has read from where it started to the right boundary of the target, then retraced and read from the left boundary to where it started, the 2900 ends the digitize operation by unasserting DIG. The 2900 then merges the data so that on readout it begins with the top, left-most data point and proceeds to the right. It throws away duplicate points it may have detected both at the beginning of the digitize and at the end where it rescans the vertical channel it first digitized to make sure no data is missed.

Power Supply

Introduction

The 7912AD Power Supply provides operating power to all circuits in the instrument as well as the plug-ins. The supply also provides regulated power for the cooling fans to insure adequate cooling even at low line voltages. Remote ACTUATE and ENABLE inputs on the rear panel allow the 7912AD to be connected as part of a system with daisy-chained power control.

The Power Supply is represented on diagrams 31, 32, and 33.

Power Control and Fan Supply

Line Input. Line power is applied to the supply through J5402 (top-left of diagram 31). L5401, L5402, and C5400 suppress interference from the power line and keep the inverter signal from entering the power line. RT628 and RT622 limit the surge current demanded by the supply when it is first turned on. After the instrument is in operation, the resistance of these devices drops so they have little effect on the operation of the supply. The rear-panel PRINCIPAL POWER SWITCH (S5400) disconnects all input power from the instrument. During normal operation, this switch is left on and power is controlled by the front panel ON/OFF switch. S5402 opens the power input circuit if the internal temperature of the instrument rises beyond safe limits.

Line Selector Switch S5401 allows the 7912AD to operate from either a 115-volt nominal or 230-volt nominal line-voltage source. In the 115-volt position, CR364 and CR154 operate as a full-wave doubler. On alternate cycles of the line input power C110 and C310 (top-left corner of diagram 32) charge to near the peak voltage. The capacitors are in series with the input of the inverter, so the voltage applied to the inverter transformer is the peak-to-peak line voltage. When S5401 is set to the 230-volt position, CR364, CR258, CR262, and CR154 are connected as a full-wave bridge, and the output voltage across C110 and C310 is the peak value of the line voltage. As a result, the output voltage applied to the inverter stage is about the same for either 115-volt or 230-volt operation.

Power Control. T5404 (left-center of diagram 31) steps down the line voltage and provides operating power to the power control circuit. This circuit has power as long as the PRINCIPAL POWER SWITCH is on. The secondary of T5404 also provides a signal for the power-up comparators and a sample of the line signal for LINE triggering the horizontal plug-in.

CR538 and CR532 form a full-wave rectifier with C536 providing filtering. U444 regulates the output of the rectifier and filter. Power for the power control circuit is supplied through CR348.

When the front-panel ON/OFF button is pressed, $\overline{\text{POWER ON}}$ goes low, firing one-shot U166A. The positive transition on the Q output of U166A toggles flip-flop U364A. When the instrument is turned on, the Q output of U364A goes high and the output of U562B goes low, energizing relay K654. The S1 and S2 contacts of relay K654 close and apply power to the main inverter. The low on LOCKOUT also enables the main inverter oscillator.

If a TTL-level enable signal is connected to the rear-panel ACTUATE connector, this signal overrides the front-panel ON/OFF switch. When ACTUATE goes low, the set and clear inputs of U364A both go low. The Q output goes high, turning the power supply on through K654. When ACTUATE goes high, the set input of U364A goes high immediately. R372 and C472 hold the clear input low for a short time longer to insure that the flip-flop is cleared, turning the power supply off.

When the power supply is turned on, the high on the Q output of U364A forward biases CR566, turning Q574 off, and applying a high to pin 2 of U562A. The positive-going transition on U364A's output also fires U468B, and its $\overline{\text{Q}}$ output goes low for about 150 milliseconds. When U468B times out, pin 1 of U562A goes high and the output (pin 3) goes low, asserting ENABLE. The delay generated by U468B keeps the power-up surges from dasiy-chained instruments from occuring simultaneously. On power down, U468A is fired to generate a short delay before ENABLE goes high.

The positive transition on power up also fires one-shot U166B, pulsing RESET to initialize the power-on logic in the supply.

Fan Supply. The fan supply, shown at the top of diagram 31, generates regulated 60-hertz power for the cooling fan. Fig. 3-60 shows a simplified schematic of the fan circuit.

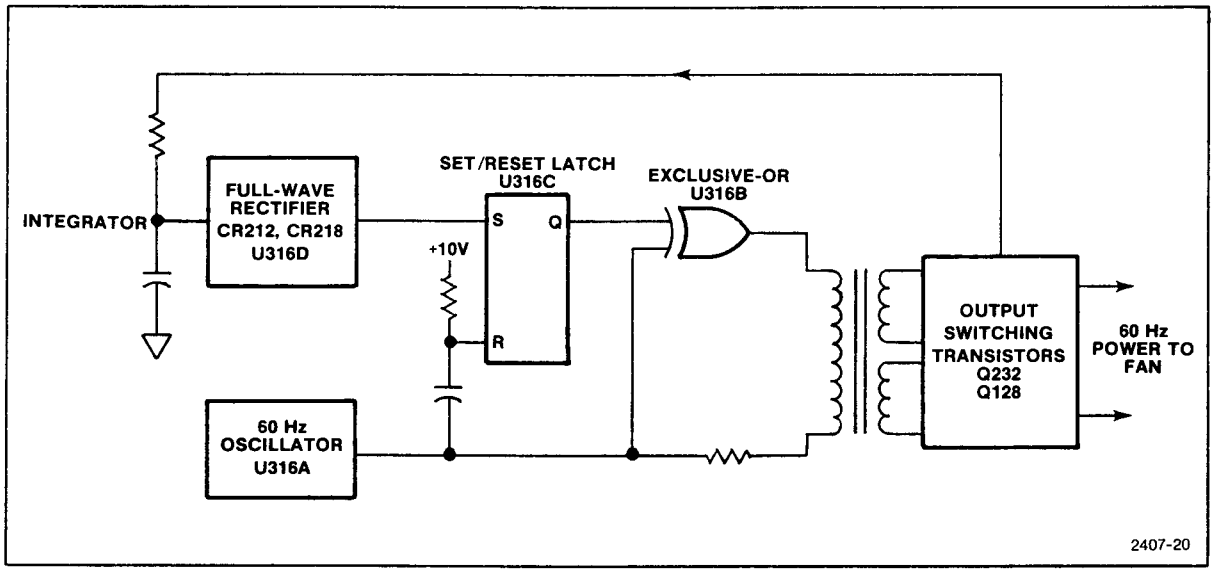


Fig. 3-60. Simplified block diagram of the fan circuit.

The R-C oscillator formed by U316A produces the basic 60-hertz clock for the fan supply. The clock signal is fed to R-S flip-flop U316C and one input of exclusive-OR gate U316B. On each transition of the clock, a pulse is passed through the differentiator formed by C416 and R308. Negative-going pulses are passed through CR314 to the non-inverting (+) input of U316B, while positive pulses are passed through CR412 to the inverting (-) input. The result is a negative-going output on every clock transition. R318 provides positive feedback to latch the output in its low state on each transition.

Referring to the timing diagram in Fig. 3-61, when the 60-hertz clock makes a negative transition, the output of R-S flip-flop U316C goes low, forward biasing CR414. This pulls pin 6 of U316B low, and the the output (pin 7) goes high. Since the output of U316A is low, current flows from the output of U316B through the primary of T512 and into the output of U316A. This provides base drive to one of the output transistors (Q232 and Q128) and reverse-biases the other.

A sample of the output voltage is fed back to the integrator formed by R124, R122 and C114. C114 begins to charge toward the fan voltage. CR212, CR218 and U316D comprise a full-wave rectifier with unity gain. When the charge on C114 reaches 10 volts, the output of U316D forward biases CR312, forcing pin 10 of U316C high enough to set the R-S flip-flop. Now the output of U316C is high and the output of U316A is low. The voltage on the non-inverting input (pin 6) of U316B is above 14 volts, so

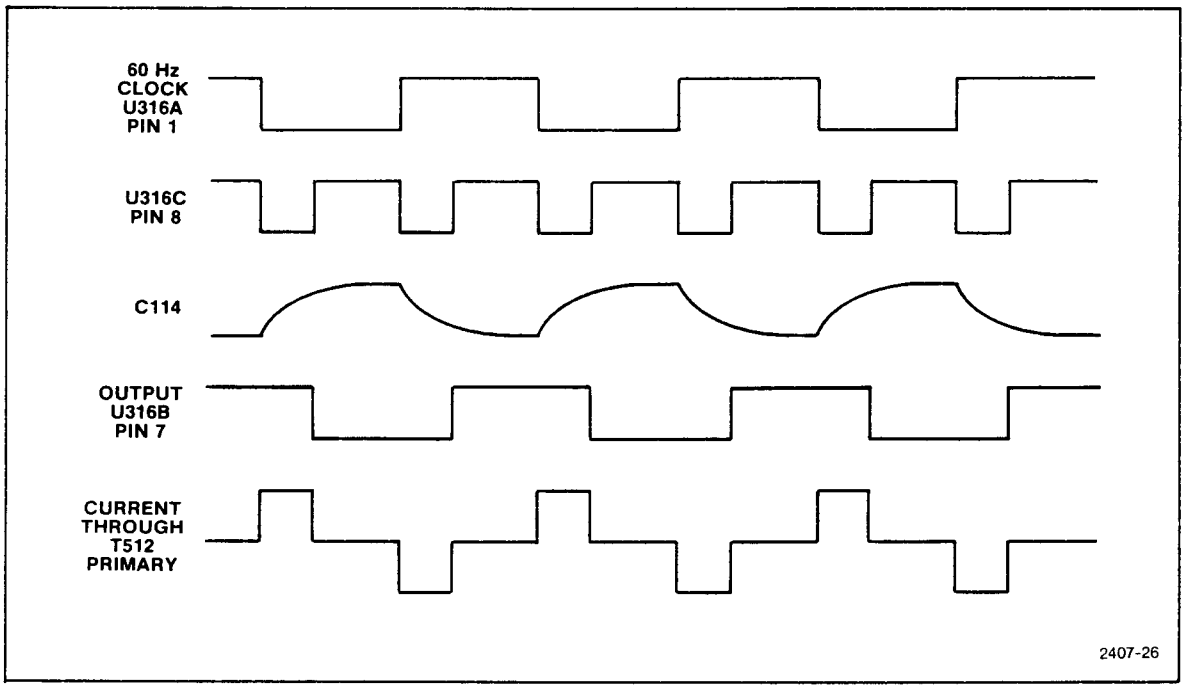


Fig. 3-61. Timing of the fan circuit.

the output of U316B goes low. Since both ends of the transformer primary are low, no current flows and both output transistors are cut off.

When the clock goes high, U316C is reset again and the output of exclusive-OR gate U316C goes low. Current flows in the opposite direction through T512, providing base drive to the other transistor. C114 begins to charge toward the fan voltage. When the charge reaches 10 volts, the R-S flip-flop is set and its output goes high, setting the output of exclusive-OR U316B high. With both sides of the transformer high, no primary current flows and the output transistors are cut off. Then the 60-hertz clock goes low, repeating the process.

If the fan voltage drops, the charge on C114 takes longer to reach the 10-volt threshold required to set the R-S flip-flop. As a result, the output current flows for a longer time, producing a constant volt-seconds product. Since the fan is an inductive load, a constant volt-seconds product produces constant current and constant speed.

Inverter/Rectifier (SN B100940 and Below)

Block Diagram. The Inverter/Rectifier circuit takes the filtered DC input from the line input stage and chops it to produce drive for the inverter transformer. The output of the inverter transformer is rectified and filtered to produce the semi-regulated voltages for the final regulators. Regulation of the main inverter is controlled by the +5.1-volt supply level, so no other regulation is required on this supply. Fig. 3-62 shows a block diagram of the Inverter/Rectifier circuit. The complete schematic diagram is shown on diagram 32.

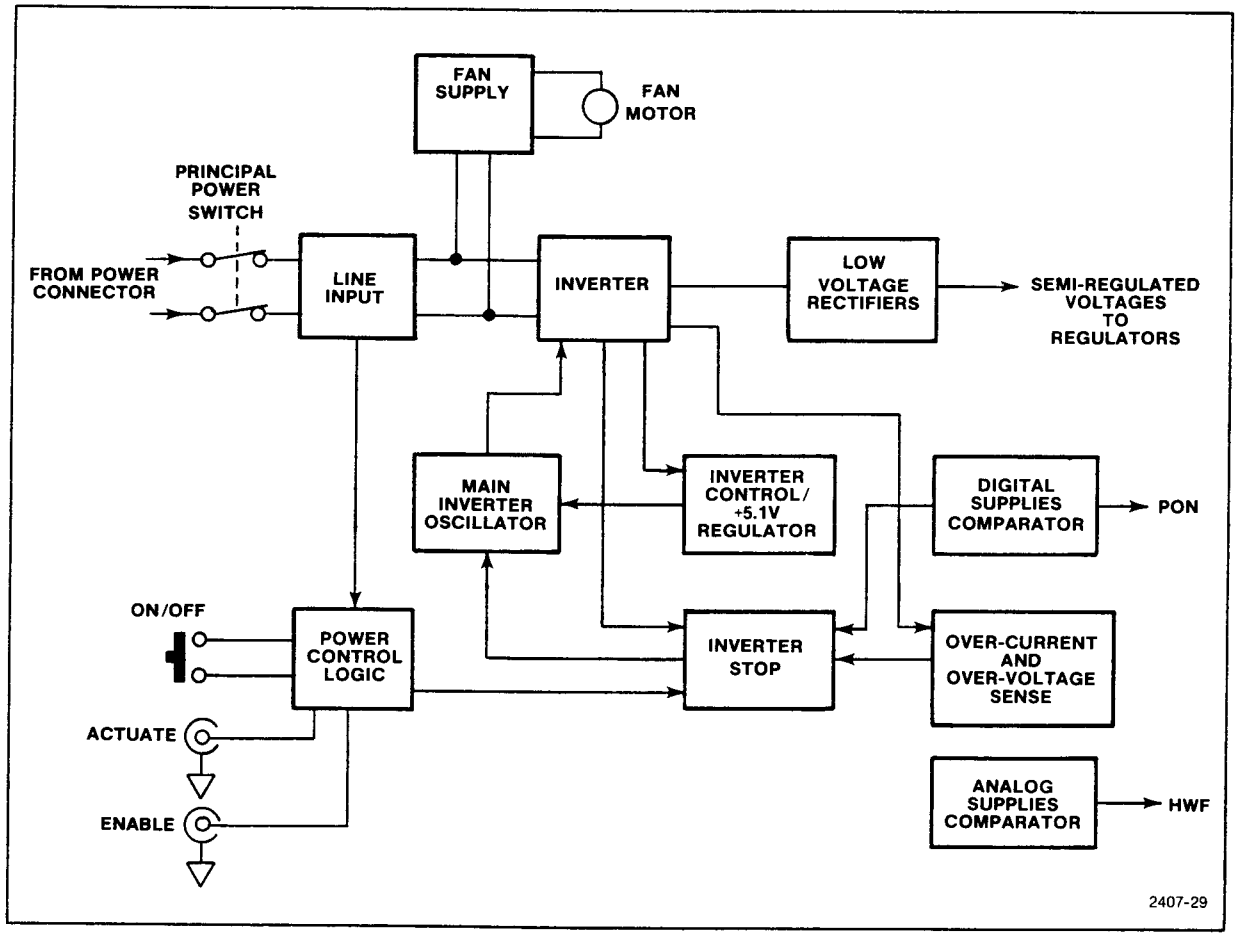


Fig. 3-62. Block diagram of the inverter/rectifier.

Main Inverter Oscillator. The Main Inverter Oscillator provides a 40-kilohertz square wave (at the output of U150A) to the chopping circuit. One-shots U150A and U150B, connected as an astable multivibrator, comprise the oscillator. The period of the oscillator is controlled by the R-C networks above each one-shot. R052 provides an adjustment for the period time. Q142 disables the oscillator is a fault in the power supply is detected.

+5-Volt Reference. U130B and the associated components comprise the +5-Volt Reference source. Zener diode VR520 generates the base reference voltage. The divider formed by R131, R130, and R133 sets the precise reference level. R010 provides an adjustment for the reference level, which controls the +5.1-Volt supply level. U130B is connected as a voltage follower, so its output provides a precise buffered reference.

Main Inverter. The clock signal from the inverter oscillator clocks J-K flip-flop U250. The J, K, clear, and preset inputs of U250 are tied high, so the flip-flop toggles on each clock pulse. The outputs of U250 drive the chop transistors Q240 and Q350 through high-power OR gates U350A and B. When the Q output of U250 goes high, the output of U350B goes high, turning Q240 on. Current flows through the top half of T340's primary, providing base drive to switching transistors Q318 and Q132. The $\overline{Q}$ output (pin 6) of U250 is low and the output of U350A is low, so Q350 is off, and no current flows through the bottom half of the transformer.

On the next positive edge of the inverter clock, the Q output of U250 goes low and the $\overline{Q}$ output goes high, turning Q350 on. Current flows in the bottom half of T340's primary, providing base drive to the opposite pair of switching transistors. CR240 and CR350 protect Q240 and Q350 from damage due to reverse-transients from the transformer.

The switching transistors, Q318, Q332, Q118, and Q132, provide drive to the primary of the main inverter transformer, T014. This transformer provides the raw 20-kilohertz AC voltages that are rectified, filtered, and fed to the low-voltage regulators. The rectifier and filter networks are shown to the left of the transformer.

Inverter Control. The positive-going transitions on the clock signal also fire one-shot U040A. When this one-shot times out, its $\overline{Q}$ output goes high, forcing the output of both OR gates (U350A and B) high. This turns both Q240 and Q350 on, and current flows in opposite directions through the bottom and top halves of T340's primary. This removes the drive from the secondary windings, and both pairs of switching transistors are cut off.

U130A, Q050, and the associated components control the period of one-shot U040A, which, in turn, controls the width of the drive pulses from the inverter. If the one-shot's period is reduced, the outputs of OR gates U350A and B go high sooner, and the drive and output pulse width is reduced. If the one-shot's period is increased, the drive and output pulse width increases. Thus, the period of U040A regulates the output voltage of the inverter.

U130A compares the +5.1-volt sense and the +5.1-volt ripple lines to the +5-volt reference. The output of U130A controls the timing current for U040A through Q050. The 5.1-volt ripple signal is AD coupled through C352 to pin 3

of U130A. This signal compensates for fast changes in the 5.1-volt supply, while the 5.1-volt sense line compensates for slower DC-level changes in the output.

Over-Current Protection. All the primary current for the main inverter transformer (T014) also flows through the primary of T630. This induces a proportional current in T630's secondary, which is sensed by R430. If the voltage across R430 rises to about 0.6 volts (corresponding to about one ampere of secondary current in T630), Q420 turns on and its collector drops to near ground potential. As a result, Q430 turns on, and its collector goes high, firing SCR (Silicon Controlled Rectifier) Q234. When the SCR fires, current flows through R134, the SCR, and CR240. This current turns Q142 on, shorting the timing current for U150 to ground, and stopping the inverter oscillator. This protects the inverter from excessive current due to a fault in the regulators or load.

When the over-current protection circuit is tripped during normal operation, the SCR (Q234) latches in the on state, disabling the inverter. During power-up, the over-current protection circuit is normally tripped several times while charging the large output filter capacitors, so the RESET line keeps the circuit from latching during power-up. RESET goes low at power-up forward-biasing CR220 and pulling the anode of Q234 near ground. About 700 milliseconds after power-up, RESET goes high, allowing the protection circuit to latch when tripped.

Over-Voltage Protection. Q520 compares the +5.1-volt ripple line to the +5-volt reference. If the ripple line rises to about 0.6 volts above the reference level, Q520 turns on, supplying base drive to Q142. Q142 turns on and disables the inverter oscillator until the +5.1-volt supply drops to the reference level.

Digital Supplies Comparator. U610A through D forms a comparator that monitors the state of the digital supplies and the AC line input. A sample of the line input power is rectified by CR300 and CR310, filtered by C500, and applied to U610C. If line power is present, U610C's output goes high. U610B monitors the -5.2-volt supply, while U610A monitors the -2-volt supply. If all of the supplies are up, the OR-tied outputs of U610A, B, and C go high, and the output of U610D goes low. CR524 clamps the low output at ground potential. If any of the supplies fall below acceptable levels, or the line power is interrupted, the output of U610D goes high, turning Q235 and forcing PON low. The low on PON tells the 6800 MPU to prepare for the loss of power.

The positive transition on U610D's output also turns Q140 on (left-center of the diagram), and its collector goes low, firing one-shot U040B. The $\overline{Q}$ output of U040B goes low, pulling the anode of CR040 low. This gives the 6800 microprocessor time to prepare for power-failure before the comparator can disable the inverter oscillator. If the comparator output is still high when the one-shot times out about 10 milliseconds later, CR242 conducts, turning Q142 on and disabling the inverter oscillator.

Inverter/Rectifier (SN B100941 and Up)

Block Diagram. (See Fig. 3-62.)

Main Inverter Oscillator. The Main Inverter Oscillator provides a 40-kilohertz square wave (at the output of U430F) to the chopping circuit. Comparator, U530B, connected as an astable multivibrator, comprises the oscillator. The period of the oscillator is controlled by the R-C network, C520, R529, and R510, for one-half the period; then by C520 discharging through CR520, and R528 for the second one-half period. R510 provides an adjustment for the period time. U530D disables the oscillator if a fault in the power supply is detected.

+2.5-Volt Reference. U550, a regulator, provides the 2.5-Volt reference source. The divider formed by R012, R010, and R111 sets the precise 5.1-volt sense reference level. R010 provides an adjustment for the reference level which controls the 5.1-volt supply level. U530C compares the reference level with a ramp, generated by Q530, R530, and C536, from the oscillator. The resultant from U530C controls the duty factor of the final waveform going into the primary of T360, as explained below.

Main Inverter. The clock signal from the inverter oscillator, after NANDing with the regulation signal, clocks J-K flip-flop, U570A. The J, K, clear, and preset inputs of U510A are tied high so the flip-flop toggles on each clock pulse. The outputs of U570A drive the chop transistors, Q372 and Q370, through high-power OR gates, U572A and B. When the Q output of U570A goes high, the output of U572A goes low, turning Q372 on. Current flows through the top half of T360's primary, providing base drive to the switching transistors, Q318 and Q132 (Socket Board--A84). The $\overline{Q}$ output (pin 14) of U570A is low and the output of U572B is high, so Q370 is off, and no current flows through the bottom half of the transformer.

On the next positive edge of the inverter clock, the Q output of U570A goes low and the $\overline{Q}$ output goes high, turning Q370 on. Current flows in the opposite pair of switching transistors, Q332 and Q118. CR374 and CR376 protect Q372 and Q370 from damage due to reverse-transients from the transformer. R372 and R370 provide pull-up to U572A and B when they are not asserted (low).

The switching transistors, Q318, Q332, Q118, and Q132, provide drive to the primary of the main inverter transformer, T014. This transformer provides the raw 20-kilohertz AC voltages that are rectified, filtered, and fed to the low-voltage regulators. The rectifier and filter networks are shown to the left of the transformers.

Inverter Control. The output from U530C asserts the set of J-K flip-flop U570B, causing $\overline{Q}$ to go low; unless the oscillator is in its high state, clearing U570B and causing $\overline{Q}$ to remain high. With $\overline{Q}$ low, this places a low at the outputs of U572A and B. Note that the output of U530C also inhibits the

oscillators clocking of U570A, so that after U530C becomes unasserted, U570A will be on the right edge of the incoming clock. When the outputs of U572A and B are low, this turns both Q372 and Q370 on, thus allowing current to flow in opposite directions through the bottom and top halves of T360's primary. This removes the drive from the secondary windings, and both pairs of switching transistors are cut off.

U530C and the associated components control the period that U570B is set, which in turn controls the width of the drive pulses from the inverter. If the U530C's period is reduced, the outputs of OR gates U572A and B go low sooner, and the drive and output pulse width is reduced. If the U530C's period is increased, the drive and output pulse width increases. Thus, the period of U530C regulates the output voltage of the inverter.

U530C's inverting input combines the +5.1-volt sense, +5.1-volt ripple lines, and the Line Sense. The 5.1-volt ripple signal is AC coupled through C546 to pin 8 of U530C. This signal compensates for the fast changes in the 5.1-volt supply, while the 5.1-volt sense line compensates for slower dc level changes in the output.

Over-Current Protection. All the primary current for the main inverter transformer (T014) also flows through the one turn primary of T260. This induces a voltage in T260's multi-turn secondary, which is rectified by a full-wave bridge (CR370, CR372, CR470, and CR472). U530A's non-inverting input is sensed at 5.6 volts by VR430. If the voltage across R562 rises to above +5.6 volts, then U530A asserts its output low. As a result, Q422 turns on, and its collector goes high, making U430D output go low. The time during which U430D is low, creates a voltage level determined by R542 and C440. This level is compared to the ramping voltage of the main oscillator, U530B, by U530D. If too much current is sensed by T260, the resulting level on U530D asserts the output low, and the switch transformer, T360, is disabled. As soon as the current level decreases to an allowable level, the transformer, T360, is again enabled.

Over-Voltage Protection. CR540 allows the +5.1-volt ripple line to assert U530A if its voltage becomes too large. If the ripple line rises to about 0.6 volts above the reference level, then U530D asserts and disables the drive to T360. This continues until the 5.1-volt supply drops to the reference level.

Digital Supplies Comparator. U410A, U410B, and U410D form a comparator that monitors the state of the digital supplies and the AC line input. A sample of the line input power is rectified by CR020, CR021, CR010, and CR011; then it is filtered by C111, and then applied to U410A. If line power is present, U410D's output goes high. U410B monitors the -5.2-volt supply, while U410D monitors the -2-volt supply. If all the supplies are up, the OR-tied outputs of U410A, U410B, and U410D go high, which in turn causes U560's and U430's outputs to go high. If any of the supplies fall below acceptable levels, or the line power is interrupted, the associated output of the comparators assert low, through U560B, and U430C forces PON low. The low on PON tells the 6800 MPU to prepare for the loss of power.

Low-Voltage Regulators

Overview. The low-voltage regulators convert the semi-regulated voltages from the Converter/Rectifier to low-ripple regulated output voltages. The regulators are series-pass type, using the -50-volt supply as a reference level. Diagram 33 shows the low-voltage regulators.

All of the regulators, except the +130-volt and +365-volt circuits, use remote sensing, Since the load current varies over a considerable range, the losses in the supply cabling also vary. Sensing the output voltage at the supply would not take these losses into account, so a low-current sample of the supply voltage is fed back from the load. This allows the regulators to compensate for variations in wiring losses and, as a result, hold the voltage at the load constant regardless of the load current.

-50-Volt Regulator. A semi-regulated -54-volt supply is fed to this regulator circuit in the bottom-right of diagram 33. The comparator formed by Q228 compares the voltage fed back on the sense line (-50V SENS) to a reference level set by zener diode VR328. R504, R506, and R508 divide the sense voltage down to match the reference level and R508 provides an adjustment to precisely set the -50-volt supply level. Any difference between the sense and reference levels is fed to the regulator as a correction voltage.

If the output voltage decreases (becomes less negative) due to an increase in load current or a decrease in input voltage (as a result of line-voltage changes or ripple), the voltage across divider R504-R506-R508 decreases. This results in a more positive level at the base of Q228A than that established by the reference level on the base of Q228B. The collector current in Q228A increases, increasing the drive to Q128. Q128 begins to conduct more current, increasing the drive to Q028 and the series regulator, Q022. When the current through Q022 increases, the load current increases and the output voltage increases (becomes more negative). The sense voltage fed back to the regulator reflects the increased output voltage and the base of Q228A returns to the same level as the reference.

Similarly, if the output voltage increases (becomes more negative), the sense voltage increases, decreasing the collector current in Q228A, and decreasing the drive to Q022. This reduces the current supplied through Q022, decreasing the output voltage of the supply.

The -50-volt supply is protected from excessive load current by Q118. The load current flows through the series regulator, Q022 and sense resistor R024. Under normal operating conditions, the voltage drop across R024 is not sufficient to forward bias Q118. If the load current increases beyond a safe level, the voltage drop across R024 forward biases Q118. The collector current in Q118 reduces the current available to drive Q128, effectively limiting the drive to Q028 and Q022. This current limiting protects Q022 from damage due to excessive power dissipation when excessive load current is demanded.

CR502 prevents the output of the supply from going more positive than about +0.6 volts if it is shorted to a positive supply.

-15,+15,+5, and +50-Volt Regulators. The -15, +15, +5, and +50-volt supplies are functionally identical to -50-volt supply. We will discuss the -15-volt supply (shown directly above the -50-volt supply) as an example. The reference level for voltage comparator Q306 is derived from the -50-volt sense level. R404 and R406 divide the -50V SENS voltage down to -15 volts for comparison with the -15V SENS signal. Any change in the output of the -15-volt supply appears at the base of Q306B as an error signal. This error signal controls the regulator as described in the -50-volt supply description.

The over-current protection circuit is similar to the -50-volt circuit. Q102 is connected as a comparator. If the load current causes sufficient voltage drop across R004 to switch the comparator, Q102A turns off and Q102B turns on, limiting the drive to Q202 and the series pass transistor Q012.

CR102 clamps the -15-volt output to +0.6 volts if it is shorted to a positive supply.

+130 and +365-Volt Regulators. The +130 and +365-volt supplies are functionally identical. We will discuss the +130-volt supply (shown in the top-center of diagram 33) as an example.

The +130 and +365-volt supplies do not supply the heavy current demands that the other low-voltage supplies do. As a result, the line losses are not as significant in these supplies and the remote sensing system used in the other supplies is not necessary. Instead, the output voltage of the +130-volt supply is fed back to the comparator through the voltage divider formed by R537, R530, and R531. This network divides the feedback voltage down so that under normal operating conditions, the base of Q534A sits near ground potential. If the output voltage falls, the voltage on the base of Q534A also drops, turning Q534B on. As the collector current through Q534B increases, its collector voltage drops, decreasing the drive to Q538. The decrease in collector current through Q538 increases the base current in Q634 and the series pass transistor, Q526. The increase in current through Q526 increases the output voltage to correct for the drop.

Over-current is sensed by R639 and Q636. If load current increases beyond a safe limit, the voltage drop across R639 forward biases Q636, decreasing the base drive for Q634 and Q526. This limits the current through the pass transistor to a safe level.

-5.2 and -2-Volt Regulators. The -5.2-volt and -2-volt regulators use an integrated circuit operational amplifier for the comparator functions. These regulators supply heavy current demands, so they use remote sensing to regulate output voltage. The -5.2-volt and -2-volt supplies provide substrate bias to many integrated circuits in the instrument. As a result, their output voltage is critical, and the voltage is sensed against the +5.1-volt supply and COM SENS (COMmon SENSe). If the common (ground) or +5.1-volt supply level shifts, these supplies will shift to compensate for the change.

The two supplies are functionally identical. We will discuss only the -5.2-volt supply in detail.

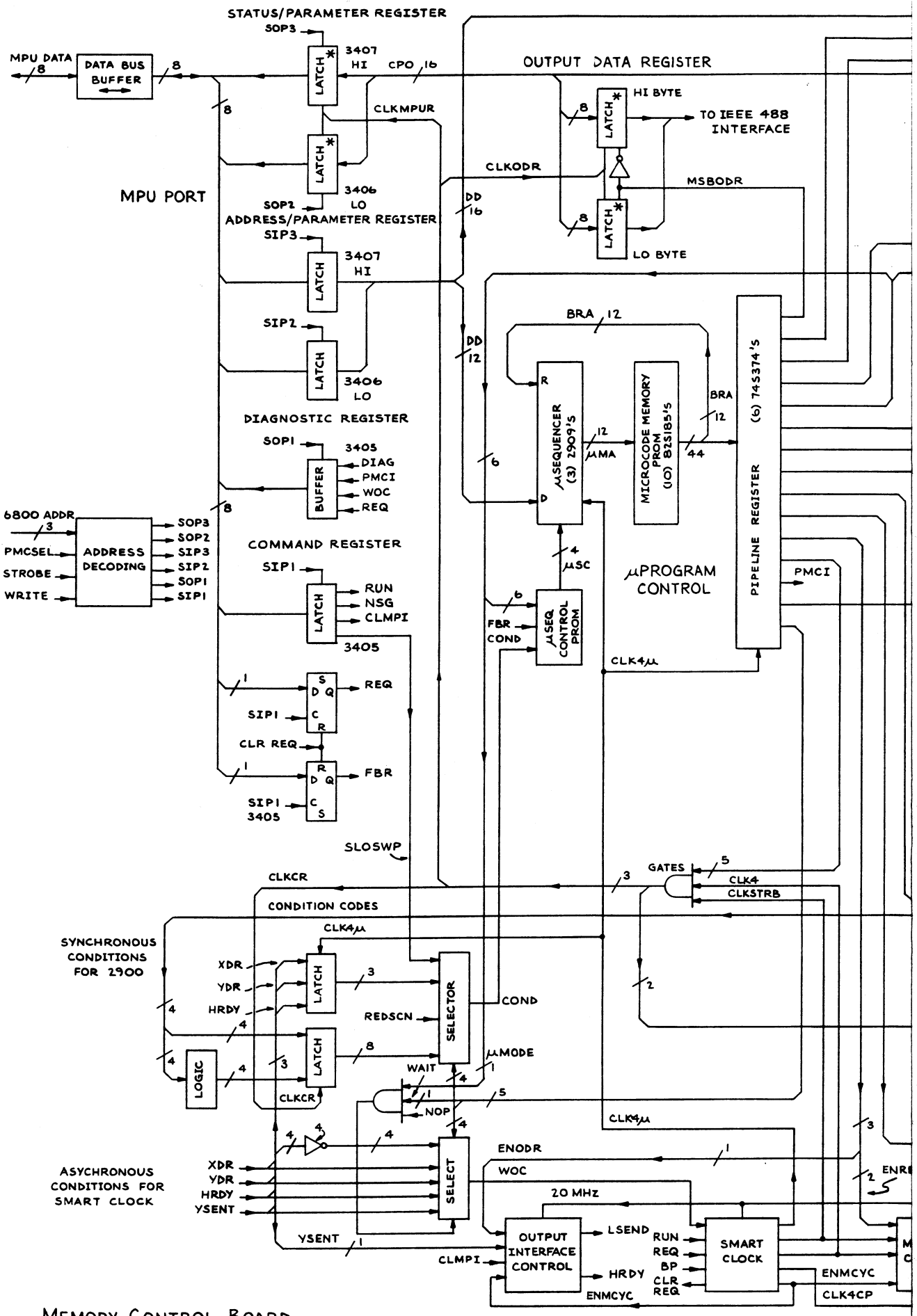
The output voltage at the load is fed back on the -5.2 SENS line. This voltage is divided down by R612, R613, and R615 to near ground potential. The resulting voltage is compared to the COM SENS level by U628A. The output of this comparator provides base current to Q626 through CR608 and R618. If the supply voltage at the load falls, the voltage on -5.2V SENS also falls (becomes less negative) and the output of U628A goes more negative, increasing the base current to Q626. This increases the drive to Q738 causing its collector current to increase and its collector voltage to go more positive. The base drive to Q748 increases and as a result, the output current and voltage increase to compensate for the change.

U628B and the associated components protect the regulator from damage due to excessive load current. The load current passes through R714, producing a voltage drop across the resistor which is proportional to the load current. R726 and R728 divide the potential at the bottom of the sense resistor down and U628B compares the result to the potential at the top of the sense resistor (the supply line). If the load current exceeds a safe level, drop across R714 causes the inverting (-) input of U628B to become more negative than the non-inverting (+) input. The output of U628B goes to about +5 volts, decreasing the drive current to Q626 and Q738 and limiting the drive current for the pass transistor Q748. This protects the output transistor from excessive dissipation due to excessive load current.

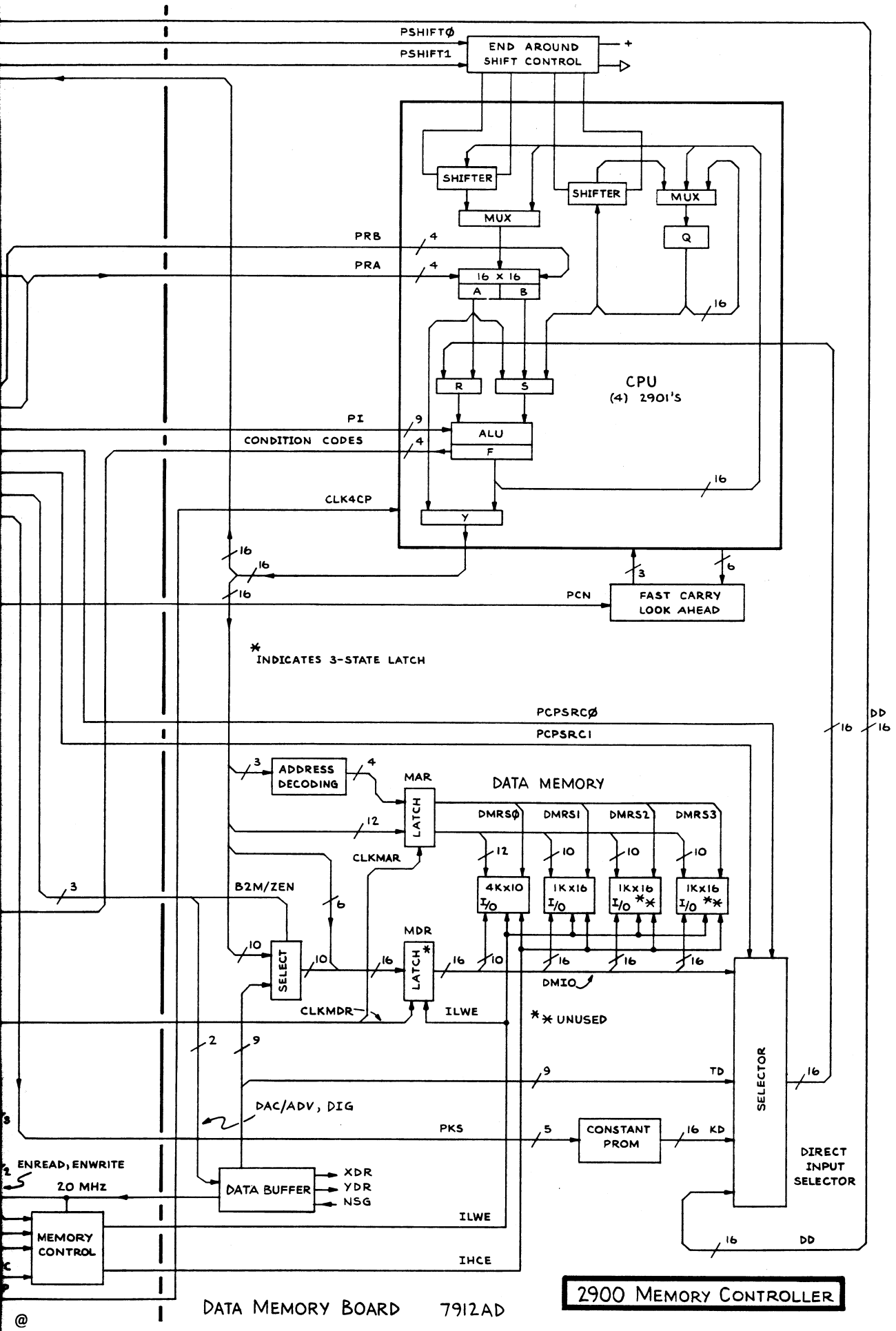
Analog Supplies Comparator. U248, Q246, Q248, Q258, and the associated components (bottom-left of diagram 33) monitor the analog supplies and generate an interrupt to the 6800 MPU if any of the supplies fail. During normal operation, the output of U248 is low. Q246 and Q248 are off and Q258 is on, so REG UP (Regulator Up) is low. This line is inverted by Q600 (SN B100940 and below) or U430B (SN B100941 and up) to drive the $\overline{\text{HWF}}$ line. If any of the analog supplies fail, REG UP goes high, and $\overline{\text{HWF}}$ goes low, generating an interrupt to the MPU. The instrument reports a power-fail error when polled in this condition. After the instrument has been polled, it will respond to the ERR? query with error code 401 (decimal).

Power Distribution

The outputs of the power supply are distributed to the instrument through the Power Connector board (A62). This circuit card plugs into J104 on the Main Interconnect board, next to the power supply. The supplies are fed through the Connector board to the Main Interconnect, and to the instrument circuitry. The Power Connector board provides a common connection point for all the supply outputs, making it a simple task to remove the supply from the instrument.



MEMORY CONTROL BOARD



DESTINATION FUNCTIONS

*4

		B REG.	Q REG.	ALU OUT
0 0 0 X X	FTOQ		Q←F	Y←F
0 0 1 X X	FOUT			Y←F
0 1 0 X X	FTOBA	B←F		Y←A
0 1 1 X X	FTOB	B←F		Y←F
1 0 0 0 0	SRQBØ	B←F/2	Q←Q/2	Y←F
1 0 0 0 1	SRQB1			
1 0 0 1 0	SRQBR			
1 0 0 1 1	SRQBA			
1 0 1 0 0	SRBØ	B←F/2		Y←F
1 0 1 0 1	SRB1			
1 0 1 1 0	SRBR			
1 0 1 1 1	SRBA			
1 1 0 0 0	SLQBØ	B←2F	Q←2Ø	Y←F
1 1 0 0 1	SLQB1			
1 1 0 1 0	SLQBR			
1 1 0 1 1	SLQBA			
1 1 1 0 0	SLBØ	B←2F		Y←F
1 1 1 0 1	SLB1			
1 1 1 1 0	SLBR			
1 1 1 1 1	SLBA			

NOTE:
Q AND B REGISTERS
LINKED ONLY IN
ARITHMETIC SHIFT MODE.

SHIFT MODES

0 0	SHIFT IN (Ø)
0 1	SHIFT IN (1)
1 0	ROTATE
1 1	ARITHMETIC SHIFT

ALU OPE

0 0 0 0	F← R+S
0 0 0 1	F← R+S+1
0 0 1 0	F← −R+S−1
0 0 1 1	F← −R+S
0 1 0 0	F← R−S−1
0 1 0 1	F← R−S
0 1 1 X	F← R/S = R∨S
1 0 0 X	F← R&S = R∧S
1 0 1 X	F← NR&S = $\overline{R}$∧S
1 1 0 X	F← R#S = R⊻S
1 1 1 X	F← N(R#S) = $\overline{R⊻S}$

R	S	
0 0 0	A	Q
0 0 1	A	B
0 1 0	0	Q
0 1 1	0	B
1 0 0	0	A
1 0 1	D	A
1 1 0	D	Q
1 1 1	D	0

CPU OPERATION MODE

MODE CONTROL BIT

μSEQ OPERATION MODE

43	42	41	40
0	I_8	I_7	I_6
1	0	0	1

A-REGISTER ADDRESS

39	38	37	36
A3	A2	A1	A0

*3

B-REGISTER ADDRESS

35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20
B3	B2	B1	B0	S_1	S_0	I_5	I_4	I_3	I_2	I_1	I_0	C_N	K_4	K_3	K_2
		P WAIT	PNC	PSC_3	PSC_2	PSC_1	PSC_0	A11	A10	A9	A8	A7	A6	A5	A4

CONSTANT PR

BRANCH ADDRESS

μSEQUENCER CONTROL

*2

		SI	SS	FE	PUP	
0 0 0 0	CONT	0	0	1	X	CONTINUE
0 0 0 1	POP	0	0	0	0	POP STK
0 0 1 0	PUSH	0	0	0	1	PUSH μPC
0 0 1 1	EXITL	0	1	0	0	POP STK AND USE AR FOR ADDRESS
0 1 0 0	JSR	0	1	0	1	PUSH μPC AND JMP TO ADDRESS IN AR
0 1 0 1	JMP	0	1	1	X	JMP TO ADDRESS IN AR
0 1 1 0	RTS	1	0	0	0	JMP TO ADDRESS IN STKØ AND POP STK
0 1 1 1	LOOP	1	0	1	X	JMP TO ADDRESS IN STKØ
1 0 0 0	POPIF	0	0	0	0 / 0	0 1 X POP OTHERWISE CONTINUE
1 0 0 1	PUSHIF	0	0	0	1 / 0	0 1 X PUSH OTHERWISE CONTINUE
1 0 1 0	EXITLIF	0	1	0	0 / 0	0 1 X EXITL OTHERWISE CONTINUE
1 0 1 1	USRIF	0	1	0	1 / 0	0 1 X USR OTHERWISE CONTINUE
1 1 0 0	JMPIF	0	1	1	X / 0	0 1 X JMP OTHERWISE CONTINUE
1 1 0 1	ENDLIF	0	0	0	0 / 1	0 1 X POP OTHERWISE LOOP
1 1 1 0	RTSIF	1	0	0	0 / 0	0 1 X RTS OTHERWISE CONTINUE
1 1 1 1						

CONDITION SELECT

0 0	0 0 0 0	EQ = Z	
0 1	0 0 0 0	NE = $\overline{Z}$	
0 0	0 0 0 1	CS OR HIS = C	
0 1	0 0 0 1	CC OR LO = $\overline{C}$	
0 0	0 0 1 0	VS = V	
0 1	0 0 1 0	VC = $\overline{V}$	
0 0	0 0 1 1	MI = N	SYNCHRONOUS C
0 1	0 0 1 1	POS = $\overline{N}$	UPDATED BY ENC
0 0	0 1 0 0	LT = N⊕V	
0 1	0 1 0 0	GE = $\overline{N⊕V}$	
0 0	0 1 0 1	LE = Z+(N⊕V)	
0 1	0 1 0 1	GT = $\overline{Z+(N⊕V)}$	
0 0	0 1 1 0	LOS = $\overline{C}$+Z	
0 1	0 1 1 0	HI = $\overline{C}$+Z	
0 0	0 1 1 1	RSCAN = REDUCED SCAN	HARD
0 1	0 1 1 1	NRSCAN = NORMAL SCAN	
0 0	1 0 0 0	XDR = X-DATA RDY	
0 1	1 0 0 0	NXDR = X-DATA NOT RDY	
0 0	1 0 0 1	YDR = Y-DATA RDY	SY
0 1	1 0 0 1	NYDR = Y-DATA NOT RDY	TO
0 0	1 0 1 0	IR = INTERFACE RDY	
0 1	1 0 1 0	NIR = INTERFACE NOT RDY	
0 0	1 0 1 1	SLOSWP = SLOW SWEEP	
0 1	1 0 1 1	NSLOSWP = NORMAL SWEEP	
0 0	1 1 0 0	MPU1	MPU
0 1	1 1 0 0	NMPU1	
0 0	1 1 0 1	MPU2	
0 1	1 1 0 1	NMPU2	
0 0	1 1 1 0	MPU3	
0 1	1 1 1 0	NMPU3	
0 0	1 1 1 1	COZ = C+Z	UPDATED BY EN
0 1	1 1 1 1	NCOZ = $\overline{C+Z}$	

UNSIGNED CONDITION (A-B)

HIS	A ≥ B	C
HI	A > B	$\overline{(\overline{C}+Z)}$
LOS	A ≤ B	$\overline{C}$+Z
LO	A < B	$\overline{C}$
EQ	A = B	Z
NE	A ≠ B	$\overline{Z}$

SIGNED CONDITION (A-B)

GE	A ≥ B	$\overline{(N⊕V)}$
GT	A > B	$\overline{Z+(N⊕V)}$
LE	A ≤ B	Z+(N⊕V)
LT	A < B	N⊕V
EQ	A = B	Z
NE	A ≠ B	$\overline{Z}$

ASYNCHRONOUS CONDITIONS FOR SMART

1 X	X 0 0 0	WNXDR = WHEN X-DATA NOT RDY
1 X	X 0 0 1	WNYDR = WHEN Y-DATA NOT RDY
1 X	X 0 1 0	WNIR = WHEN INTERFACE NOT R
1 X	X 0 1 1	WNYSENT = WHEN YSENT NOT ASS
1 X	X 1 0 0	WXDR = WHEN X-DATA RDY
1 X	X 1 0 1	WYDR = WHEN Y-DATA RDY
1 X	X 1 1 0	WIR = WHEN INTERFACE RDY
1 X	X 1 1 1	WYSENT = WHEN YSENT ASSERTED

@

ALU OPERATION

*2

A	-A	NA	A+1	A-1	-A-1	∅
B	-B	NB	B+1	B-1	-B-1	
Q	-Q	NQ	Q+1	Q-1	-Q-1	
D	-D	ND	D+1	D-1	-D-1	
A+Q		A+B	D+A	D+Q		
A+Q+1		A+B+1	D+A+1	D+Q+1		
Q-A-1		B-A-1	A-D-1	Q-D-1		
Q-A		B-A	A-D	Q-D		
A-Q		A-B	D-A	D-Q		
A-Q-1		A-B-1	D-A-1	D-Q-1		
A/Q		A/B	D/A	D/Q	⇒	(R∨S)
A&Q		A&B	D&A	D&Q	⇒	(R∧S)
NA&Q		NA&B	ND&A	ND&Q		
A#Q		A#B	D#A	D#Q	⇒	(R⊻S)
N(A#Q)		N(A#B)	N(D#A)	N(D#Q)		

NOTE:
*INDICATES INFORMATION IN EACH AREA ASSOCIATES WITH A NUMBER ON TABLE, ASSEMBLER SOURCE STATEMENT FIELDS.

DIRECT DATA SELECT

*5

0 0	MPU	6800 BUS
0 1	K#	CONSTANT PROM
1 0	LATAM	DATA MEMORY
1 1	DATAB	DATA BUFFER

CONSTANT PROM ADDRESS

K_4	K_3	K_2	K_1	$K_\emptyset$															
22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

*6

CH ADDRESS *4

A6	A5	A4	A3	A2	A1	A0

UNUSED BITS

ENMDR
B2M/ZEN
ENODR
MSBODR
ENCR
ENMAR
ENWRITE
ENREAD
DIG
DAC/ADV
ENMPUR
PMCI

ELECT

*3

HRONOUS CONDITIONS
TED BY ENCR SIGNAL

N } HARDWARE STRAP

RDY
RDY } SYNCHRONIZED TO CLK4μ
RDY

EEP } MPU-6800 INPUTS

TED BY ENCR

SMART CLOCK

NOT RDY
NOT RDY
ACE NOT RDY
T NOT ASSERTED
RDY
RDY
CE RDY
ASSERTED

EXTERNAL VARIABLES

ENMDR - LOAD MEMORY DATA REGISTER
B2M/ZEN - DATA BUFFER TO MDR/Z-AXIS ENABLE (XYZ)
ENODR - LOAD OUTPUT INTERFACE
MSBODR - ENABLE THE MSB OF OUTPUT DATA REGISTER

ENCR - LOAD CONDITION CODE REGISTER
ENMAR - LOAD MEMORY ADDRESS REGISTER
ENWRITE - BEGIN DATA MEMORY WRITE CYCLE
ENREAD - BEGIN DATA MEMORY READ CYCLE

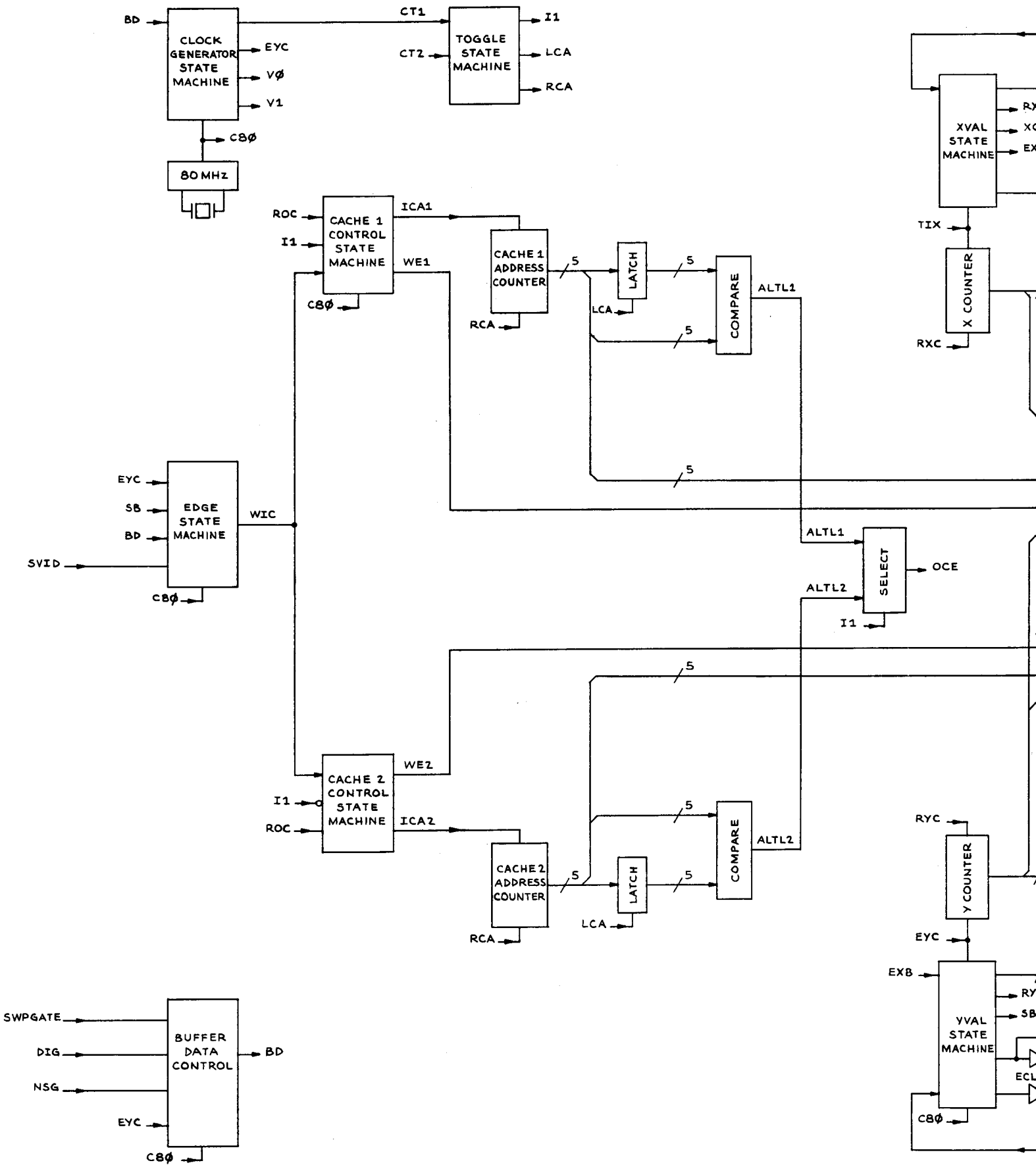
DIG - DIGITIZE
DAC/ADV - DATA ACCEPTED (DATA BUFFER)/ ADVANCE (XYZ DISPLAY)
ENMPUR - LOAD MPU (6800) REGISTER
IMPU - INTERRUPT 6800 MPU

ASSEMBLER SOURCE STATEMENT FIELDS

MODE	1	2	3
CPU OP / μSEQ OP	LABEL / LABEL	ALU OP CONTROL	A REG, B REG CONDITION
	4	5	6
CPU OP / μSEQ OP	DESTINATION / BRANCH ADDR	CPU SELECT	EXT VAR / EXT VAR

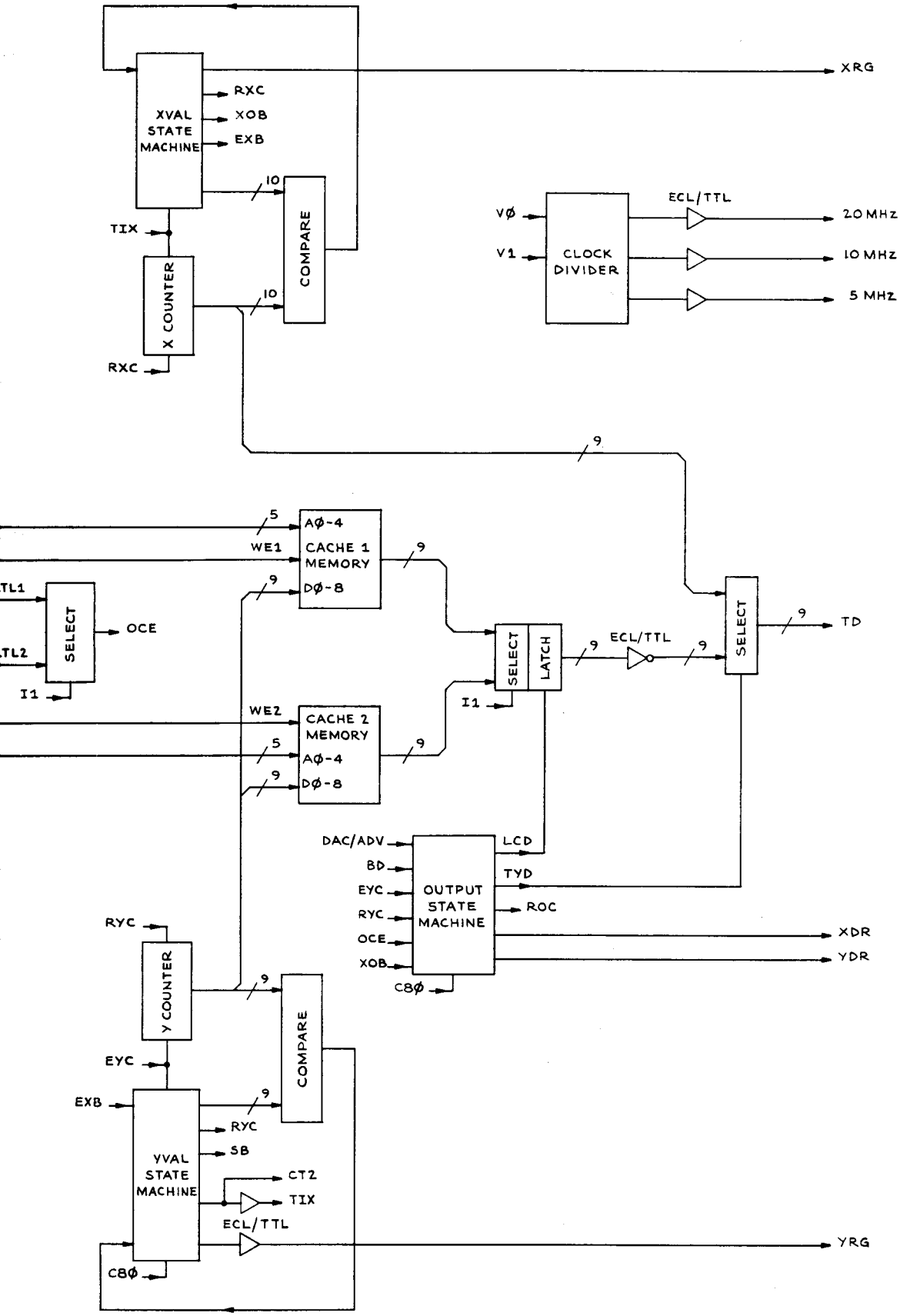
PIPELINE REGISTER FORMAT 7912AD

PIPELINE REGISTER FORMAT



7912AD

@



DATA BUFFER

@

DATA BUFFER

DATA BUFFER SIGNALS

ALTL1	Address Less Than Latch 1
ALTL2	Address Less Than Latch 2
BD	Buffer Data
BY1Ø-8	Buffer 1 Y data bits Ø-8
BY2Ø-8	Buffer 2 Y data bits Ø-8
CDB	Composite Digital Blanking
CT1	Cache Toggle 1
CT2	Cache Toggle 2
DAC/ADV	2900 Data ACcepted (or ADVance for XYZ)
DIG	DIGitize
DR	Data Ready
ECNT	Enable Y state couNTer
EJMP	Enable output state counter JuMP
EXB	Enable X Blanking
EYC(A,B)	Enable Y Counter (A,B are buffered)
I1	Input cache 1
ICA1	Increment Cache 1 Address
ICA2	Increment Cache 2 Address
LCA	Latch Cache Address
LCD	Latch Cache Data
NSG	No Sweep Gate required
OCE	Output Cache Empty
RCA	Reset Cache Address
ROC	Read Output Cache
RYC	Reset Y Counter
SB	Storage Blanking
SVID	Schmitted VIDeo
SWPGATE	SWeeP GATE
TIX	Increment X counter
TRXC	Reset X Counter
TYØ-8	Y data bits Ø-8
TYD	Y Data
WE1	Write Enable cache 1
WE2	Write Enable cache 2
WIC	Write Input Cache
XD	X Data
XDR	X Data Ready
XOB	X Output Blanking
XRG	X Ramp Gate
YØ-8	Y data bits Ø-8
YDR	Y Data Ready
YRG	Y Ramp Gate

Bars above signal names on schematics indicate the signal is asserted low.

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: June 9, 1983 Change Reference: M45437

Product: 7912AD Service Vol.1 Manual Part No.: 070-2407-00

DESCRIPTION

EFF SN: B111166

TEXT CHANGES

For Page 3-43, Fig. 3-11.
CHANGE TO READ:

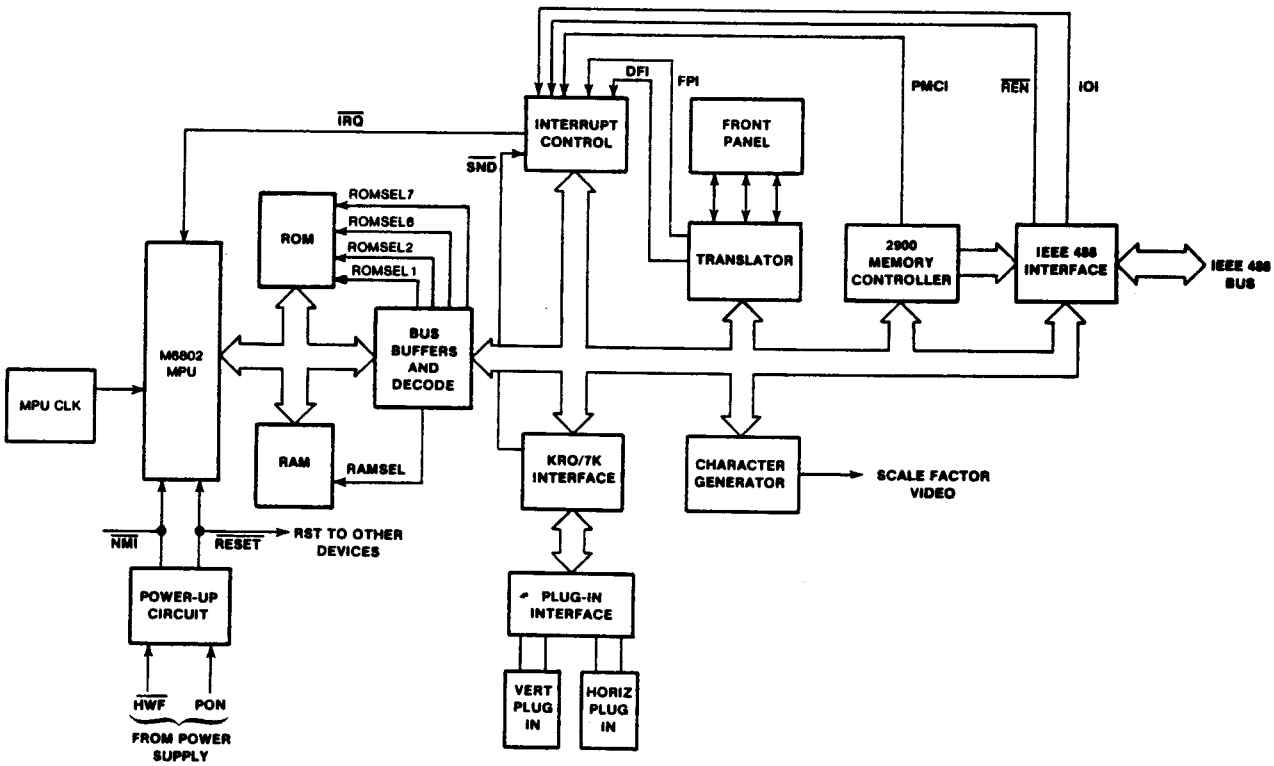


Fig. 3-11. Block diagram of the 6802 MPU system.

DESCRIPTION

For Page 3-44, Paragraphs 1 & 2.
CHANGE TO READ:

The firmware operating system that directs the MPU's activity is resident in 12 k (1 k = 1024) bytes of ROM (Read-Only Memory) on the MPU board (A54). The MPU system also uses 1 k bytes of RAM (Random-Access Memory) as a "scratch pad". A limited amount of the RAM space is available for diagnostic purposes.

6802 MPU Architecture

Before we discuss the microprocessor system as it is used in the 7912AD, a review of the 6802 MPU might be helpful. For more information on the 6802, refer to the Motorola 6800 Microcomputer Design Data Manual. Figure 3-12 shows a block diagram of the 6802 internal architecture. The 6802 is an 8-bit parallel processor with an 8-bit bidirectional data bus and a 16-bit address bus. The MPU consists of the following functional units:

Two 8-bit Accumulators
Program Counter
Stack Pointer
Index Register
Condition Code Register
Arithmetic Logic Unit (ALU)
Instruction Register and Decoder/Timing
Data and Address Buffers

DESCRIPTION

For Page 3-45, Fig. 3-12.
CHANGE TO READ:

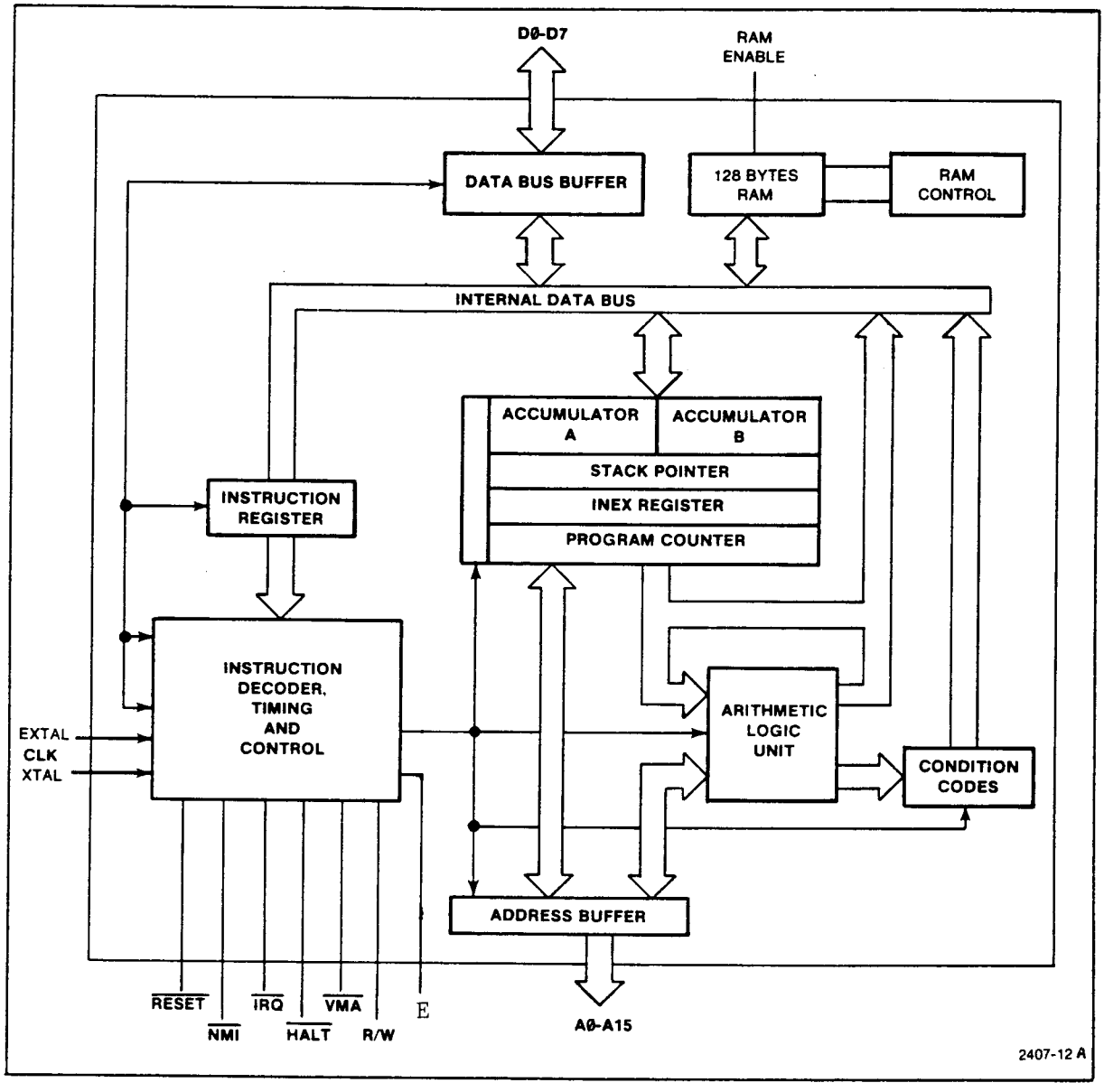


Fig. 3-12. Block diagram of the 6802 internal architecture.

DESCRIPTION

For Page 3-46
CHANGE TO READ:

Index Register. The index register can be used to store 16-bit data or an address used in the indexed mode of memory addressing. Instructions are provided in the 6802 instruction set that load, increment, decrement, compare, etc. the index register.

Instruction Register and Decoder/Timing. During an instruction fetch (the first one, two, or three machine cycles, depending on the instruction), successive bytes of an instruction are loaded from the program memory into the instruction register. The contents of this register are, in turn, passed to the decoder and timing logic which decodes the byte(s) and generates the machine states and control signals necessary to execute the instruction. The timing and control block also generates and receives the external control signals.

Data and Address Buffers. These three state buffers isolate the 6802 internal busses from the external data and address busses. The data bus buffer is bidirectional.

RAM/RAM Control. (Not used) Internal RAM is used as primary RAM for program flow or as 128 bytes of extra RAM, 32 bytes of which could be maintained by a battery supply setup.

The Instruction Cycle

The 6802 is driven by a divided down, TTL system clock. The 6802 then divides this incoming frequency by 4 which results in a Ø1 like signal. A machine cycle is defined as the interval between two successive positive-goint transitions of the phase-one clock signal. An instruction cycle consists of from 2 to 12 machine cycles required to fetch and execute the instruction. The number of machine cycles required depends on the instruction and addressing mode. For more information on these cycles refer to the Motorola M6800 Microcomputer Design Data Manual.

MPU Control Signals

Extal and Xtal. A crystal may be placed across Extal and Xtal for clock generation or in this case Extal is driven by a TTL level and Xtal is left open.

Halt. When asserted, this input causes the 6802 to halt all activity when the current instruction execution is complete. The HALT input is unused in the 7912AD system.

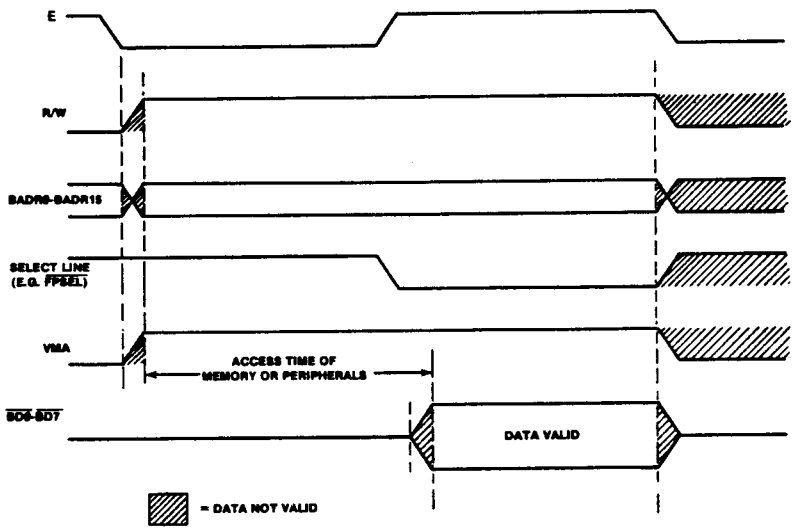
RAM Enable. During a high TTL level, the internal RAM of the 6802 is enabled. It is tied low and always disabled in this case.

For Page 3-47, Paragraph 3.
CHANGE TO READ:

Enable. This TTL leveled signal is equivalent to phase two of the clocking cycles, and is used in the generation of the strobe $\overline{(STB)}$ on the 7912AD.

DESCRIPTION

For Page 3-48, Fig. 3-13.
CHANGE TO READ:



(a) Read cycle timing on the 6802 bus.

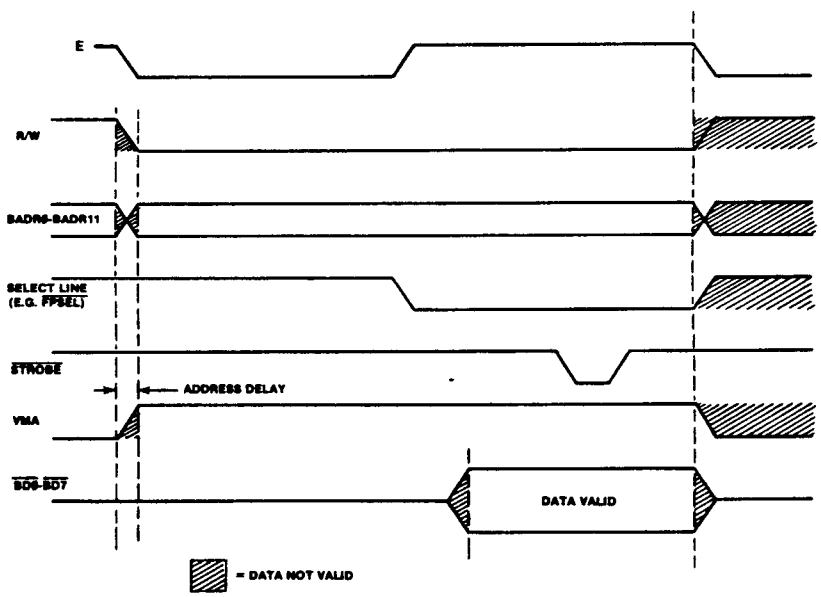


Fig. 3-13. (b) Write cycle timing on the 6802 bus.

DESCRIPTION

For Page 3-51
CHANGE TO READ:

The 6802 Bus

The 6802 communicates with the program memory (ROM), RAM and the instrument functions it controls through a 15-bit address bus, an 8-bit data bus, and a set of device select lines. The 6802 bus, bus drivers, and decoders are shown on diagram 15.

The 15-bit address bus allows the MPU to address 32 k (8000 hex) unique locations including ROM, RAM, and instrument control/status registers. Figure 3-15 shows a map of the 6802 address space. Each of the functions controlled by the 6802 is addressed by the low-order 11 bits of the address bus and one or more select signals derived from A10-A14. For example, to address a location in ROM 2 the MPU asserts the address of the location (in the range of 2000 2FFF) on A0-A14. After a short address settling time, the MPU asserts VMA. The reset signal, RSTOB is high and during the E clock period, pins 4 and 5 of U1220 (center of diagram 15) are low, enabling the decoder. U1220 decodes A12-A14 and asserts pin 13 ($\overline{\text{ROMSEL2}}$), enabling ROM 2 to be addressed by A0-A11. The low order bits (A0-A11) select the individual location within ROM 2.

The other ROM, RAM, and instrument control registers are addressed in a similar manner where U1220 and U200B decode the 5 high-order bits of the address bus (A10-A14) to generate the select signals. Table 3-2 shows the functions selected by each of these signals.

TABLE 3-2
6802 BUS SELECT SIGNALS

SIGNAL NAME	LOWEST ADDRESS	FUNCTION SELECTED
$\overline{\text{FPSEL}}$	5000	Character Generator
$\overline{\text{INTSEL}}$	3C00	6802 Interrupt Control
$\overline{\text{IOSEL}}$	4000	IEEE 488 Interface
$\overline{\text{PISEL}}$	3800	KRO/7K Bus Interface
$\overline{\text{PMCSEL}}$	3400	2900 Memory Controller
$\overline{\text{RAMSEL}}$	0000	MPU RAM Memory
$\overline{\text{ROMSEL1}}$	1000	Diagnostic ROM Space
$\overline{\text{ROMSEL2}}$	2000	ROM 2
$\overline{\text{ROMSEL6}}$	6000	ROM 6
$\overline{\text{ROMSEL7}}$	7000	ROM 7
$\overline{\text{TLTRSEL}}$	3000	Translator

DESCRIPTION

For Page 3-52, Fig. 3-15.
CHANGE TO READ:

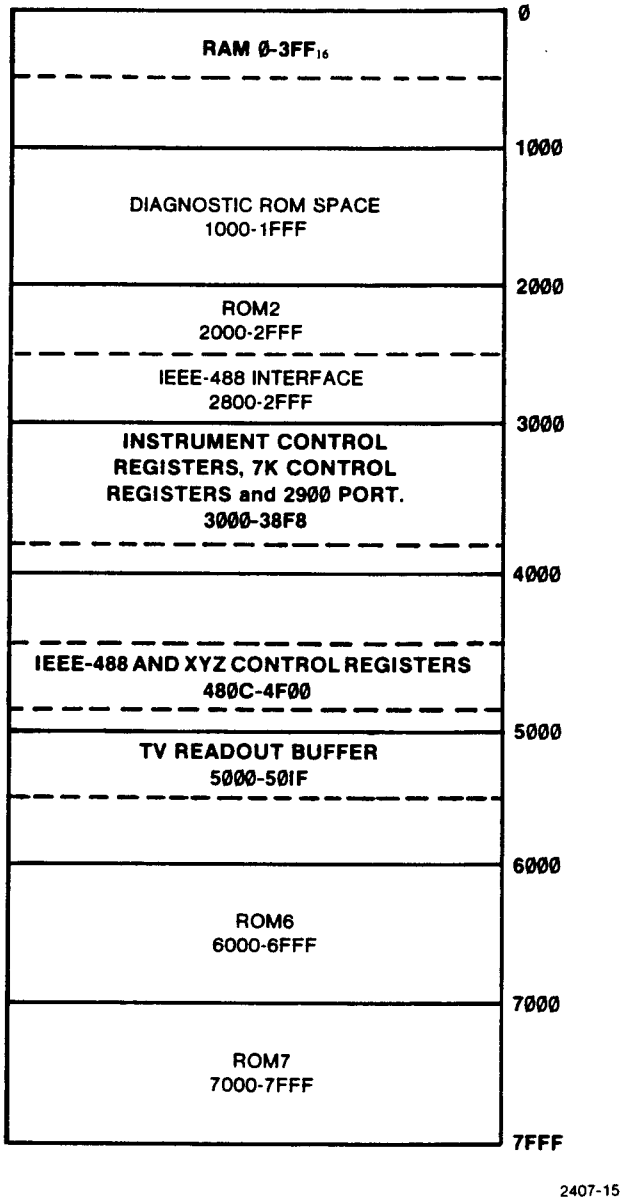


Fig. 3-15. Address map of the 6802 system.

DESCRIPTION

For Page 3-53
CHANGE TO READ:

Bus Buffers

U920 and U930 (top-right of diagram 15) comprise the address bus buffer for the 6802 system bus. The enable inputs (pins 1 and 19 of U920) are tied to ground, so the buffers are always enabled. This buffer also drives the $\overline{\text{WRITE}}$ and $\overline{\text{STROBE}}$ lines. The $\overline{\text{STROBE}}$ pulse occurs at the center of each high state E clock period. This pulse tells devices that the address on the bus is valid and initiates data transfer to or from the selected device. The $\overline{\text{WRITE}}$ line is driven by the MPU R/W output. When $\overline{\text{WRITE}}$ is asserted, the MPU is writing data to the bus. When the MPU is reading data, $\overline{\text{WRITE}}$ is high. The R/W line also controls the 6802 data bus buffers, U1130 and U1030 (top-center of diagram 15). When R/W is low, the output of U1420C is high as well as the output of U1320C, enabling the buffer output drivers. If the MPU is reading data from the bus, R/W is high and the buffer receivers are enabled.

The MPU memory (ROM and RAM) and part of the interface to the 7K plug-in bus are connected directly to the MPU data bus, ahead of the bus buffer. When the MPU addresses these devices, the bus buffer is tri-stated.

MPU Clock Circuit

The 6802 system clock is derived from an 80 MHz master clock on the Data Buffer board (A20). The clock signal is divided down to 10 MHz on the data buffer board and fed to the MPU clock circuit in the bottom-left of diagram 15. The 10 MHz clock drives the clock inputs of two J-K flip flops (U910A and B) in a divide by 3 configuration. The resulting 3.33 MHz drives the clock input of the 6802.

Since both halves of U910 are simultaneously clocked, the outputs will reflect what was on the inputs at the time of the positive transition of the clock. (Refer to Fig. 3-16).

Both J_a and J_b are always high. During T1, assume pin 9 (Q_b) has just went high, placing K_a high also. Since K_a was low during the previous cycle, $\overline{Q_a}$ is presently low.

The transition of T2 places $\overline{Q_a}$ high, but since K_b was low at the time of the T_2 transition, Q_b remains high.

The T3 transition see all inputs high, so all outputs toggle, bringing Q_b to a low.

Going into T1 again with K_a and K_b both low, Q_b goes high starting the process over again.

DESCRIPTION

For Page 3-53 (cont), Fig. 3-16.
CHANGE TO READ:

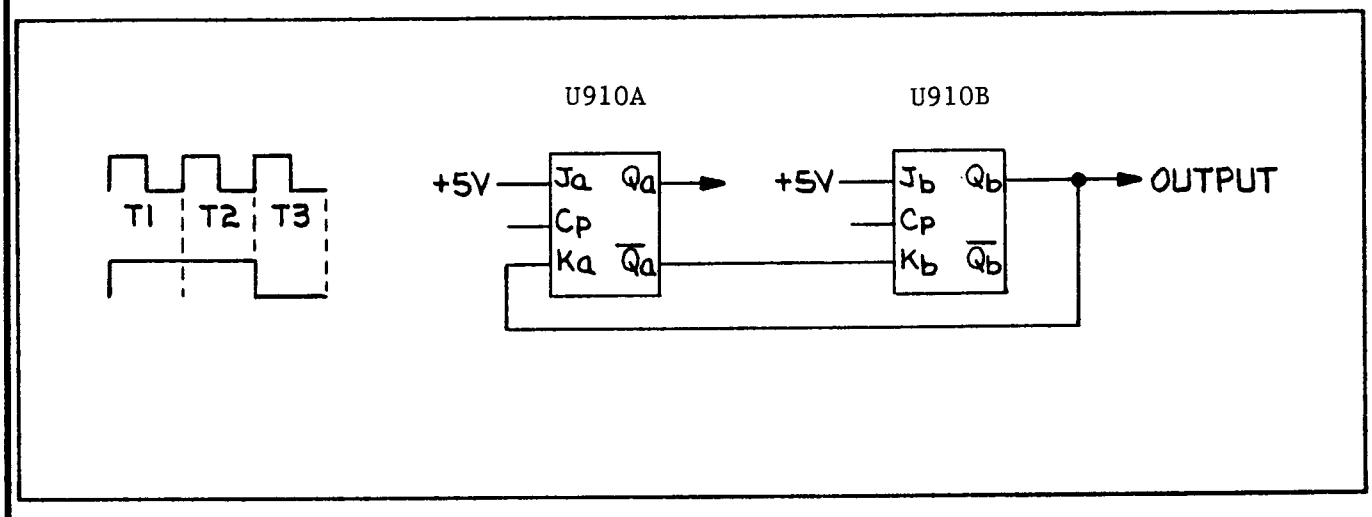


Fig. 3-16. MPU Clock Circuit and Timing.

For Page 3-54
CHANGE TO READ:

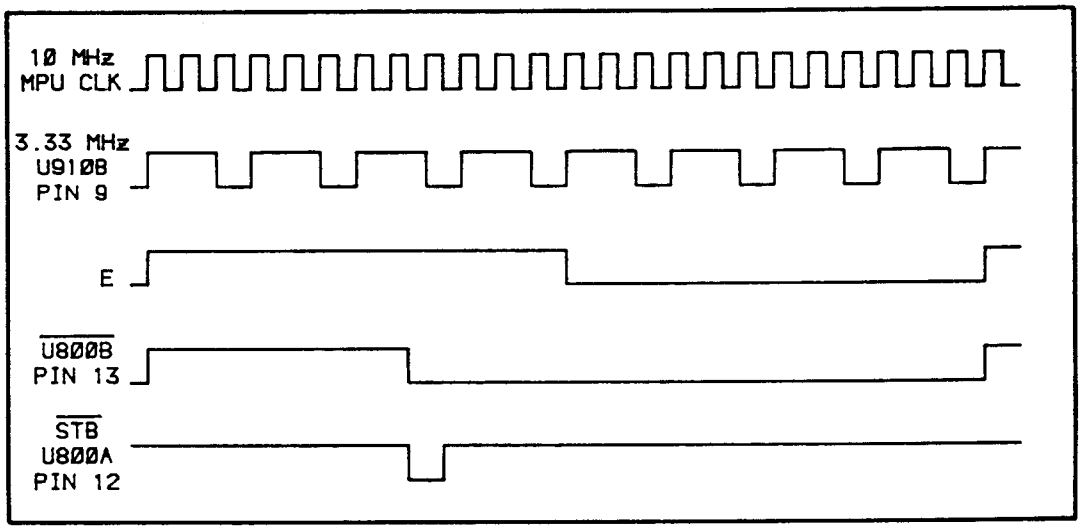


Fig. 3-16A. Timing of 6802 Clock Circuitry.

STROBE. $\overline{\text{STB}}$ is generated from the E output of the 6802 to guarantee synchronization with the E output, as well as, to have a strobe ($\overline{\text{STB}}$) during emulation that is relative to E.

U800B, on the positive edge of E, times the $\overline{\text{STB}}$ to occur in the later half of E. When it times out, U800A is triggered by negative edge of U800B and provides the duration of $\overline{\text{STB}}$. The result is a 100 nanosecond pulse near the middle of each E clock period. See Fig. 3-16A.

DESCRIPTION

For Page 3-55
CHANGE TO READ:

Reset Circuit

When power is applied to the 7912AD, the reset circuit shown at the left-center of diagram 15 asserts the 6802's $\overline{\text{RESET}}$ input, forcing it to execute the initialize and self-test routines that begin at the address stored in 7FFE and 7FFF.

When the 5.1-volt power supply comes up, U1430A is cleared by the RC network of R1530, C1530, and CR1530. The Q output of U1430A is low, so the output of U1330C is high and $\overline{\text{RSTOB}}$ is asserted. The low on $\overline{\text{RSTOB}}$ (Reset) holds the 6802 in an idle state until PON makes a low-to-high transition to indicate that the power supplies are stable. During the delay while the power supplies stabilize, C1530 charges through R1530 and the clear input of U1420A goes high (unasserted). The positive-going transition on PON clocks the Q output of U1420B high, and fires U1420A. The low on U1410A's Q times out, $\overline{\text{RSTOB}}$ goes high, and the 6802 begins executing the initialization and self-test routines.

The $\overline{\text{RSTOB}}$ line also resets logic circuits in the Readout/7K Interface.

Power Fail and Hardware Failure Interrupts

If any of the 7912AD's analog power supplies fall out of tolerance, $\overline{\text{HWF}}$ (Hardware Failure) goes low. If the line input power is interrupted, PON goes low. U1410B provides a time duration to assure a NMI will be generated, even on short $\overline{\text{HWF}}$ transitions. In either case, the output of U7420B goes high. If NMIEN (Non-Maskable Interrupt Enable) is high, U1420D goes low, generating a non-maskable interrupt to the 6802. The NMIEN line is held low (interrupts disabled) during the power-up routine and set high after power-up and self-test are complete.

DESCRIPTION

For Page 3-56
CHANGE TO READ:

MPU Memory

The MPU memory is all on-board. (ROM=3, 4k by 8-bit ROMS, and RAM=2, 1k by 4-bit RAMS.)

When one of the $\overline{\text{ROMSEL}}$ lines is asserted, this enables the appropriate EPROM as well as asserting $\overline{\text{ANSW}}$ through U1210, U1420A, and U1320B. $\overline{\text{ANSW}}$ then tri-states the output data buffers (U1130, U1030). U1120 is also enabled; used as a buffer between the 6802, the memory, and PIA. U1120 is clocked by the R/W signal of the 6802, as well as enabling the output of the selected ROM, after being inverted by U1310F.

RAM is accessed in the same manner, using the R/W signal directly. Both RAM's are selected at the same time, with U1400 providing the upper 4 bits and U1500 providing the lower 4 bits of the 8-bit word going to the processor. Again, $\overline{\text{ANSW}}$ is asserted to tri-state the data output buffers.

U1300 is for use with a diagnostic ROM at a later date. Therefore, it is vacant.

Interrupt Control Logic

The Interrupt Control Logic, shown on diagram 16, consists of two Interrupt Occured Registers, U430 and U1230, and two Interrupt Mask Registers, U330 and U230A. This control logic receives interrupt signals from instrument functions controlled by the 6802. These interrupt signals are ORed together through the Interrupt Mask Registers to drive the $\overline{\text{IRQ}}$ input of the 6802.

DESCRIPTION

For Page 3-46
CHANGE TO READ:

Index Register. The index register can be used to store 16-bit data or an address used in the indexed mode of memory addressing. Instructions are provided in the 6802 instruction set that load, increment, decrement, compare, etc. the index register.

Instruction Register and Decoder/Timing. During an instruction fetch (the first one, two, or three machine cycles, depending on the instruction), successive bytes of an instruction are loaded from the program memory into the instruction register. The contents of this register are, in turn, passed to the decoder and timing logic which decodes the byte(s) and generates the machine states and control signals necessary to execute the instruction. The timing and control block also generates and receives the external control signals.

Data and Address Buffers. These three state buffers isolate the 6802 internal busses from the external data and address busses. The data bus buffer is bidirectional.

RAM/RAM Control. (Not used) Internal RAM is used as primary RAM for program flow or as 128 bytes of extra RAM, 32 bytes of which could be maintained by a battery supply setup.

The Instruction Cycle

The 6802 is driven by a divided down, TTL system clock. The 6802 then divides this incoming frequency by 4 which results in a Ø1 like signal. A machine cycle is defined as the interval between two successive positive-goint transitions of the phase-one clock signal. An instruction cycle consists of from 2 to 12 machine cycles required to fetch and execute the instruction. The number of machine cycles required depends on the instruction and addressing mode. For more information on these cycles refer to the Motorola M6800 Microcomputer Design Data Manual.

MPU Control Signals

Extal and Xtal. A crystal may be placed across Extal and Xtal for clock generation or in this case Extal is driven by a TTL level and Xtal is left open.

Halt. When asserted, this input causes the 6802 to halt all activity when the current instruction execution is complete. The HALT input is unused in the 7912AD system.

RAM Enable. During a high TTL level, the internal RAM of the 6802 is enabled. It is tied low and always disabled in this case.

For Page 3-47, Paragraph 3.
CHANGE TO READ:

Enable. This TTL leveled signal is equivalent to phase two of the clocking cycles, and is used in the generation of the strobe ($\overline{\text{STB}}$) on the 7912AD.

DESCRIPTION

For Page 3-58
CHANGE TO READ:

Q output goes high. This sets bit 0 of the Interrupt Occured Register. The interrupt latched by U702A is unused, (except in troubleshooting test mode). The 6802 clears U220A and U220B by writing to address 3C02. U220A (bottom-center of diagram 16) decodes the address and asserts $\overline{IA2}$. When $\overline{IA2}$ and $\overline{WRITE}$ are asserted, the output of U210A (left-center of the diagram) goes low. The MPU can selectively clear U220B or U220A by asserting $\overline{BD1}$ or BD0] respectively. When $\overline{BD0}$ is low, the output of U210B goes low, clearing U220A and resetting the $\overline{SND}$ interrupt.

Interrupt Mask Registers (U330 and U230A)

U230A	R-REN	X	X	X	X	X	X	X	3C01 (Write only)
Bit	7	6	5	4	3	2	1	0	
U330	IOI	DFI	PMCI	X	FPI	X	X*	SND	3C03 (Write only)

***Diagnostic Interrupt**

3C01 Bit 0-6: Unused.

3C01 Bit 7 - R-REN: When set, this bit masks $\overline{REN}$ interrupts.

3C03 Bit 0 - SND: When this bit is set, $\overline{SND}$ interrupts are masked.

3C03 Bit 1 — Diagnostic only

3C03 Bit 2 — Unused.

3C03 Bit 3 - FPI: When set, front-panel interrupts are masked.

3C03 Bit 4 - FPI: Unused.

3C03 Bit 5 - PMCI: When set, this bit masks memory controller interrupts.

3C03 Bit 6 - DFI: When cleared, duty factor interrups are masked.

3C03 Bit 7 - IOI: When cleared, I/O interrupts are disabled.

The 6802 can mask (disable) $\overline{IRQ}$ interrupts in two ways. All $\overline{IRQ}$ interrupts can be internally masked by setting a bit in the MPU's condition code register. If this bit is set, the Interrupt Control Logic passes interrupts as usual, but the 6802 ignores its $\overline{IRQ}$ input. The 7912AD firmware operating system sets this interrupt mask bit while the 6802 is executing the power-up routine. The mask is also set when routines are being executed that should not be interrupted, such as adjusting the main intensity value.

DESCRIPTION

For Page 3-51
CHANGE TO READ:

The 6802 Bus

The 6802 communicates with the program memory (ROM), RAM and the instrument functions it controls through a 15-bit address bus, an 8-bit data bus, and a set of device select lines. The 6802 bus, bus drivers, and decoders are shown on diagram 15.

The 15-bit address bus allows the MPU to address 32 k (8000 hex) unique locations including ROM, RAM, and instrument control/status registers. Figure 3-15 shows a map of the 6802 address space. Each of the functions controlled by the 6802 is addressed by the low-order 11 bits of the address bus and one or more select signals derived from A10-A14. For example, to address a location in ROM 2 the MPU asserts the address of the location (in the range of 2000 2FFF) on A0-A14. After a short address settling time, the MPU asserts VMA. The reset signal, RSTOB is high and during the E clock period, pins 4 and 5 of U1220 (center of diagram 15) are low, enabling the decoder. U1220 decodes A12-A14 and asserts pin 13 ($\overline{\text{ROMSEL2}}$), enabling ROM 2 to be addressed by A0-A11. The low order bits (A0-A11) select the individual location within ROM 2.

The other ROM, RAM, and instrument control registers are addressed in a similar manner where U1220 and U200B decode the 5 high-order bits of the address bus (A10-A14) to generate the select signals. Table 3-2 shows the functions selected by each of these signals.

TABLE 3-2
6802 BUS SELECT SIGNALS

SIGNAL NAME	LOWEST ADDRESS	FUNCTION SELECTED
$\overline{\text{FPSEL}}$	5000	Character Generator
$\overline{\text{INTSEL}}$	3C00	6802 Interrupt Control
$\overline{\text{IOSEL}}$	4000	IEEE 488 Interface
$\overline{\text{PISEL}}$	3800	KRO/7K Bus Interface
$\overline{\text{PMCSEL}}$	3400	2900 Memory Controller
$\overline{\text{RAMSEL}}$	0000	MPU RAM Memory
$\overline{\text{ROMSEL1}}$	1000	Diagnostic ROM Space
$\overline{\text{ROMSEL2}}$	2000	ROM 2
$\overline{\text{ROMSEL6}}$	6000	ROM 6
$\overline{\text{ROMSEL7}}$	7000	ROM 7
$\overline{\text{TLTRSEL}}$	3000	Translator

DESCRIPTION

For Page 3-68, Paragraph 1.
CHANGE TO READ:

Q540 provides adequate drive for the plug-in interface circuitry. Shortly after ROT goes high, the output of U530D (bottom-left of diagram 17) goes low, asserting $\overline{\text{TIMESLOT}}$. The $\overline{\text{TIMESLOT}}$ pulse drives a voltage source formed by Q409, Q502, and Q504 (left-center of diagram 3). The output of this circuit supplies the voltage source for the outputs of the time-slot counters.

For Page 3-70, Paragraphs 1, 2, & 3.
CHANGE TO READ:

Analog Data Decoder. The Analog Data Decoder (U510 — left-center of diagram 17) converts the current levels it receives fromk the analog multiplexer to a binary code. The 6802 reads this code from the Readout Data Register located at 38EF in the 6802 address space.

The analog data is fed to a current-input analog-to-digital converter (A/D), U510 through a divider network. U510 converts the analog current to a one-of-ten (0-9) code. One output is asserted for each level between 100 and 900 microamps; no outputs are asserted for a 0 milliamp input, U610 converts this one-of-ten code to its 4-bit BCD equivalent and U620 buffers the data onto the 6802 bus.

If the analog input current reaches 1.0 milliamp, the output of comparator U600 goes high, clearing bit 7 ($\overline{\text{BD7}}$) of the readout register. Table 3-8 shows the output codes for each analog input current.

DESCRIPTION

For Page 3-55
CHANGE TO READ:

Reset Circuit

When power is applied to the 7912AD, the reset circuit shown at the left-center of diagram 15 asserts the 6802's $\overline{\text{RESET}}$ input, forcing it to execute the initialize and self-test routines that begin at the address stored in 7FFE and 7FFF.

When the 5.1-volt power supply comes up, U1430A is cleared by the RC network of R1530, C1530, and CR1530. The Q output of U1430A is low, so the output of U1330C is high and $\overline{\text{RSTOB}}$ is asserted. The low on $\overline{\text{RSTOB}}$ (Reset) holds the 6802 in an idle state until PON makes a low-to-high transition to indicate that the power supplies are stable. During the delay while the power supplies stabilize, C1530 charges through R1530 and the clear input of U1420A goes high (unasserted). The positive-going transition on PON clocks the Q output of U1420B high, and fires U1420A. The low on U1410A's Q times out, $\overline{\text{RSTOB}}$ goes high, and the 6802 begins executing the initialization and self-test routines.

The $\overline{\text{RSTOB}}$ line also resets logic circuits in the Readout/7K Interface.

Power Fail and Hardware Failure Interrupts

If any of the 7912AD's analog power supplies fall out of tolerance, $\overline{\text{HWF}}$ (Hardware Failure) goes low. If the line input power is interrupted, PON goes low. U1410B provides a time duration to assure a NMI will be generated, even on short $\overline{\text{HWF}}$ transitions. In either case, the output of U7420B goes high. If NMIEN (Non-Maskable Interrupt Enable) is high, U1420D goes low, generating a non-maskable interrupt to the 6802. The NMIEN line is held low (interrupts disabled) during the power-up routine and set high after power-up and self-test are complete.

DESCRIPTION

For Page 3-83, Paragraph 1.
CHANGE TO READ:

When one of the plug-ins is talking, it places a byte on the bus and pulses $\overline{7KSND}$. The low-to-high transition at the end of the pulse latches the data from the bus in U412. The low-to-high transition on $\overline{SND}$ also generates an interrupt to the MPU, telling it that the PIA has data to be sent on the IEEE 488 bus. The MPU reads the data from the A port of the PIA. If the other plug-in is not addressed to listen (the usual case), the peripheral control output (CA2) is programmed to go low when the MPU reads the data. The low on CA2 causes the output of U580F to go high which in turn causes the output of U630A and $\overline{7KDAV}$ to go low. On the next rising edge of the E clock (pin 25 of the PIA), the CA2 output returns to its high state. The high-to-low transition that results on $\overline{7KDAV}$ tells the plug-in that the byte has been accepted by the 7912AD.

For Page 3-84
CHANGE TO READ:
If one plug-in is addressed to talk and the other to listen, the CA2 output is not asserted when the 6802 reads the data from the PIA. Instead, the CB2 output of the PIA (pin 19) is set to go low when the 6802 writes the data to the output port, When the CB2 goes low as the result of writing data to the PIA output port, U230B is cleared and the low on its Q output enables bus driver U820. On the rising edge of the next E pulse, the PIA's CB2 output returns to its high state. The high on CB2 and the high on the $\overline{Q}$ output of U230A cause the output of U370C to go high, asserting $\overline{7KDAV}$. This signals the listening plug-in that the data on the 7K bus is valid. When the plug-in accepts the data, it releases $\overline{7KNDAC}$. The positive transition clocks U230B, setting its Q output high to disable the bus drivers and its $\overline{Q}$ output low, to release $\overline{7KDAV}$. The positive transition on $\overline{7KDAV}$ signals the talking plug-in that the transfer is complete. The positive transition on the Q output of U230B also generates an interrupt through the CA1 input of the PIA. This interrupts tells the 6802 that the source handshake was completed. If, for some reason, the listening plug-in doesn't release $\overline{7KNDAC}$, the source handshake can be terminated by clearing bit 1 of the 7K bus control register (pin 19 of U830). Clearing this bit asserts the set input of U230B, resetting it to its idle state.

If either of the plug-ins assert $\overline{7KSRQ}$, the PIA generates an interrupt to the 6802 through IRQB. The 6802 echoes this SRQ to the external IEEE 488 bus. The plug-in reports its status when polled by the controller-in-charge.

7K Bus Control Register. The 6802 controls the 7K management bus and other 7K bus functions through the 7K Bus Control Register. The register, U830 in the bottom-center of diagram 17, is located at 38F8 in the 6802 address space. When the 6802 places the register's address on its bus, $\overline{PISEL}$ (pin 1 of U300A, bottom-left of diagram 17) is asserted. Recall that the $\overline{STROBE}$ pulse occurs near the middle of each E clock period. As a result, the output of U300A ($\overline{PISTROBE}$) follows the $\overline{STROBE}$ line when $\overline{PISEL}$ is asserted. Data from the 6802 bus is latched into the 7K Bus Control Register on the rising edge of $\overline{PISTROBE}$.

Table 3-11 lists the name and function of the bits in the register.

DESCRIPTION

For Page 3-85, Table 3-11. & Paragraph 1.
CHANGE TO READ:

TABLE 3-11

7K BUS CONTROL REGISTER BITS

BIT	NAME	FUNCTION
Ø	7KTST	Diagnostic "IN TEST" only
1	$\overline{\text{HSRST}}$	Resets source handshake
2	$\overline{\text{7KRVADR}}$	Addresses right (horizontal) plug-in
3	$\overline{\text{7KLVADR}}$	Addresses left (vertical) plug-in
4	7KREN	7K Remote Enable (inverted)
5	$\overline{\text{7KATN}}$	7K Attention (inverted)
6	$\overline{\text{7KIFC}}$	7K Interface Clear (inverted)
7	$\overline{\text{7KEOI}}$	7K End or Identify (inverted — output with source handshake only)

Bits 4-7 of the 7K Bus Control Register drive one of the 7K management bus lines through an inverter (U730 C through F). The function of these lines was previously discussed. Bits 1, 2, and 3 of the register drive the $\overline{\text{HSRST}}$, $\overline{\text{7KRVADR}}$ and $\overline{\text{7KLVADR}}$ lines respectively.

Scans
By
Artek Media

Artek Media
1042 Plummer Cir. SW
Rochester, MN 55902

www.artekmedia.com

"High resolution scans of obsolete technical manuals"

If your looking for a quality scanned technical manual in PDF format please visit our WEB site at www.artekmedia.com or drop us an email at manuals@artekmedia.com and we will be happy to email you a current list of the manuals we have available.

If you don't see the manual you need on the list drop us a line anyway we may still be able to point you to other sources. If you have an existing manual you would like scanned please write for details, This can often be done very reasonably in consideration for adding your manual to our library.

Typically the scans in our manuals are done as follows;

1) Typed text pages are typically scanned in black and white at 300 dpi.
2) Photo pages are typically scanned in gray scale mode at 600 dpi
3) Schematic diagram pages are typically scanned in black and white at 600 dpi unless the original manual had colored high lighting (as is the case for some 70's vintage Tektronix manuals).

If you purchased this manual from us (typically through our Ebay name of ArtekMedia) thank you very much. If you received this from a well-meaning "friend" for free we would appreciate your treating this much like you would "share ware". By that we mean a donation of at least $5-10 per manual is appreciated in recognition of the time (a manual can take as much as 40 hours to reproduce, book, link etc.), energy and quality of effort that went into preserving this manual. Donations via PayPal go to: manuals@artekmedia.com or can be mailed to us the address above.

Thanks

Dave & Lynn Henderson
Artek Media